Silicon Carbide Power Device Performance Under Heavy-Ion Irradiation

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Abstract: Heavy-ion induced degradation and catastrophic failure in SiC power MOSFETs and diodes are examined to provide insight into the challenge of single-event effect hardening of SiC power devices.

Introduction

This work presents heavy-ion test data for several SiC power MOSFETs and diodes in order to increase the body of knowledge that will enable single-event effect (SEE) hardening of this technology. Specifically, diode data and MOSFET current signatures under different bias, temperature, and beam conditions are presented for devices from different manufacturers or different generations within a single manufacturer, and the emerging patterns are discussed.

Both the performance benefits of SiC over Si power devices (Fig. 1) and the high tolerance of commercial SiC components to total ionizing dose (TID) [1-3] have enhanced the allure of SiC technology in the aerospace community. To date, however, SiC power devices have not performed well under heavy-ion irradiation, suffering permanent degradation and/or catastrophic SEE (Fig. 2, modified from [6]) [4-6]. The mechanisms of heavy-ion induced degradation and failure are an active area of research [6-9].

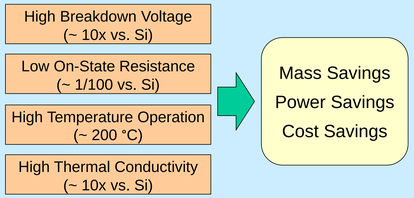

Fig. 1. Benefits of SiC power technology as compared to silicon.

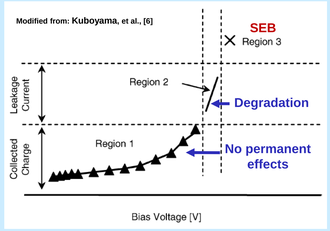

Fig. 2. Power diode response to heavy-ion irradiation range from no permanent effect to leakage current degradation to sudden catastrophic single-event burnout (SEB) depending on the reverse bias voltage (V_R) during irradiation [6].

Test Methods and Devices

Table I: Summary of SiC Power Devices Tested

Device Type	Technology	# of Part Types/ Manufacturers	Voltage Rating *(V)*
Power MOSFET	VDMOS*	7/4	1200 – 3300
Diode	SBD†	3/3	650 – 1200
Diode	PiN	2/1	1200 – 3300

*VDMOS: Vertical, planar gate double-diffused power MOSFET
†SBD: Schottky barrier diode

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Part Preparation

- Decapsulation via acid-etching or manufacturer-supplied unlidded.
- 1-mil parylene-C deposited to prevent arcing.
- Typical sample size of each part type: 15 pieces

Beam Conditions

- Heavy-ion beam facility and properties given in Table II.
  - Flux range: under 10 $cm^{-2} \cdot s^{-1}$ up to 5×10^3 $cm^{-2} \cdot s^{-1}$.

Diode Single-Event Effect Testing

- Test conditions:
  - Reverse bias (V_R) incremented before each run;
  - DC peak reverse voltage (V_{RRM}) and I-V curves measured after each run.
- Failure criteria:
  - Maximum bias yielding no degradation: no measurable change in reverse current (I_R) pre- vs. post-irradiation;
  - Threshold bias for sudden SEB: catastrophic failure (ΔI_R > 20 mA, shorted device) upon beam shutter opening.

Power MOSFET Single-Event Effect Testing

- Test conditions:
  - Gate-source voltage (V_{GS}) held at 0 V (off-state);
  - Drain-source voltage (V_{DS}) incremented before each run;
  - Post-irradiation gate stress (PIGS) test performed and breakdown voltage (BV_{DSS}) measured after each run.
- Failure criteria:
  - Maximum bias yielding no degradation: no change in PIGS or BV_{DSS} pre- vs. post-irradiation;
  - Onset bias for current degradation: lowest bias yielding measurable change in gate (I_G) or drain (I_D) current during run;
  - Threshold bias for sudden SEE: catastrophic failure (ΔI_D > 20 mA and BV_{DSS} < 1 V (shorted), or ΔI_G > 1 mA) immediately upon beam exposure.

Table II: Heavy Ion Facilities and Ions Used Values are Surface-Incident to the Die

Facility	Ion	Energy *(MeV)*	LET* (SiC) *(MeV-cm²/mg)*	Range (SiC) *(μm)*
TAMU	Ne	267	2.9	177
	Ag	1110	49	66
	Xe	1291	60	64
LBNL	Ar	361	11	77
	Cu	566	23	61
	Kr	750	34	62
	Xe	996	65	45

*LET = linear energy transfer

Results

Tables III and IV summarize results of the discrete power diode and MOSFET responses to heavy-ion irradiation. Device hardness was evaluated principally under Ag and Xe irradiation to reveal performance at typical robotic mission SEE hardness requirement conditions (LET > 40 MeV-cm^2/mg in silicon, range to Bragg peak > overlayer + epilayer thickness). Diode ("D") and MOSFET ("M") manufacturers are distinguished by numerical identification; different parts from the same manufacturer are further distinguished by sequential lettering ("A", "B", etc.). See Test Methods section for definitions and criteria for the tabulated device responses. Importantly, the threshold bias condition necessary for catastrophic SEB or single-event gate rupture (SEGR) cannot be identified due to the rapid degradation and damage to the device when irradiated at biases just below that resulting in immediate catastrophic failure upon beam exposure [6]. In Table IV, V_{DS} levels falling between the maximum bias at which no damage was measured (column 4) and the onset bias for current degradation (column 5), resulted in latent degradation identified only after beam exposure during PIGS or BV_{DSS} testing. The degradation revealed by these tests was in part a function of ion fluence as opposed to a true single-event effect.

Table III: Summary of Discrete Power Diode Test Results

Ion	Device	Type	Rated Voltage	Max V_R No Degradation	Min V_R Sudden SEB *V*	Min V_R Sudden SEB %
1110 MeV Ag	D1A	PiN	1200	350 ≤ V_R < 375	425 < V_R ≤ 500	35% - 42%
	*D1B	PiN	3300	400 ≤ V_R < 450	800 < V_R ≤ 1000	24% - 30%
	D2	SBD	1200	100 ≤ V_R < 200	500 ≤ V_R ≤ 550	42% - 46%
	D3	SBD	1200	not found (< 350)	475 < V_R ≤ 500	40% - 42%
	D4	SBD	650	150 ≤ V_R < 175	250 < V_R ≤ 300	38% - 46%
1291 MeV Xe	D2	SBD	1200	150 ≤ V_R < 175	not found (see Ag)	
	D4	SBD	650	150 ≤ V_R < 175	not found (see Ag)	
996 MeV Xe	D1A	PiN	1200	325 ≤ V_R < 350	450 < V_R ≤ 475	38% - 40%
278 MeV Ne	D3	SBD	1200	550 ≤ V_R < 600	600	50%

*Small sample size; older-quality wafer

Table IV: Summary of Power MOSFET Test Results at 0 V_{GS}

Ion	Device	Rated Voltage	Max V_{DS} No Damage	Onset V_{DS}: I_D, I_G Degradation $I_G = I_D$	$I_D > I_G$	Min V_{DS} Sudden SEE
1110 MeV Ag	M1	1200	50 < V_{DS} < 75	200 ≤ V_{DS} < 225	350 < V_{DS} < 400	500 < SEB ≤ 600
	M6	1200	25 < V_{DS} < 50	50 < V_{DS} < 100	not found	SEE ≤600 (see Xe)
996 MeV Xe	M1	1200	50 < V_{DS} < 75	200 < V_{DS} < 300	400 < V_{DS} < 425	450 < SEB ≤ 500
	M2A	1200	40 < V_{DS} < 50	< 182	*400 < V_{DS} < 500	600 < SEB ≤ 700
	M2B	1200	50 < V_{DS} < 60	< 182	300 < V_{DS} < 400	not found (> 500)
	M2C	3300	50 < V_{DS} < 75	n/a†	325 < V_{DS} < 350	600 < SEB ≤ 800
	M5	1200	40 < V_{DS} < 50	< 182	200 < V_{DS} < 400	400 ≤ SEE ≤ 600
	M6	1200	not found	not found	not found (≤ 500)	SEE >500 (see Ag)
566 MeV Cu	M5	1200	70 < V_{DS} < 80	200 < V_{DS} ≤ 400	not found (> 400)	400 < SEB ≤ 600

*Onset > 400 V based on 4 samples irradiated to low, 1×10^3 cm^{-2} fluence
†Latent gate damage only; during beam exposure, all events resulted in $I_D > I_G$

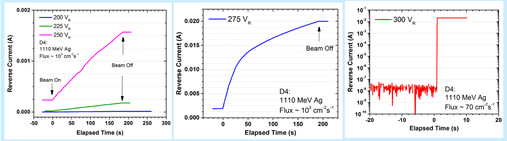

Fig. 3. D4 response to Ag radiation. Left: I_R degradation is proportional to fluence (ϕ); rate increases (non-linearly) with V_R [6]. Middle: SEB susceptibility is reduced by damage [6] and functionality is gradually lost. $dI_R/d\phi$ decreases possibly due to reduced mobility (thus impact ionization) from heat and/or collapsed drift fields from the distributed excessive I_R. Right: Immediate SEB upon a pristine D4 sample exposure to Ag ions.

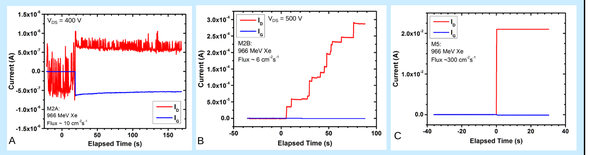

Fig. 5.A-C. Four possible regions of SiC MOSFET response include latent damage (not shown); Ig = Id runtime events (A); Id > Ig runtime events (B); and sudden catastrophic SEB (C).

Discussion

Several conclusions emerge from Tables III & IV:

- PiN diodes exhibit higher onset V_R for heavy-ion induced degradation of I_R than do SBDs, but similar susceptibility to sudden SEB.
  - Different mechanisms may be responsible for the two responses.
- Not surprisingly, PiN diode performance is more comparable to power MOSFET I_{DS} and sudden SEB performance than is SBD performance.
- Gate leakage current effects (latent and prompt) show the most variability between part types and manufacturers.
  - Process and geometry play an important role in I_G-related effects.
- Known defect-dense SiC material results in sudden SEB at a lower fraction of rated V_R.

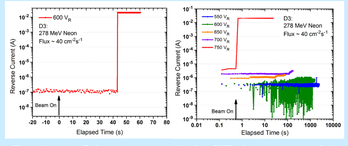

Fig. 4. Low-Z ion exposure. Left: SEB in absence of I_R degradation. Right: Despite minimal degradation at lower V_R, sudden SEB occurs at a higher V_R (750 V vs. 600 V) than sample on left, possibly due to inhibition by prior damage [6]. Note $dI_R/d\phi$ increases slightly with total fluence.

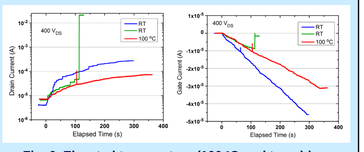

Fig. 6. Elevated temperature (100 °C, red trace) has no effect on SEE in SiC power MOSFETs

Discussion Cont'd

In silicon power MOSFETs, SEB susceptibility during radiation testing is often reduced by elevated temperature and/or by the addition of a drain resistor to dampen the drain voltage and suppress second breakdown. In two of the SiC power MOSFETs studied here, elevated temperature tests did not impact current degradation or sudden SEB onset, suggesting different fundamental mechanisms are involved in SiC power devices.

Small sample sizes limit the conclusions that can be drawn from the studies conducted here. It is hoped that this work will contribute meaningfully to the growing collaboration of SiC power device researchers seeking to understand the failure mechanisms in order to harden these devices against heavy ions and neutrons.

Conclusions

From the work presented here and performed by others, it is clear that serendipitously SEE-hard commercial SiC power devices are rare or non-existent. Most space applications will require SiC power devices that have been hardened to SEE.

All commercial SiC power devices evaluated here exhibit immediate catastrophic SEE at biases below 60 % of their rated breakdown voltage and experience permanent degradation down to much lower biases (< 10 % for MOSFETs). The catastrophic SEE safe operating area falls within the range of biases at which cumulative degradation occurs and at this time cannot be established for space applications. This limitation is compounded by the unknown impact of the non-catastrophic, cumulative heavy-ion damage on device life time. Much work remains to be done to reliably introduce SiC technology into space applications.

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