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Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

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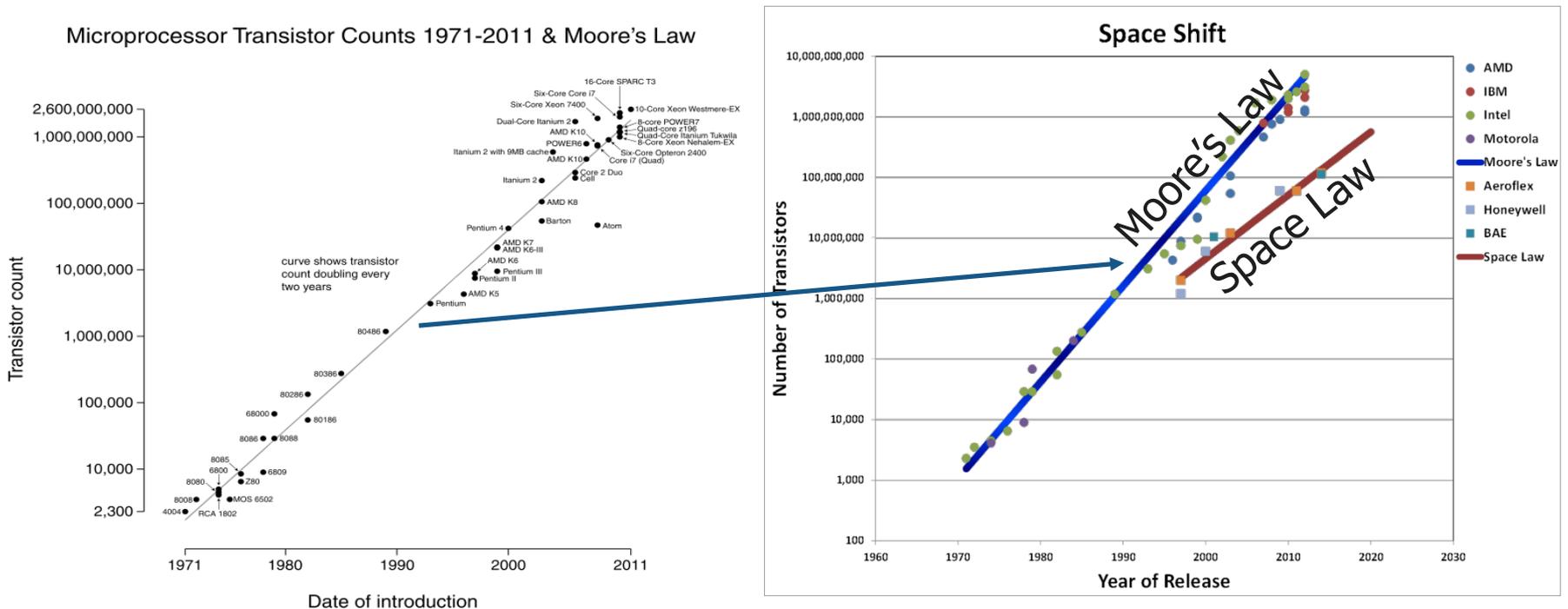
Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

- **Abstract:** *The advent of Class Y flip chip on ceramic package technology is a key enabler for 90nm ASIC's for space. However, limitations of ceramic packages in turn limit utilization of sub-90nm nodes, driving the need for organic substrate technology. Thus a flip chip on organic feasibility study has been completed looking at the effects of underfill and moisture on reliability.*
- **Acknowledgement:** *The authors would like to acknowledge the significant contributions of JPL Materials Scientist/Engineer Jong-ook Suh, Ph.D. Dr. Suh provided invaluable guidance in scoping and executing this feasibility study. Funding provided by the NEPP program is also gratefully acknowledged, without which this study would not have been possible.*

Cobham Flip Chip Package Technology

Space Law – Moore’s Law Adjusted for Space Applications

- Moore’s Law: The number of transistors will double every two years
- Space Law: The number of transistors will quadruple every six years
- Space lags Moore’s Law in both offset and rate of growth
- *Flip chip technology is critical for closing the gap between Moore and Space*

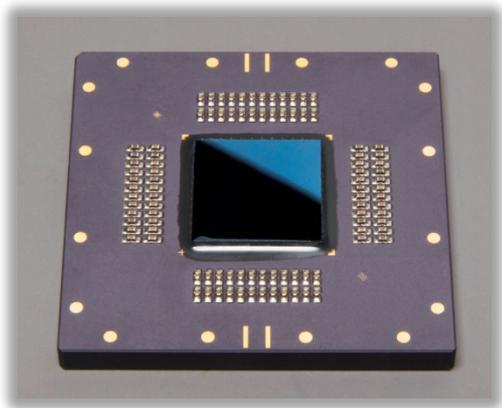


- MIL-PRF-38535 Revision K – released on December 2013
 - Defines for the first time Class Y requirements for ceramic non-hermetic packages for space applications
 - First DLA Class Y flip chip audit completed at Cobham Semiconductor Solutions COS facility in August 2014
 - *First DLA Class Y certification awarded to the Cobham COS facility in December 2014*
 - Stipulates that a Package Integrity Demonstration Test Plan (PIDTP) be performed for all new package technologies
 - Flip chip assembly, Chip cap attach, Heat sink attach all require PIDTP reliability assessments
 - *PIDTP reliability assessments completed by Cobham in December 2015 in support of its UT1752FC Class Y package qualification effort*

Cobham Class Y Package Technology

Class Y Technology as a 90nm Enabler

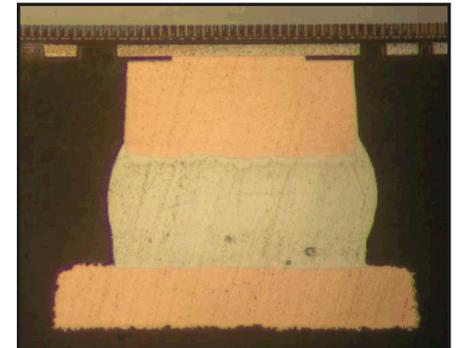
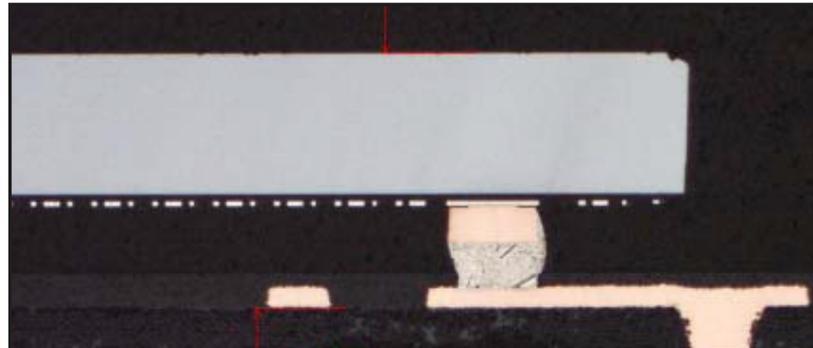
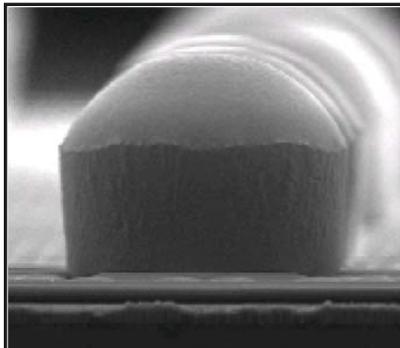
- *UT1752FC Class Y Non-hermetic Package Technology for Space*
 - Flip chip on ceramic, with decoupling capacitors and heat sink attach
 - Cobham COS awarded first ever Class Y certification by DLA in December 2014
- *90nm ASIC Class Y Assembly*
 - 90nm SerDes technology, enabled by Class Y package technology
 - Product qualification scheduled to complete in Q2 2017



Next Generation Flip Chip Technology

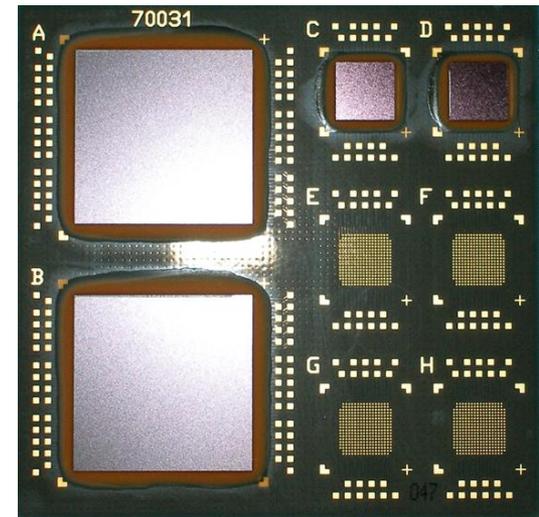
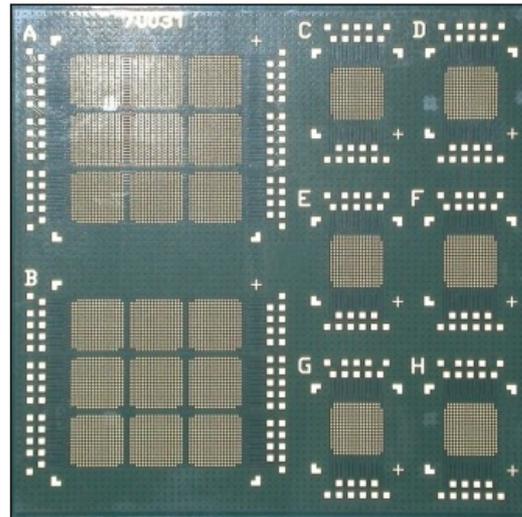
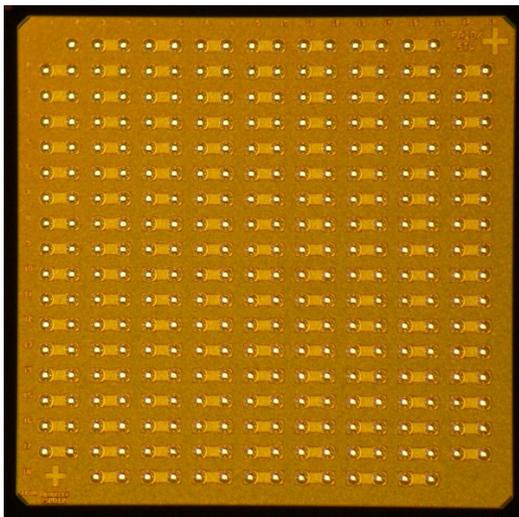
Flip Chip on Organic Technology as a sub-90nm Enabler

- Flip Chip on Organic Substrate Package Technology
 - *Ceramic package technology is becoming the limiting factor for sub-90nm technology nodes, limiting performance/speeds to ~6 Gpbs*
 - Kyocera High Density Build-Up (HDBU) “organic” substrate technology is capable of handling speeds associated with sub-90nm technology nodes (>10 Gbps)
- Fine Pitch Flip Chip with Copper Pillar Interconnects
 - *Sub-90nm technology nodes typically utilize fine pitch die I/O (150µm or less) that in turn require copper pillar flip chip interconnects as opposed to solder*
 - Solder interconnects limited to pitches of ~200µm, while copper pillar interconnects can accommodate pitches down to 100µm or less



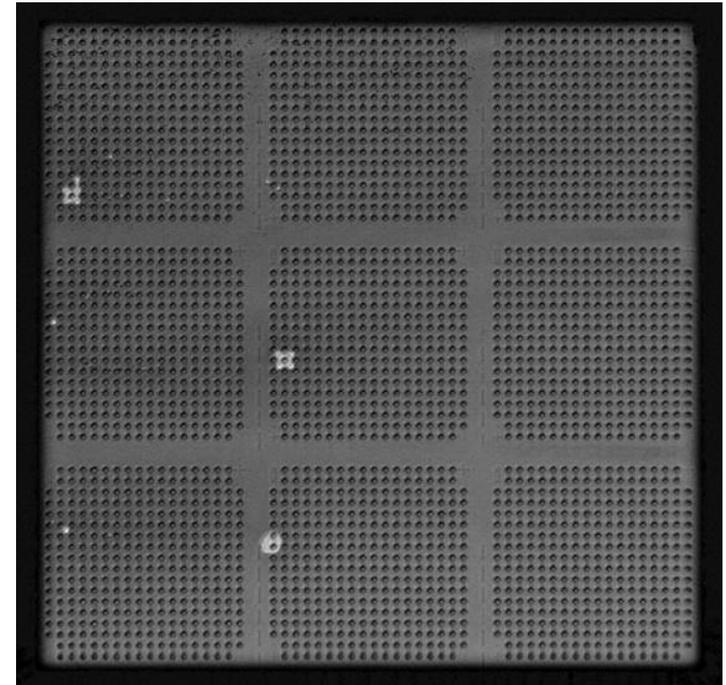
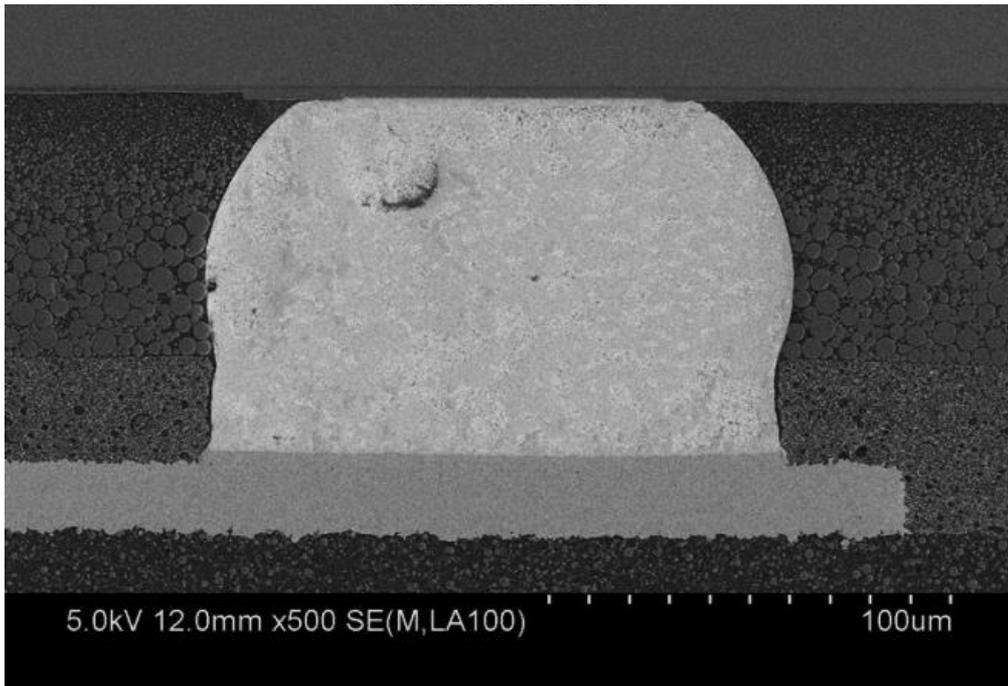
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- *FA10 Flip Chip Daisy Chain Test Die*
 - 254µm bump pitch, 110µm bump height
 - Eutectic Sn/Pb solder alloy; FCI wafer bumping technology
 - 5x5mm (317 I/O) and 15x15mm (2,853 I/O) die sizes
- *Organic High Density Build-Up (HDBU) test substrate*
 - Dual-sided, 1.0mm thick
 - 127µm solder mask defined pads with ENIG plating



Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

- *Cross-section and CSAM Assembly Monitors*
 - Solder joint integrity at die and substrate interface
 - Minimal underfill void content (much less than 10% allowable)



Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

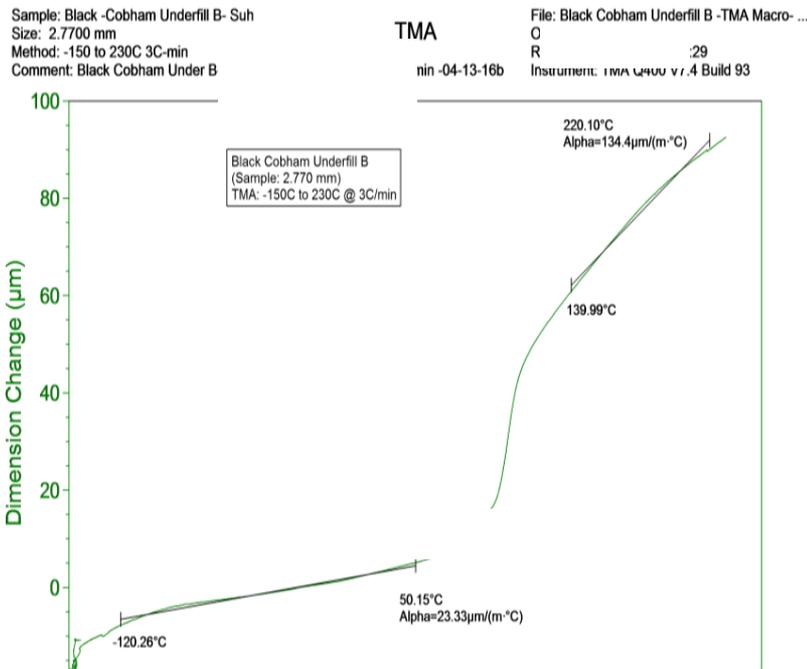
- *Underfill Material Selection*

- “Control” qualified for Class Y applications; meets TM5011 requirements
 - $T_g = 120^{\circ}\text{C}$, $\text{CTE} = 28\text{ppm/C}$
- Underfill “A” selected due to its T_g that is higher than that of the Control
 - $T_g = 135^{\circ}\text{C}$, $\text{CTE} = 27\text{ppm/C}$
- Underfill “B” selected due to its CTE being lower than that of the Control
 - $T_g = 115^{\circ}\text{C}$, $\text{CTE} = 22\text{ppm/C}$
- *All three underfill materials meet outgassing requirements*

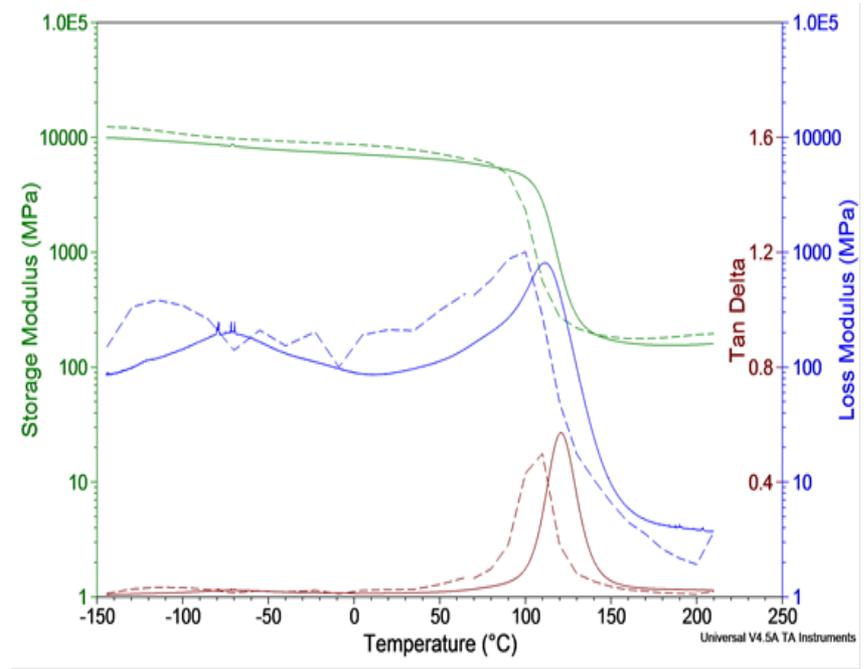
Underfill	IWV per TM1018 (5000ppm limit)	TML per ASTM E-595 (1.0% limit)	CVCM per ASTM E-595 (0.1% limit)
Control	816ppm	0.24%	0.01%
A	518ppm	0.18%	0.00%
B	612ppm	0.19%	0.01%

Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

- *Underfill Material Mechanical Characterization (Underfills A and B)*
 - Differential Scanning Calorimetry (DSC), Dynamic Mechanical Analysis (DMA) and Thermo Mechanical Analysis performed over temperature
 - Required for detailed finite element analysis



TMA Example (Underfill B)



DMA Example (Underfill B)

Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

- Reliability Assessments*

Test Type	Test Method	Criteria	Status
Flip Chip Pull-Off Test Assembly Monitor	MIL-STD-883, TM 2031 • Pre underfill	Minimum load of 18.1kg	Pass
CSAM Assembly Monitor	MIL-STD-883, TM 2030 • Post underfill	Underfill void content < 10% of die area	Pass
Stud Pull Test Assembly Monitor	MIL-STD-883, TM 2027 • Post underfill	Minimum load of 10.7kg	Pass
Cross Section Assembly Monitor	IAW Cobham specification 49210 • Post underfill	0 defects allowed related to solder joints or underfill	Pass
High Temperature Storage Testing	JEDEC JESD22-A103C • High temperature storage at 125°C and 150°C • Endpoints every 250 hours, up to 2000 hours; extended testing to 4000 hours	Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure	Pass 4000 hrs at 125°C

Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

- Reliability Assessments*

Test Type	Test Method	Criteria	Status
Temperature Cycle Testing Fast Ramp Rate (~3.5C/sec) Slow Ramp Rate (~0.2C/sec)	MIL-STD-883, TM 1010, Condition B (-55/125°) <ul style="list-style-type: none"> 250 cycle endpoints, or as appropriate Test to failure, or 3000 cycles, whichever occurs first Failure analysis 	Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure	Refer to following slides
Moisture Loading	JEDEC JESD22-A101 <ul style="list-style-type: none"> 1000 hours at 85°C/85%RH Endpoint testing at 0 and 1000 hours Continuity testing Stud pull testing per TM 2027 	Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure	Pass
Moisture Loading Temperature Cycle Testing	JEDEC JESD22-A101 <ul style="list-style-type: none"> 1000 hours at 85°C/85%RH MIL-STD-883, TM 1010, Condition B (-55/125°C) <ul style="list-style-type: none"> 250 cycle endpoints Test to 3000 cycles 	Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure	Refer to following slides

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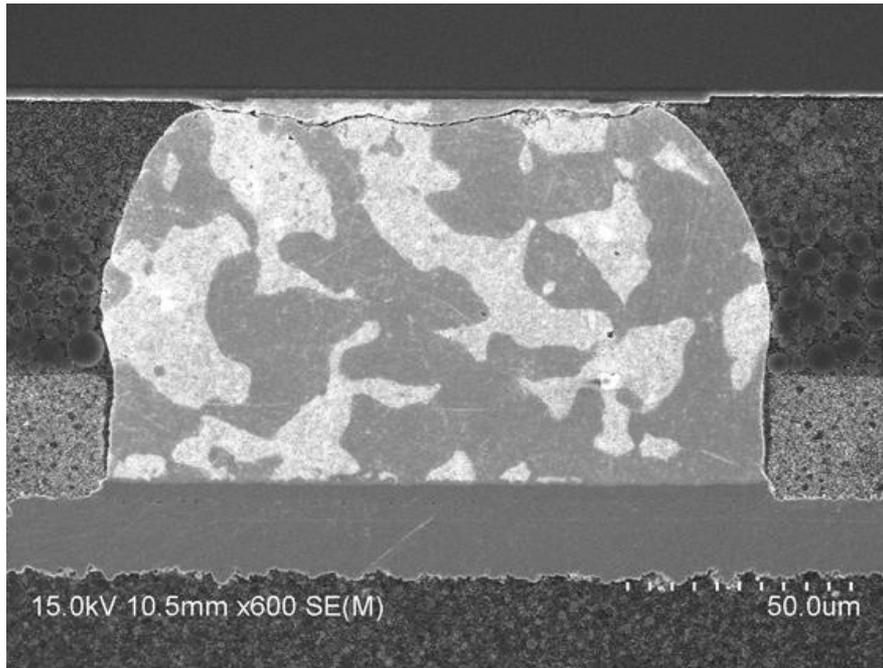
- *125°C High Temperature Storage Testing*
 - 4000 hours completed with no failures detected
- *150°C High Temperature Storage Testing*
 - First failure detected at 750 hour endpoint
 - Failures indicative of UBM consumption due to thermal migration
- *No HTS dependence on underfill material observed*
 - All three underfill materials pass 4000 hours at 125°C
 - Failures at 750 hours at 150°C with all three underfill materials
- *No HTS dependence on substrate material observed*
 - Flip chip on organic results consistent with those for Class Y flip chip on ceramic results
 - HTS at 150°C limited by UBM consumption

Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

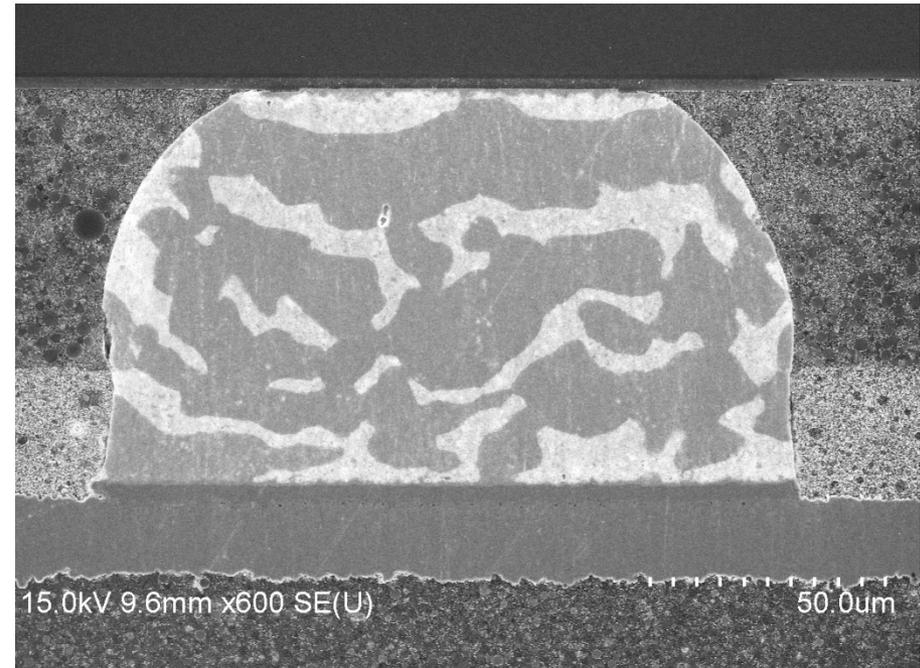
- *Fast Ramp Rate Condition B Temperature Cycle Testing (-55/125°C)*
 - 3000 fast ramp rate cycles completed ($\sim 3.5\text{C/sec}$)
- *Die Size Dependence Observed (5x5mm vs 15x15mm die size)*
 - No failures with 5x5mm die, across all underfill materials
- *Underfill Dependence Observed (15x15mm die size)*
 - Control: First failure at 250 cycle endpoint; 100% failure at 3000 cycles
 - A: First failure at 2000 cycle endpoint; 70% failure at 3000 cycles
 - B: First failure at 2250 cycle endpoint; 10% failure at 3000 cycles
- *Slow Ramp Rate Condition B Temperature Cycle Testing (-55/125°C)*
 - 1750 slow ramp rate cycles completed to date ($\sim 0.2\text{C/sec}$)
 - Testing to continue to 3000 cycles
 - Similar failure rates compared to fast ramp rate temperature cycle testing

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- *Fast Ramp Rate Temperature Cycle Cross Section Failure Analysis*
 - Significant grain coarsening between lead and tin components (typical)
 - Interconnect failure due to underfill delamination (Underfill A)



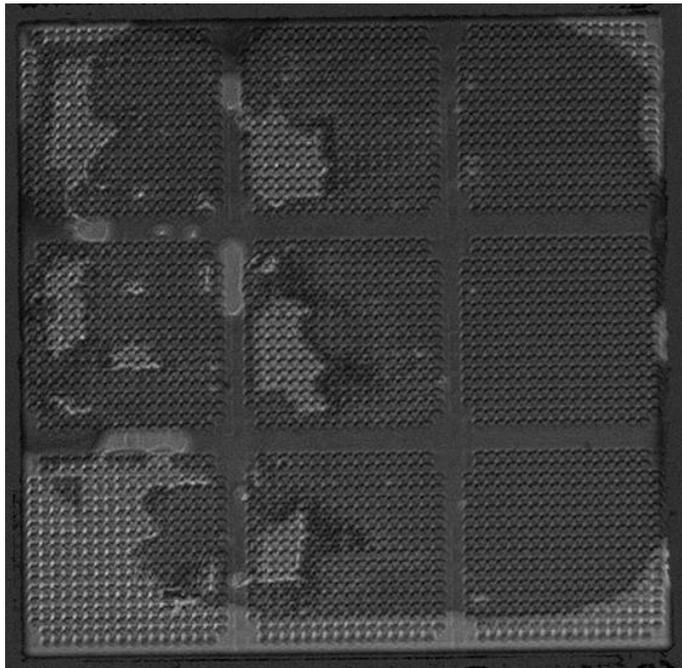
Failed solder interconnect after 3000 cycles
(Underfill A)



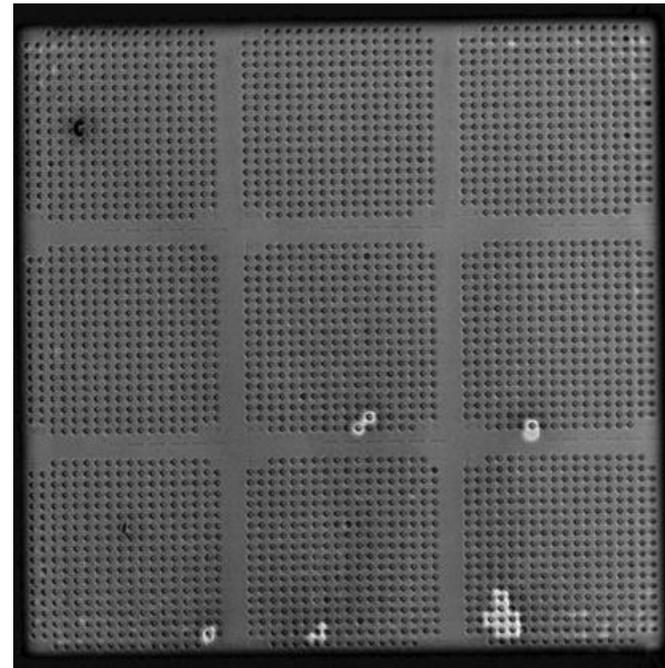
Passing solder interconnect after 3000 cycles
(Underfill B)

Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

- *Fast Ramp Rate Temperature Cycle CSAM Failure Analysis*
 - CSAM analysis performed after 3000 cycle endpoint
 - Evidence of delamination with Underfill A; no evidence with Underfill B



Strong evidence of underfill delamination
(Underfill A)



No evidence of underfill delamination
(Underfill B)

Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

- *Moisture Loading*
 - 1000 hours completed at 85°C/85%RH moisture loading
 - All parts pass continuity testing and stud pull monitor
- *Effect on Fast Ramp Rate Temperature Cycle Testing (3000 cycles)*
 - Accelerated failure rate with Control and Underfill A
 - No effect on failure rate observed with Underfill B
- *Effect on Slow Ramp Rate Temperature Cycle Testing (1750 cycles)*
 - No effect on Control underfill; still early failures at 250 cycles
 - Accelerated failure rate with Underfill A
 - No effect on failure rate observed with Underfill B

Flip Chip on Organic Substrates: A Feasibility Study for Space Applications

- Conclusions

- Underfill selection with respect to temperature cycle resistance and influence of moisture loading is critical
 - Underfill B outperforms Control and Underfill A materials
 - Underfill CTE match to solder appears to increase reliability
- The study demonstrates the feasibility of flip chip on organic substrate technology for use in space applications
 - Underfill B flip chip on organic assemblies exhibit comparable reliability to Class Y flip chip on ceramic assemblies with the Control underfill

- Future Work

- Perform detailed reliability assessments focused on Underfill B as well as other viable candidates
- Evaluate fine pitch flip chip on organic substrate technology
- Evaluate copper pillar flip chip interconnects