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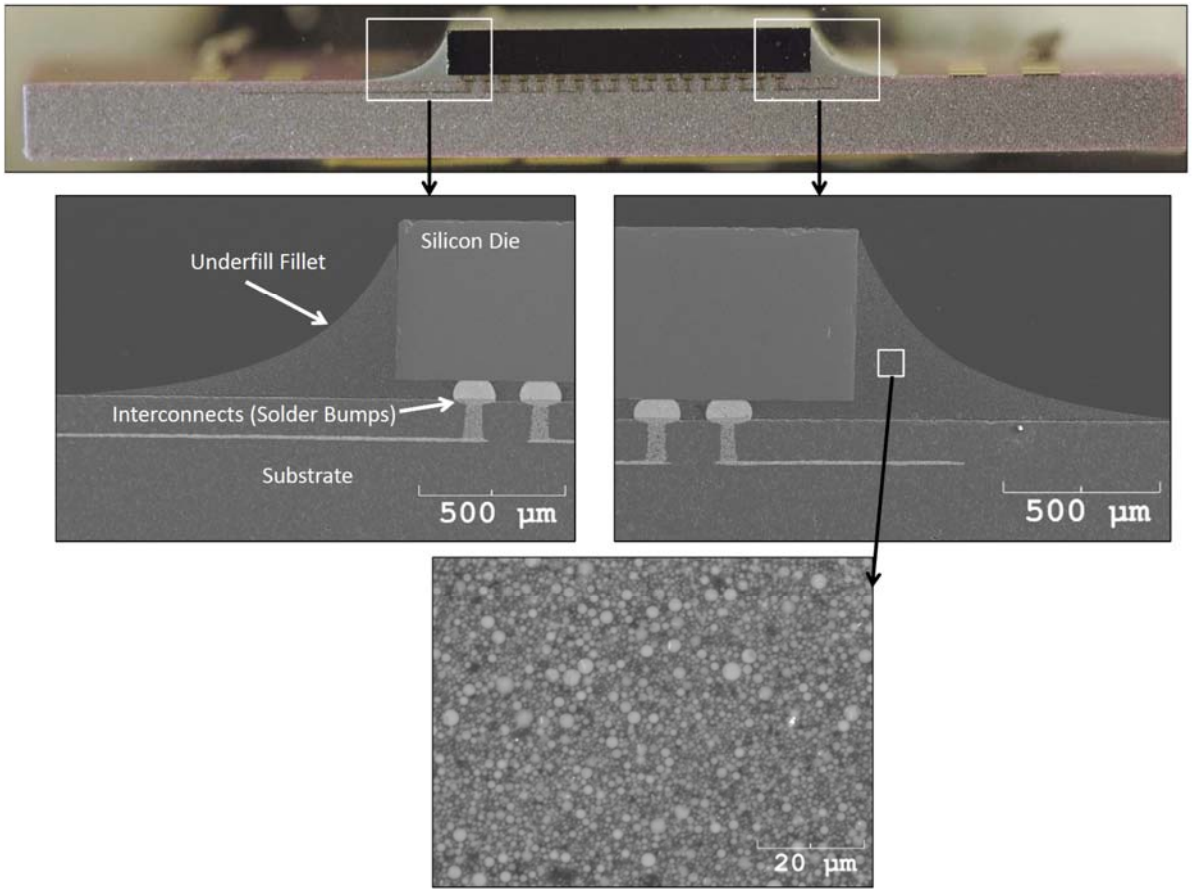
Special Issue

Flip-Chip Underfills

This is a special edition of the NASA *EEE Parts Bulletin* that brings awareness of the issues currently being worked as part of the new technologies for space applications, in this case, flip-chip underfills. The following articles were written by NASA specialists. The first introduces the subject matter, and the second describes the results of evaluations conducted for the NASA Electronic Parts and Packaging (NEPP) program. Also included is a third article noting the parallel effort by the Defense Logistics Agency (DLA) to elicit input from the manufacturing and user communities regarding development of test requirements for flip-chip underfills.



Cross section of a flip-chip die (top) with underfill fillet keyed to two diagrams (middle) showing the location and general arrangement of underfill around the chip components. Right diagram shows relationship to enlarged view of fillet (bottom) at 20 µm. (Photographs and micrographs were generated by R. Ruiz.)

Flip-Chip Underfill for Space Applications

The electronics industry is constantly increasing functionality whereas the space electronics industry has a need for increased reliability/increased mission life in addition to the increased functionality.

One approach to increasing the functionality has been to increase the input/output (I/O) connections. Higher I/O counts were achieved by transitioning from wire-bonded die to flip-chip die with increased functionality. In flip-chip dies, the active area is faced downward and faces the substrate where it is mounted by solder interconnects. The use of flip-chip interconnects has a history of more than 40 years in commercial industry.

A major concern with flip-chip technology is thermo-mechanical fatigue reliability due to stresses on the interconnects (such as controlled collapse chip connection [C4] and solder balls). Stresses arise due to coefficient of thermal expansion (CTE) mismatch between the semiconductor die (silicon 3–4 ppm/degC) and substrate (5–10 ppm/degC for ceramics and 18–20 ppm/degC for polyimide or FR4 (glass-reinforced epoxy). As the distance from the center of die increases, the magnitude of stresses increases at the interconnects accordingly. To relieve these stresses on interconnects, underfill materials were developed. The use of underfills has been shown to increase the reliability of the package by several orders of magnitude in commercial electronics.

Although this technology has not yet been used extensively in space, it is expected that this reliability increase will result in increased mission lifetimes. There is a need to understand the effect of underfill materials in increasing the reliability of electronic parts in space applications.

Underfill materials are adhesives that are introduced between the flip-chip die and the substrate (Figure 1). Underfill materials are configured to match the CTE of interconnect and distribute the stresses on interconnect solder joints. A balance of key material properties such as CTE, glass transition temperature (Tg), elastic modulus, moisture absorption, and shrinkage after cure, based on the package design is required to achieve a highly reliable package.

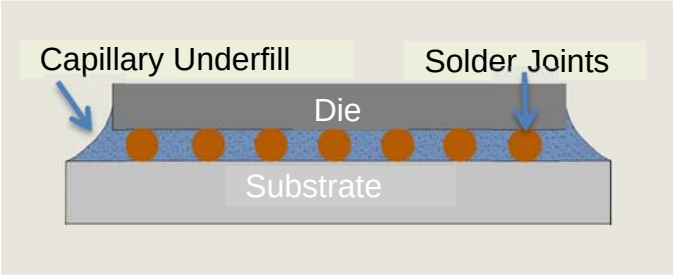


Figure 1. Diagram showing a schematic representation of underfill between the die and the substrate. (The diagram was generated by Daniel Lamadrid.)

Underfill adhesives have been categorized as dispensable liquid and dry-film based. Underfills are applied essentially by three methods.

1. Capillary underfilll is applied after the flip-chip die is mounted onto the substrate, the underfill is dispensed on the die side wall, and it flows under the die due to capillary action.
2. Pre-applied liquid underfill is dispensed on the substrate first, and then the die is placed. Due to the pressure from the die the underfill spreads and covers the area under the die.
3. Dry film underfill is laminated under temperature and pressure onto the silicon wafer or the substrate.

Liquid underfills have been used for commercial industry for the past 20 years. Pre-applied liquid underfill and dry film underfill are being evaluated in the industry as options for three-dimensional (3D) chip stacking.

In addition to these two methods, there are several other techniques being evaluated in the industry, such as vacuum-assisted underfill, for applications wherein the die is large or the gap between die and substrate is minimal. However, they are only in the research stage at this point.

The scope of this study is to evaluate the feasibility, reliability, and concerns in using underfills. Some of these underfill concerns can be categorized into material issues, process issues, and reliability issues.

Material issues: Material properties that need to be consistent from lot to lot include, viscosity, Tg, CTE, modulus, filler distribution, resin and filler loading levels, and filler size variation. Changes in these material properties can affect the flow properties and curing properties affecting the process and reliability of the product. Along with these are other important properties such as material aging at extreme temperatures.

Process issues: Voiding under the chip is a key process issue with capillary underfills. During the assembly process, underfill is dispensed on the side walls of the die, and capillary forces drive the underfill to the other side of the die to fill the area under the die. Due to the flow of underfill, if the flow front is not uniform, underfill could flow faster in some areas, thus capturing voids, termed as capture voids. Controlling these voids is essential for reliability because the presence of voiding could cause solder shorting during the subsequent reflow and surface mount process. Other process issues include dispensing issues, machine issues (e.g., dispense-pump clogging or machine temperature drift), thawing and storage life control, life in the processing machine (time and temperature), and limited ambient storage. Incorrect cure time, temperature, and moisture control can also result in voiding.

Reliability issues: Poor adhesion of underfill to the die and substrate could cause delamination or cracking. The modulus of underfill must be configured based on the dielectric being used in the die active area, which could be

stress sensitive. A key essential reliability issue is delamination of underfill if the coverage of underfill on the die side walls (termed as fillet) is not optimal. Fillet height and shape are key variables that can affect the component reliability. Another property is underfill shrinkage after cure, which can affect the adhesion of underfill to the die, substrate, and solder interconnects.

Filler separation has also been known to cause reliability issues. Filler separation occurs when there are filler-rich regions and resin-rich regions after the material cures. This would cause a CTE difference with lower CTE in the filler-rich regions and higher CTE in resin-rich regions potentially causing reliability issues.

Space applications: Capillary underfills have been used in the commercial industry for decades, and several of the issues related to material, process, and reliability have been well documented. However, the space environment presents a different challenge in qualifying these materials for use to enhance long term reliability of electronics. There arises a need to qualify these underfill materials to space environments such as wider operating temperature ranges, temperature cycling, and endurance to shock and vibration during launch and landing. A well-controlled study needs to be conducted to establish specifications and guidelines for material properties, process tolerances, and reliability. Sensitivity to the Jovian radiation belts is yet to be addressed.

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Class-Y Related Studies on the Reliabilities of Flip-chip Underfill

MIL-PRF-38535 defines Class Y as: "A microcircuit employing a ceramic non-hermetic package, which meets all applicable requirements of this specification …". All of the candidates for Class Y identified to date have employed flip chip and underfill construction. The underfill material has drawn increased attention upon the release of class-Y parts, since the underfill materials of Class-Y parts are exposed to the external environment. For commercial applications, an underfilled flip-chip package does not always require hermetic packaging. One of the reasons is because the underfill is considered to provide sufficient environmental protection to the solder bumps by encapsulating them, though the main function of underfill is to reduce the amount of stress on the solder bumps. Before the invention of the underfill, flip-chip packages were often hermetically sealed to improve the reliability by minimizing interaction between the environment and the solder bumps. Although underfill was considered to provide environmental protection to the solder bumps, the concern with Class-Y parts is that the underfill was not protected from the environment.

There were concerns that the exposure of the underfill to the space environment would cause underfill degradation and ultimately lead to decreased package reliability. To address these concerns, NASA, under the NEPP program, has investigated the effect of low Earth orbit (LEO) environment and humidity on underfill properties. Prior to conducting the actual experiments, the potential risks of various constituents of the LEO environment were assessed. Since electronics within a spacecraft are exposed to less harsh conditions than outside of the spacecraft, the long-term vacuum exposure was rated as the most realistic environmental concern for the underfill material among all the negative constituents of the LEO environment. A raw underfill material used in an actual class-Y product was procured and exposed to long term vacuum, heat, oxygen plasma, and humidity. The underfill did not show any signs of degradation after the long term vacuum and heat exposure; instead, it showed signs of improvement. Conversely, humidity exposure resulted in decreased adhesive strength and lowered glass transition temperature of the underfill. The oxygen plasma exposure, conducted to simulate the exposure to the atomic oxygen environment, did not result in generation of any potential contaminants.

Since an underfill material exhibited property changes after the exposure to various environments, the impact of the underfill property change on the package reliability was of interest; NASA has collaborated with a part manufacturer and procured the manufacturer's research and development (R&D) samples to study this issue. The samples were underfilled daisy-chained flip-chip dies assembled on ceramic substrates. The samples were pre-conditioned and temperature cycled. The pre-conditioning conditions included vacuum thermal aging, humidity exposure, multiple reflow, and current stressing.

After temperature cycling, all the samples failed by an underfill breakdown mechanism, regardless of the pre-conditioning condition. A crack initiated at the longest fillet of the underfill and propagated to the flip chip solder bumps, causing the solder bump failure. This result was in agreement with the conventional wisdom among flip-chip engineers that flip-chip solder bumps generally do not fail before the underfill is compromised. After the current stressing, half of the flip-chip bumps suffered a minimum of 20% drop in the joint shear strength. However, the temperature cycling life of the current stressed samples did not exhibit changes, which indicates that underfill plays a far greater role than the flip chip solder joint strength in temperature cycling life of flip chip packages. The vacuum thermal aged and multiple reflowed samples exhibited 50% increase in temperature cycling life, while the humidity exposed samples showed a 30% decrease.

The strong correlation between the results of the two different studies, the study with the raw underfill material and the study with industry R&D samples, suggests that underfills' capability to withstand degradation by

environmental exposure plays an important role in the Class-Y parts' flip-chip interconnect reliability. The underfill materials used in the two studies were different materials, and it is likely that many other underfill materials would exhibit similar behavior when subjected to environmental exposures. Results of the two studies also indicated that the exposure to the LEO environment poses low risk to underfills in non-hermetic Class-Y parts, while exposure to humidity prior to the launch at the ground must be minimized. For underfills in Class-V parts, the environmental exposure is not of a concern, due to the parts' hermeticity.

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Defense Logistics Agency Engineering Practice Study on Flip-Chip Underfill Test Requirements

On July 13, 2015 the Defense Logistics Agency (DLA) released an initial draft of *Engineering Practice (EP) Study for Flip Chip Underfill Test Requirements to TM 5011 and MIL-PRF-38535* (EP study project number 5962-2015-004).

Because underfill is new, there are no references to it in the present requirements documents. Underfill-related material is needed for the requirements because it is a major new direction for complex package technologies such as flip chips.

The current draft of the EP study may be accessed at http://www.landandmaritime.dla.mil/programs/milspec/ListDocs.aspx?BasicDoc=5962EPStudies

The EP study summarized the new technology of underfills and requested inputs from the military services, microcircuit manufacturers, package assembly houses, and user communities regarding possible underfill evaluation/testing requirements.

The goal of the EP study process is to develop a consensus of underfill requirements that can be proposed for incorporation in either or both of

- Test Method 5011 (TM 5011) (Evaluation and acceptance procedures for polymeric materials) of MIL-STD-883, *Test Method Standard, Microcircuits*.
- The "Package Integrity Demonstration Test Plan" (PIDTP) of MIL-PRF-38535 (*Integrated Circuits (Microcircuits) Manufacturing, General Specification for*).

It is expected that the EP study will be concluded by the end of September. Those with comments regarding the EP study should contact Muhammad Akbar, DLA Land and Maritime-VAC, Post Office Box 3990, Columbus, OH 43218, or by facsimile 614-692-6939, or by e-mail to: Muhammad.akbar@dla.mil

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JEDEC/SSTC G-11 & G-12 meeting, Columbus, OH, Sept. 28–Oct. 1, 2015

Japanese Aerospace Research and Development (JAXA) 28th Microelectronics Workshop (MEWS), Tsukuba, Japan, Oct. 21–22, 2015

JEDEC/SSTC G-11 & G-12 meeting, Jacksonville, FL, Jan. 11–14, 2016

ESA/ESTEC European Space Components Conference (ESCCON), Noordwijk, the Netherlands, March 1–3, 2016

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