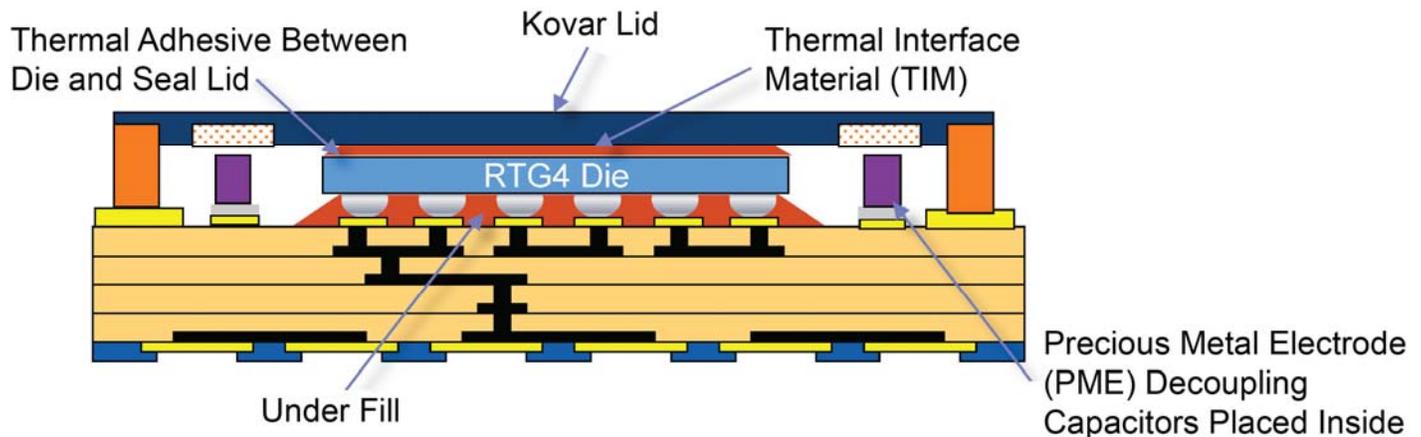




August–December, 2015 • Volume 7 • Issue 3 (Published since 2009)

This edition of the NASA *EEE Parts Bulletin* provides updates of the issues currently being worked. As part of the new technologies, Figure 1 shows a general view of how flip chips, underfills, and thermal interface materials (TIMs) fit together. The first of the following articles describes the newly released “thin” specification. The second is a proposal for standardized flows for CubeSats and SmallSats. The third article lists new space part developments in fiscal year 2015. The fourth article describes the interim underfill requirement generated by Defense Logistics Agency (DLA), and there is a cautionary note about “ELDRS-free”.



**Figure 1. Illustration showing a next-generation field-programmable gate array (FPGA) product from Microsemi that uses underfill. The diagram is the cross-section, showing flip-chip construction with underfill, TIM), and signal integrity capacitors of precious metal electrode (PME) design. (Image courtesy of Microsemi SoC Products)**

### **Status of Thin Dielectric Multilayer Ceramic Capacitors and Additional Slash Sheets for Interdigitated Capacitors (IDCs)**

MIL-PRF-THIN has been released by DLA Land and Maritime (Defense and Logistics Agency). The assigned specification number is MIL-PRF-32535. The specification covers thin dielectric multilayer ceramic capacitors manufactured with precious metal electrodes (PMEs) as well as those with base metal electrodes (BMEs). Ten initial slash sheets ranging from case sizes of 0201 to 2220, as well as reverse configurations of case sizes 0306 and 0508, have been released and are listed in Table 1. Figure 2 shows a typical IDC. Please see the DLA website at <http://www.landandmaritime.dla.mil/programs/qmlqpl/>

and use Assist-Quick Search for all available part numbers. Manufacturers have begun testing in order to qualify for the MIL-PRF-32535 Qualified Product List (QPL).

Three additional draft slash sheets for the interdigitated capacitors were sent to DLA Land and Maritime. DLA expects the draft documents to be uploaded to their website to solicit feedback from the community. MIL-PRF-38535, Paragraph 3.15.1, will be updated to include parts supported by MIL-PRF-32535. The NASA and Aerospace community will continue meeting to discuss the exceptions within the draft slash sheets.

These kinds of capacitors are finding usage in new technology microcircuit products slated for flight use.

**Table 1. MIL-PRF-32535 Case Sizes by Slash Sheet**

MIL-PRF-32535 Slash Sheet	Case Size
/1	0201
/2	0402
/3	0603
/4	0805
/5	1206
/6	1210
/7	1812
/8	2220
/9	0306
/10	0508
/11 (Draft under industry review)	0306 (IDC)
/12 (Draft under industry review)	0508 (low profile IDC)
/13 (Draft under industry review)	0508 (IDC)



Figure 2. Photographic image of a typical IDC placed on a dime between the E and the D in “ONE DIME.” (The image was generated by JPL Analysis and Test Laboratory.)

For more information, contact  
**Penelope Spence 818-354-2246**

**Working toward Standardized Flows for NASA CubeSats and SmallSats**

There are many new NASA flight missions categorized as CubeSats and SmallSats. During the weekly NEPAG telecons, the group has discussed what kind of standard products would fit those applications, including commercial-off-the-shelf (COTS) plastic encapsulated microcir-

cuits (PEMs). NASA is supporting SAE SSTCG12 committee activities with the goal of developing PEM standard flows for avionics and space applications.

At least three parts manufacturers have recognized the need for this newly developing market and are offering customized parts. Cobham Aeroflex has several flows assigned based on extent of testing to assist users in picking the best parts. Similarly, Texas Instruments offers parts in five different versions, including their QML offerings. Linear Technology plans to offer PEM products with guaranteed total dose radiation (rad tolerant, RT) ratings. Also, there is an existing QML N flow for standard non-space PEM devices.

These are all good developments. However, it would be cumbersome to manage multiple nonstandard flows. Moreover, some of these approaches may or may not apply to NASA missions depending on acceptable risk levels. The ideal situation would be for the space community and manufacturers to agree on a limited number of standard QML PEM flows (Figure 3) to offer solutions for CubeSats, SmallSats, and other similar applications. This needs to be discussed.

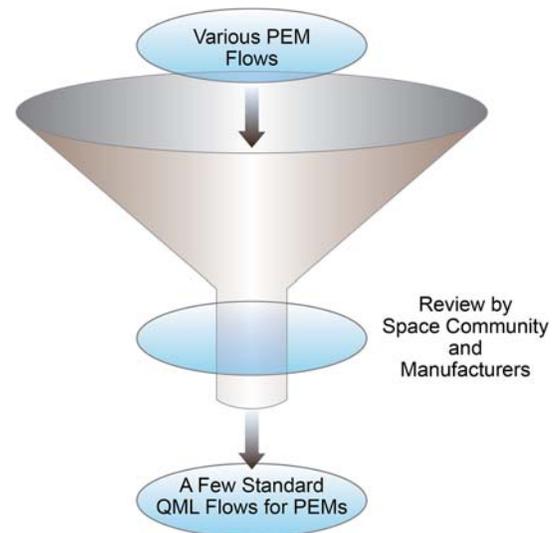


Figure 3. The proposed goal of standardizing on a few well-defined flows rather than multiple flows defined by each manufacturer or by each standards group.

For more information, contact  
**Shri Agarwal 818-354-5598**

**New Standard Space Microcircuits for Potential Use on Flight Projects**

NASA is in the review and approval cycle of new space monolithic (Class V) and hybrid (Class K) microcircuits. Many of these products are guaranteed to be radiation

hardened to the levels specified in the Standard Microcircuit Drawings (SMDs). Table 2 lists the space product SMDs approved in FY2015. Radiation-hardened parts are denoted by an asterisk. The microcircuit manufacturers have reported strong demand for space products. So much so that the number of new space products to be introduced in 2016 is projected to be much higher than the number released in 2015. This will provide more options to the designers of NASA flight hardware.

**Table 2. FY2015 Released SMDs.**

SMD No.	Function	Manufacturer
5962-08224	RTAX FPGA	Microsemi SoC
*5962-09B01	ASIC	Honeywell
*5962-12214	DC/DC Converter	Crane
*5962-13205	High-Speed ECL Buffer	ADI
*5962-13245	Op Amp	ADI
5962-13249	Dual Switch	IR
*5962-14B01	Standard Cell	Cobham Colorado Springs
*5962-14201	Voltage Regulator	Cobham Plainview
*5962-14202	Voltage Regulator	Cobham Plainview
*5962-14206	Op Amp	ADI
5962-14207	Op Amp	ADI
*5962-14227	14-bit 125-Msps A/D	ADI
*5962-14233	Op Amp	ADI
5962-15201	DC/DC Converter	IR
5962-15208	DC/DC Converter	VPT
5962-15209	DC/DC Converter	VPT
5962-15221	10-bit 3 Gsps SiGe D/A	E2V
5962-15230	DC/DC Converter	VPT

**For more information, contact**

**Shri Agarwal 818-354-5598**

### **Update on Flip-Chip Underfill Requirement for Space Products**

The subject of underfill was introduced in the previous Issue 2 of this bulletin. Underfill is a liquid encapsulating material, usually epoxy resins filled with silicon dioxide (SiO<sub>2</sub>) that is applied between the chip and the substrate.

<sup>1</sup> The JEDEC Solid State Technology Association, formerly known as the Joint Electron Device Engineering Council (JEDEC)

The thermal interface materials (TIMs) are similar to adhesives, but TIMs are used in flip chip devices as lid attachment materials.

There is now an interim requirement for using underfill and thermal interface materials (TIM) evaluation and acceptance criteria for flip-chip devices. This interim requirement was needed for moving forward underfill and TIM qualification for flip-chip devices.

The September 30, 2015, meeting of the 13.2 (JC-13.2 JEDEC Government Liaison subcommittee JC-13.2 Microelectronic Devices) subcommittee of the JEDEC<sup>1</sup> agreed to the interim solution.

Flip-chip manufacturers are required to document their “underfill evaluation and acceptance criteria” and their “TIM evaluation and acceptance criteria” in the package integrity demonstration test plan (PIDTP), which is a part of the product quality management (QM) plan for review and approval by the qualifying activity (QA) per MIL-PRF-38535, Rev. K. For aerospace applications this is the Defense Logistics Agency, NASA, and the Aerospace Corporation (supporting the Air Force). The QA will approve the interim solution PIDTP plans until the Task Group JC-13.2 (Subcommittee on Microelectronic Devices) completes its work, and the TM5011 requirements are finalized.

These underfill and TIM requirements would form the basis of all space (QML V and Y) flip-chip products for flight use.

Those with comments or questions regarding the interim requirement and the EP study should contact Muhammad Akbar, DLA Land and Maritime-VAC, Post Office Box 3990, Columbus, OH 43218, or by facsimile 614-692-6939, or by e-mail to: Muhammad.akbar@dla.mil

### **Caution Note about “ELDRS-Free”**

Enhanced low-dose-rate sensitivity is a radiation-induced phenomenon where the device shows increased degradation at a given cumulative dose when the irradiation is performed at lower dose rates than the traditional accelerated ground test rates (50-300 rad/s). The term “ELDRS-free” has been used in many datasheets but is considered a marketing term that has no real meaning. In essence, a part may show ELDRS degradation yet stay within the specified datasheet parameters to the tested dose level. One other concern is that the MIL-STD-883 Test Method 1019.9 for ELDRS calls for a low dose rate of 10 mrad/s. Typical space applications are lower than this, and commensurate increased parametric degradation may occur.

Consult your radiation specialist for more details.

## NASA Parts Specialists Recent Support for DLA Land and Maritime Audits:

Audits performed at

- Analog Devices Inc., Wilmington, MA
- AVX Corp., Fountain Inn, SC
- Coast Advanced Chip Magnetics, Torrance, CA
- Cobham-Metelics (formerly Aeroflex), Lawrence, MA
- Deutsch Relay, Incorporated, Hauppauge, NY
- Episil Technologies, Inc., Hsinchu, Taiwan
- Frequency Management, Huntington Beach, CA
- Gardien Services, Boulder, CO
- International Rectifier, Temecula, CA
- ISU Petasys Corporation, Sylmar, CA
- Jazz Semiconductor, Newport Beach, CA
- Kemet Electronics Corp., Simpsonville, SC
- Kyocera America, San Diego, CA
- Presidio Components, San Diego, CA
- Streamline Circuits, Santa Clara, CA
- Texas Instruments DMOS 6, Dallas, TX
- Texas Instruments, Malacca, Malaysia
- Texas Instruments, Sherman, TX
- Unicircuit, Incorporated, Littleton, CO
- VPT – Delta Incorporated, Blacksburg, VA

### Upcoming Meetings

JEDEC/SSTC G-11 & G-12 meeting, Jacksonville, FL, Jan. 11–14, 2016

ESA/ESTEC European Space Components Conference (ESCCON), Noordwijk, the Netherlands, March 1–3, 2016

Components for Military & Space Electronics Conference & Exhibition (CMSE 2016), Los Angeles, CA

Space Parts Working Group (SPWG), Los Angeles, CA, April 19–20, 2016

JEDEC/SSTC G-11 & G-12 meeting, New Orleans, LA, June 6–10, 2016

Electronics Technology Workshop (ETW), Greenbelt, MD, June 13–16, 2016

JEDEC/SSTC G-11 & G-12 meeting, Columbus, Ohio, Sept. 26–29, 2016

### Contacts

#### NEPAG (within JPL)

<http://atpo.jpl.nasa.gov/nepag/index.html>

Shri Agarwal 818-354-5598  
Shri.g.agarwal@jpl.nasa.gov

Roger Carlson 818-354-2295  
Roger.v.carlson@jpl.nasa.gov

---

#### ATPO <http://atpo.jpl.nasa.gov>

Doug Sheldon 818-393-5113  
Douglas.J.Sheldon@jpl.nasa.gov

---

#### JPL Electronic Parts <http://parts.jpl.nasa.gov>

Rob Menke 818-393-7780  
Robert.j.menke@jpl.nasa.gov

---

#### Previous Issues:

**Other NASA centers:** <http://nepp.nasa.gov/index.cfm/12753>

#### Public Link (best with Internet Explorer):

<http://trs-new.jpl.nasa.gov/dspace/handle/2014/41402>

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

---

[www.nasa.gov](http://www.nasa.gov)

National Aeronautics and Space Administration

**Jet Propulsion Laboratory**

California Institute of Technology  
Pasadena, California

© 2016 California Institute of Technology.  
Government sponsorship acknowledged.