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Special Edition on Electrostatic Discharge (ESD)
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Note: This revision adds a number of details and corrects ambiguities in the original issue that was released August 31, 2016 (the K. LaBel article on partnering and the back-page material were not changed).

Damage from ESD (see Figure 1) is a major cost to the microcircuit industry in terms of time, money, and mission risk. We plan to release two issues. This first special issue deals with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This issue also includes an article about partnering in radiation and reliability testing. The second special issue to be provided at a later date will give more details and examples of ESD-related problems.

(a) **(b)**

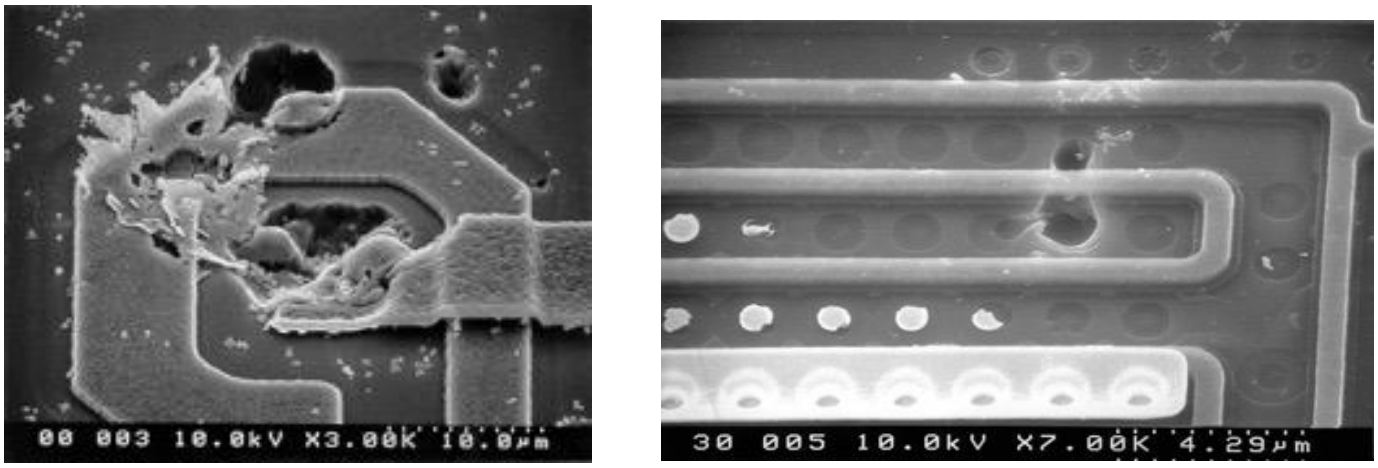

Figure 1. Examples of ESD damage to microcircuits (Images courtesy of JPL Analysis and Test Laboratory):
a) A static random access memory (SRAM) device with 5-micron features was deliberately exposed to an 8000-volt pulse from a 100-picofarad capacitor. This produced an approximately 5.3-ampere peak current pulse lasting just under one microsecond. Melting of conductive traces is typical of such ESD damage and creates an open circuit path.
b) An undefined microcircuit with 1-micron line widths that failed in service after being exposed to a pulse of approximately 500 volts. This caused a breakdown of the SiO_2 layer and a short circuit in the part.

Upgrading ESD Control: Its Importance and Possible Strategies

A. What Is ESD and How Are ESD Controls Applied?

Electrostatic discharge or ESD in electronic parts is an electrical sparking event that functions like a tiny version of lightning. When two objects with different potentials are brought sufficiently close, a current flows toward the ground equalizing the potential. These differences can be caused by friction of dissimilar materials (shoes on a carpet is a classic example), but even the difference in potential between a human body and an object may be enough to initiate an ESD event.

For electronic parts, built to carry minute amounts of current, tiny lightning bolts are a cause for concern. If such an errant current flow of an ESD goes along the outer case of a part or the outside of an ESD-resistant (anti-

static) bag or shipper, there may be no problem. However, if such a current goes through the part, serious damage may result. ESD damage can include catastrophic damage and/or latent damage. Catastrophic damage is immediately detectable by the resulting loss of function and often visible damage. Latent damage is not immediately detectable because there is no loss of function and often no visible sign of damage. However, the part has been weakened and may fail in the field or (worse) in space.

This has always been a serious concern for electronic parts, but it has grown steadily more urgent.

The purpose of this article is to sensitize the entire space community, and in particular, the standards-developing-bodies to the fact that the ESD requirements must be clearly specified in such standards documents so that everybody handling microcircuits, from manufacture to final use can minimize ESD damage. Furthermore, the standards must be updated to reflect the present level of technology.

In this context, the role of DLA (Defense Logistics Agency) for the department of defense (DoD) becomes vital. The standardization branch of DLA develops and maintains the military (MIL) standards, which are used for maintaining high-reliability quality parts production for the DoD and for NASA. Also, manufacturers and non-MIL standards organizations provide inputs to the standards

These standards are often enforced by periodic audits of parts manufacturers and their supply chains. The audit branch of DLA officially conducts enforcement. NASA actively supports DLA in both of these activities.

For the purposes of this article, we are focusing on monolithic microcircuits. The standard most commonly used by the U.S. space community for high-reliability microcircuits is MIL-PRF-38535*, Integrated Circuits (Microcircuits) Manufacturing, General Specification for*. Any microcircuit parts produced under the military system must be in compliance with the requirements of this document.

The 38535 is the periodically changing overall document controlling microcircuit quality and reliability. The ESD aspects of the document clearly need updating. For auditing, the requirements must be flowed down to the working audit, and it must be reflected in each manufacturer's quality management (QM) plan.

In addition, the ESD-related standards used by other organizations may provide ideas for upgrades to the MIL standards. Conversely, it would be highly beneficial if the MIL standard upgrades could be coordinated with those of the other standards bodies so that practices throughout the industry might be as similar and interchangeable as possible.

B. Why Improved ESD Control Practices Are Crucial

Designers have improved microcircuit performance in two ways, smaller size to allow more circuits per unit area (parts densification) and higher operating speeds. (See *ESD Technology Roadmap*, for more detail on these trends [1]).

Moore's Law has continued with microcircuit densification down to less than 50 nm for many components and some components at 20 nm and less. That and advancements in packaging technologies have resulted higher pin counts to accommodate highly complex microcircuits (e.g., system on a chip).

In the last decade, pin counts have increased particularly for communication and computing products. NASA and the space community are using 1752-pin counts, and higher counts are growing more common in the general market.

Furthermore, some applications use not just smaller parts but parts that need to operate at speeds of 1, 10, even 30 gigabits per second (Gbps).

The improved performance attained by increasing parts density and higher speeds has come at the cost of greater sensitivity to ESD. Thus, it becomes increasingly important to implement better methods of controlling potential damage from ESD. A wide assortment of books and journal papers provides information on methods for mitigating ESD.

A related issue is that current ESD rating methods were developed with typical pin counts in the twenties. Applying these old device testing standards to modern high-pin count products can cause severe problems. Testing times increase dramatically. Worse, wear caused by repeatedly stressing the same path and the increasing influence of tester parasitic losses (parasitics) can lead to false-positive failures.

For high-reliability microcircuits (where a part may cost as much as tens of thousands of dollars), organizations often develop and enforce required policies and procedures designed to mitigate ESD. These policies and procedures are codified in standards.

Furthermore, the landscape of microcircuit part production, handling, and shipping has changed radically. Because of the increased complexity of parts, the paradigm of a manufacturer shipping directly to a customer has largely given way to a highly dispersed production environment, which in turn, often requires highly dispersed ESD control among a number of organizations. Table 1 shows all the steps at which production or use of a microcircuit might be done by shipping to another facility. (The most extreme cases of maximum dispersion are more likely with new products such as flip chips.) Moreover, each of the steps involves at least one environment each for working on the part, storing the part, and shipping the part to the next step in the production.

Table 1. An Extreme Example of possible dispersion of production for a microcircuit product.

Company	Operation/Use
Component Level	
A	Die design
B	Wafer fabrication
C	Wafer bumping
D	Package Design
E	Assembly
F	Column attach
G	Testing and screening
H	Radiation testing
I	Transport by a franchised distributor
J	User Inventory Operations
K	Kitting of upper-level assembly operations
Board Level and Above	
L	Board-level test and verification
M	Intermediate board-level assembly
N	Final box-level assembly
O	Placement of the box level assembly containing the part in a system (e.g., aircraft, spacecraft, or appliance)

Note: At board level and above (L–O), reduced ESD failures can be realized through upper-level design mitigation (usually electromagnetic interference (EMI) compliance and spacecraft charging mitigation) and also box-level handling processes. System level handling processes can also reduce occurrences (for example, shorting plugs and connector covers) for the integration and test phase of the electronics system.

Increasing the number of shipping steps in the supply chain increases the number of points where ESD damage may occur. All this needs to be quantified.

It is important to recognize and fully address all the risk points to which ESD sensitive parts are subjected: from when they are fabricated and delivered from the original component manufacturer's (OCM) site; through supply chain avenues to user inventories; then on to kitting and upper-level printed circuit board (PCB) level assembly, test and verification; and eventually to final box level assembly, test and final system level test. This is particularly important for handling, packaging, and shipping of ESD Class 0A devices (<125 volts in the Human Body Model). (See ANSI/ESDA/JEDEC JS-001-2014, *ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level*, listed in subsection D)

C. Questions Related to Upgrading ESD Control Requirements

This section of the article describes challenges of high pin-count ESD device testing, solutions, and possible future trends in the standardization of device testing.

Some issues to consider include:

- What are the differences and the advantages vs. disadvantages of the MIL standards, the JEDEC standards, the ANSI/ESD standards, and other standards for potential use and/or which might influence the MIL standards?
- Are all three commonly used ESD models still valid or should the standards focus on one or two models?: Those models are 1) human body model (HBM) based on people accumulating electric charges; 2) charged device model (CDM) based on materials becoming charged after they rub against other materials; 3) machine model (MM) [designed to simulate a machine discharging through a device to ground].
- Do we want a standard for reducing the number of pin combinations required for testing?
- Would statistical pin testing be a good approach?
- How can the testing time be reduced without losing useful information (and significantly impacting the test data)?
- Should the MIL standards be expanded to include charged device model (CDM) testing?
- How do the new 2.5D and 3D configurations affect ESD testing? (See Electrostatic Discharge (ESD) in 3D-IC Packages [2].

We need to consider future trends when revising test standards. This issue is growing more important because the unit costs of contemporary devices are very high (and are growing costlier as more functionality is added), on the order of several tens of thousands of dollars per unit. Poor ESD environment for such products creates possibility of damage/ latent damage to them, both of which could be very expensive. Costs for implementing an ESD-prevention program are miniscule compared to the overall cost incurred in dealing with ESD damage.

The above concerns were presented by NASA representative Michael Sampson at the June 2016 SAE SSTG-12 Space Subcommittee meeting. He proposed that the military documents that control the ESD requirements for testing and rating ESD event severity be reviewed and updated as a first step. As part of this update process, he suggested that the Defense Logistics Agency (DLA) Land

and Maritime, which serves as the qualifying authority to maintain the MIL system of parts qualification, perform an engineering practice (EP) study on ESD to detail these issues and compare possible specification changes with those being implemented or proposed by other organizations, in particular the NASA Inter-Agency Working Group related to ESD (NASA IAWG-ESD). Ideally, coordination among the various standards-setting organizations would result in updated ESD standards with a great deal of commonality. DLA shared the results of their EP study at the JEDEC meeting held in January 2017. Based on the EP study and responses to it, JEDEC (JC-13) has opened a task group to resolve issues related to ESD.

These document changes will require review and coordination with associated reference documents from other organizations to bring consistency.

D. Existing Standards That Contain ESD Control Requirements and Suggested Changes to Them

As noted earlier, the Department of Defense MIL system has an extensive set of ESD requirements and related documents. In addition, several other standards organizations have existing ESD-control requirements documents.

The listing below includes some of the most important ESD standards relevant to MIL devices.

MIL-STD-883, *Test Method Standard, Microcircuits*, Rev. K, U.S. Department of Defense, April 25, 2016

- Test Method 3015, "Electrostatic Discharge Sensitivity [ESDS] Classification"

https://landandmaritimeapps.dla.mil/Programs/MilSpec/ListDocs.aspx?BasicDoc=MIL-STD-883

MIL-STD-883 includes Test Method 3015 (TM 3015), "Electrostatic Discharge Sensitivity Classification," which establishes the procedure for classifying microcircuits according to their susceptibility to damage or degradation by exposure to ESD. This test method utilizes what is called the human body model (HBM) and it was developed many years ago.

Unfortunately, MIL-STD-883/TM 3015 has not kept pace with the new technology developments. It needs to be revised for the new technology features, such as smaller size, greater numbers of pins, and advanced packaging mentioned earlier.

MIL-STD-1686, *Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)*, Rev. C, U.S. Department of Defense, Oct. 25, 1995.

The MIL-STD-1686 is the central MIL document that relates to ESD-related material in other documents, such as test methods. Because this document is widely referenced, it needs to be updated because it has not been revised since 1995.

SEMI E78-0309, *Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment*, Semi International Standards, July 2008.

MIL-PRF-38535, *Integrated Circuits (Microcircuits) Manufacturing, General Specification for*, U.S. Department of Defense, Dec. 20, 2013,

https://landandmaritimeapps.dla.mil/Programs/MilSpec/ListDocs.aspx?BasicDoc=MIL-PRF-38535

Paragraph A.4.4.2.8, Electrostatic Discharge Sensitivity, states that, "ESD classification shall be done in accordance with TM 3015 of MIL-STD-883 (the testing procedure defined within JESD22-A114 may be used as an alternate with acceptable correlation data) …" (See discussion below under E, Correlation.)

MIL-PRF-38535 has no specific ESD requirements for wafer foundries. However, Test Method (TM) 3015 of MIL-STD-883K and SEMI E-78-0309 constitute ESD classification methods to specify the sensitivity level for appropriate packaging/handling requirements and wafer manufacturing equipment. The entire section does not relate to laboratory practices, but it is important to note that they are a critical component of electronics needing ESD control, and perhaps a new ESD standard for the aerospace and defense community should address that. Suppliers on their own take precautions but there is nothing in the specification to audit to. For example, the ESD properties of foups (boxes used to carry wafers during processing) may degrade over time.

JESD22-A114F, *For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) - Component Level*, JEDEC Standard, JEDEC Solid State Technology Association, Arlington, VA. The JESD22-A114F has been superseded by the ANSI/ESDA/JEDEC JS-001 series of standards. However, some standards may still cross reference to this older standard.

ANSI/ESDA/JEDEC JS-001-2014, ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level, This is a revision to the JS-001-2010 document, which merged the JESD22-A114F and another ESD/ANSI standard. (Note: revisions are denoted by changes in the last four numbers of the document, as in 2010, 2011, and 2014.

ESDA/JEDEC JS-002 2014, Electrostatic Discharge *Sensitivity Testing - Charged Device Model (CDM) - Device Level*, August 29, 2014. This standard series is the CDM standard comparable to the JS-001 HBM series. It

is also revised by year as denoted in the last four digits of the name.

ANSI/ESD S20.20-2014, *Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices*, Electrostatic Discharge Association, 2014. S20.20 was prepared by the Electrostatic Discharge Association (ESDA). There are differences between MIL-STD-1686 and this document. Refer to the ESDA website for details.

NASA-STD-8739.7, *Electrostatic Discharge Control Excluding Electrically Initiated Explosive Devices)*. This document was cancelled in December 1997. However, resurrecting it is an option.

E. Correlation or Combining of ESD Documents

MIL-PRF-38535 directs that testing can be done by either MIL-STD-883/TM3015 or JESD22. However, the two documents have differences in their test methods.

- 883, TM3015 states that each device shall be tested using three positive and three negative pulses using each of the pin combinations as shown in the table II in the document. A minimum of 1 second delay shall separate the pulses.
- Whereas, JESD22 states that each sample shall be stressed using one positive and one negative pulse with a minimum of 300 milliseconds between pulses per pin for all pin combinations specified in table 2 of the document.

The community must consider whether these two test approaches provide the same results and identify necessary updates to the affected documents. A total review of the documents must be done to find and resolve any other differences.

Several major manufacturers have used other standards to perform tests not included in 38535, for example, using a charged device model (CDM) to characterize the ESD sensitivity level. (For more information about CDM, refer to Electrostatic Discharge Sensitivity Testing—Charged Device Model (CDM)—Component Level, ANSI/ESDA/JEDEC JS-002).

This is a growing issue. As the partial listing of standards in the previous subsection suggests, there has been a great deal of work accomplished in developing standards for ESD mitigation, but it has been done by multiple groups. Standards of the various groups have a number of small and major differences.

These different streams of standards development have caused waste through duplication of effort. Of more immediate concern is that suppliers and users who straddle more than one such group face greatly increased complexity of operations. This increased complexity can increase costs, increase potential supplier–user disputes, and increase the potential for parts failures due to ESD weaknesses in production.

Thus, there can be tremendous benefit by negotiating to achieve “harmonization” of standards. Harmonization can be done in some combination of three ways.

1. Different groups can combine multiple documents into a single document (e.g., combining of standards to generate JS-001-2010, now 2014),
2. Incorporate parallel changes in standards from different groups.
3. Reference a standard elsewhere as part of one’s own standard or contract (e.g., the military and space community often uses ANSI/ESD S20.20 regarding ESD).

F. Upscreening of Commercial-off-the-Shelf (COTS) and Other Parts

Performing ESDS testing when upscreening parts is not a common practice, but it should be considered by the users. At the June 2016 G12 meeting on plastic encapsulated microcircuits (PEMs), it was reported that manufacturers can lower ESD sensitivity ratings on COTS parts without any notice.

G. Conclusion

We have provided a brief introduction for two issues with ESD in microcircuits. First, the smaller part sizes of parts densification are making microcircuits much more sensitive to ESD. Meanwhile, the increased pin counts allowed by densification are increasing the complexity, risk, and time required for ESD testing on those parts. Consequently, methods for mitigating ESD must be correspondingly upgraded.

Second, there are multiple ESD mitigation standards that have been developed by different organizations. In turn, it is not clear which of these ESD standards are being used by each link in the microcircuit supply chain. This enormously confuses contracts and quality control among different organizations. It would be extremely useful to coordinate the ESD standards to make the requirements as similar as possible and to have them specified in as few standards as possible and include them in MIL-PRF38535.

Third, NASA is in the process of resurrecting the old NASA-STD-8739.7 document on ESD control. This document will unify the Agency’s centers and field component centers and align industry partners with NASA to common control program elements. The resurrected standard will contain a minimal set of built-in quality controls, it will reference industry documents, it will be tailorable and concise, and it will ensure quality workmanship from the component level through system assembly.

References

[1] *Electrostatic Discharge (ESD) Technology Roadmap*, EOS/ESD Association, Inc., Revised May 2016/

[2] *Electrostatic Discharge (ESD) in 3D-IC Packages*, Global Semiconductor Alliance, Version 1.0, Jan. 14, 2015.

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Typical ESD Weaknesses and Suggested Control Improvements from Supplier Plant Visits

Controlling electrostatic discharge (ESD) is a key component for electronic parts assurance auditing to ANSI/ESD S20.20. In early 2016, two personnel from the NASA JPL (Minh Do and Jose Uribe) conducted an ESD survey at a typical microcircuit supplier to identify any ESD issues in the supplier's operations. Similar surveys at different locations have yielded comparable results.

We would like to share some of these typical results and findings with the NASA Electronic Parts Assurance Group (NEPAG) and the wider electronic parts community. These ESD surveys are usually a result of findings during an audit by the qualifying activity (QA) for MIL standard parts. (This function is performed for the U.S. Government by DLA, and NASA is also an active participant in this function.) Such facilities usually have an ESD program in place, but they can often benefit from equipment upgrades and procedure updates such as:

a) Employee training is critical; and everyone in the work area must be aware of his/her surroundings and be properly trained in the handling of ESD-sensitive (ESDS) devices. As a confirmation for auditors, the workplace employees shall be trained to the organization's ESD control plan (CP).

b) A calibrated ESD field meter is essential. Analog field meters should be replaced by the newer and more accurate chopper-stabilized digital field meters. Also the field meters should be calibrated at least annually.

c) Housekeeping is important in keeping potentially static-generating clutter (mainly packaging material) away from the ESDS area (also known as electrostatic discharge protected area). NASA requires that all static generating material or non-grounded personnel be at least 1 meter (39 inches) away from the ESDS area, in contrast to the ANSI/ESD S20.20, which calls out 1 foot (0.3 meter).

d) Older chairs may need replacement. They often have seating surfaces that do not meet the electrical resistance requirements, so the drag chains or conductive wheels do not work properly. Chairs that do not meet ANSI/ESD STM12.1 electrical resistance requirements should be replaced, particularly for ESD protected areas (EPAs) handling parts with sensitivities less than 125 V (Human Body Model, HBM).

e) Be sure that the metal racks used to store or to transport parts between work stations are properly grounded. Rubber or plastic gaskets between metal sections may insulate the sections and prevent grounding (see Figure 2). Exposed ESDS parts cannot make contact with metal surfaces directly; however, they can contact static dissipative materials.

Figure. 2. Photograph showing a plastic insulator inserted at each connector junction in a storage rack. Such rings prevent grounding of items stored on the rack. Lack of grounding could lead to build-up of a damaging electrostatic charge. (Figure courtesy of Steve Bolin.)

f) Resistance measurements often show the groundable points in a facility having different resistances (some as high as several megaohms). Ideally all groundable points should measure very low resistance (less than 0.1 ohm).

g) One of the best upgrades for ESD protection is to replace wrist strap testing with continuous wrist strap monitoring. When doing this, it is important to use a system having two wire wrist straps rather than the common single wire wrist straps. Single wire wrist straps do not allow for actual

monitoring of resistance to the operator but instead rely on measurement of impedance and can be fooled. Single-wire systems will, in fact, indicate safe grounding of the operator even when an insulating barrier such as a shirt is placed between the wrist strap and the operator's skin.

h) Also for grounding, workers must affix their wrist straps against their skin rather than over clothing. A wrist strap will fail to alarm if (for example) it is on the sleeve of a person's lab coat.

i) Belt furnaces or shuttle ovens are always difficult to properly ground due to the moving parts, and they are often found to be isolated from ground or "floating." Using an air ionizer of sufficient capacity near the furnaces will help in these cases.

j) Old cathode ray tube (CRT) monitors are still occasionally found on wire bonders. The CRTs produce very high voltage static fields. Such CRT monitors should be replaced with flat panel displays (which do not charge) or groundable CRTs. (Both of these types of equipment are commercially available). In the rare cases in which the CRT monitors cannot be replaced, they need to be removed from the ESD protected area or made safe by enclosing them in a perforated metal box and covering the screen with a groundable transparent shield, which shields the parts in the wire-bonding area from the CRT screen.

Reference

ESD Association Standard Test Method for the Protection of Electrostatic Discharge Susceptible Item, ANSI/ESD STM12.1-2013 – Electronic, https://www.esda.org/standards/factory/view/1581 (accessed Oct. 24, 2016).

American National Standards Institute(ANSI) Electrostatic Discharge (ESD) Association Standard for the Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices), ANSI/ESD S20.20.

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An Example of Partnering: the NASA Electronic Parts and Packaging (NEPP) Program and Naval Surface Warfare Center (NSWC) Crane

NEPP has a long history of partnering with many entities to foster new knowledge on radiation effects and reliability for new electronic devices and related technologies. While we have partnered with NSWC Crane for many years on many technologies, this collaboration has accelerated with the ascent of the SPECTRA research group within NSWC Crane's Flight Division.

While not the only joint NEPP-Navy Crane effort (there's work involving evaluation of automotive grade electronics, as well), this particular effort was seeded from two items:

- Previous radiation test collaboration on Intel/AMD microprocessors, and,
- The desire of NEPP management along with Crane scientists and engineers to think outside the box and expand collaborations for the good of the Military/Aerospace community.

Starting in fiscal year 2014, a few simple premises were put in place to expand the initial partnership:

- Identify devices/technologies of common interest,
- Coordinate obtainment of test samples,
- Develop radiation and reliability test/analyses matrixes from all parties,
- Perform identified tests (individually/jointly),
- Analyze and share data, and,
- Release as appropriate.

Currently, the collaboration is focused on three device/technology areas: advanced complementary metal-oxide semiconductor (CMOS) technology processors, non-volatile memories, and, expansion to field programmable gate arrays (FPGAs). All of these categories are of high interest to future military and space missions. An example of these efforts is the collaboration on Intel 14-nm CMOS processors.

This work started out as a "standard" task similar to those in the past: NASA brings a test set to Navy Crane's unique radiation exposure facility where we jointly irradiate samples and share the data. This had been done previously with four earlier CMOS technology node Intel parts. This time, however, it was decided to go further with multiple radiation test facilities/environments utilized to more thoroughly explore the radiation sensitivities of this advanced and new technology. In addition, SPECTRA made use of its extensive failure analysis capabilities in both standard (imaging/construction) and novel (simulation/exposure) ways to augment the suite of radiation environment testing. Using the unique and superior skills on both sides has led us to go well beyond

what we might have individually accomplished. Examples of this effort are seen in several references [1–3].

Figure 3 illustrates a sample of this test campaign performed at the Texas A&M University (TAMU) Cyclotron Facility. This test was for simulation of effects from the galactic cosmic ray (GCR) environment: highly energetic particles of danger to electronics in many space missions. Both NASA and Navy Crane team members participated in this test.

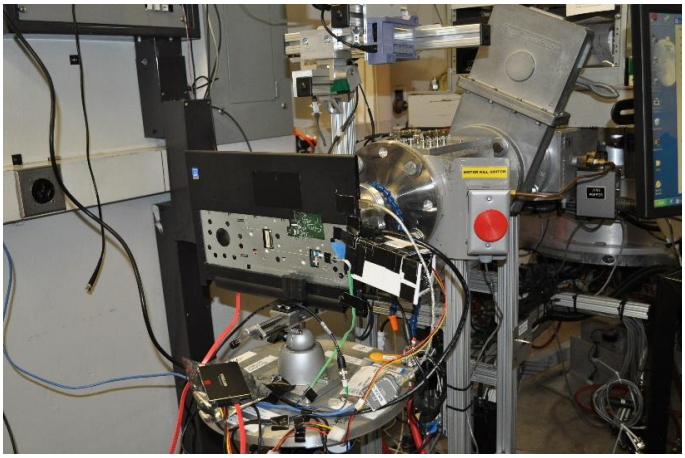

Figure. 3. Testing of Intel Broadwell Processor at TAMU.

Building upon the success of these joint efforts has both teams enthusiastically looking forward to further collaborations, and discussions are well underway to extend this teaming even further.

References

[1] C. Szabo, A. R. Duncan, K. A. LaBel, M. J. Kay, P. Bruner, M. Krzesniak, and L. Dong, "Preliminary Radiation Testing of a State-of-the-Art Commercial 14nm CMOS Processor / System-on-a-Chip," in *Proc. 2015 IEEE Radiation Effects Data Workshop*, July 2015, pp. 1–8.

[2] K. A. LaBel, R. A. Gigliuto, C. M. Szabo, M. A. Carts, M. J. Kay, T. Sinclair, M. J. Gadlage, A. R. Duncan, and J. D. Ingalls, "Hardness Assurance for Total Dose and Dose Rate Testing of a State-of-the-Art Off-Shore 32 nm CMOS Processor," in *Proc. 2013 IEEE Radiation Effects Data Workshop*, July 2013, pp. 1–6.

[3] A. R. Duncan, C. M. Szabo, D. P. Bossev, K. A. LaBel, A. M. Williams, M. J. Gadlage, J. D. Ingalls, C. H. Hedge, A. H. Roach, and M. J. Kay, "Single Event Effects in 14-nm Intel Microprocessors," Presented at *2016 IEEE Radiation Effects Data Workshop*, July 2016.

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NASA Parts Specialists Recent Support for DLA Land and Maritime Audits:

Audits performed at

- AEM Incorporated, San Diego, CA
- Amkor Technology – Taiwan, Hsinchu, Taiwan
- AVX Czech Republic s.r.o, Lanskroun Czech Republic
- AVX Ltd., Coleraine Irish Republic
- BAE Systems, Manassas, VA
- Carlisle Interconnect Technologies, Cerritos, CA
- Crane Electronics, Inc., Redmond, WA
- Dale Electronics, Inc., Columbus, NB
- Infineon Technologies Austria, Villach, Austria
- International Rectifier, Leominster, MA
- International Rectifier, San Jose, CA
- Linear Technology Corporation, Milpitas, CA
- MACOM (formerly Aeroflex Lawrence), Lowell, MA
- Microsemi Corporation, Lawrence, MA
- Micross Components – Crewe, Crewe, United Kingdom
- Sensitron Semiconductor, Deer Park, NY
- Six Sigma, Milpitas, CA
- Texas Instruments SVA, Santa Clara, CA
- UMC – Singapore, Singapore
- UMC, Tainan, Taiwan

Upcoming Meetings

- JEDEC/SSTC G-11 & G-12 meeting, Columbus, Ohio, Sept. 12–15, 2016
- JAXA Microelectronics Workshop, Tsukuba City, Japan, October 12–13, 2016

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