Abstract—We investigated the single-event effect (SEE) susceptibility of the Micron 16 nm NAND flash, and found that the single-event upset (SEU) cross section varied inversely with cumulative fluence. We attribute the effect to the variable upset sensitivities of the memory cells. Furthermore, the effect impacts only single cell upsets in general. The rate of multiple-bit upsets remained relatively constant with fluence. The current test standards and procedures assume that SEU follow a Poisson process and do not take into account the variability in the error rate with fluence. Therefore, traditional SEE testing techniques may underestimate the on-orbit event rate for a device with variable upset sensitivity.

Index Terms—Flash memories, heavy ion testing, single-event effect, standards, testing guidelines, testing techniques.

I. INTRODUCTION

NAND Flash memories are currently the dominant mass storage technology in the commercial market. State-of-the-art NAND flash devices are finding their way into many space systems thanks to the technology’s high density, low cost, and nonvolatile nature of storage [1]. The increasing popularity of commercial-off-the-shelf NAND flash devices in space applications has led to scrutiny over their radiation performance. NASA and other government agencies, as well as academia, have actively investigated the radiation susceptibility of each generation of NAND flash from various commercial vendors, from the first introduction of the technology [1]–[9]. The growing complexity of the control circuits as well as the continuously shrinking memory cell area have introduced new challenges for radiation testing.

Existing single-event effect (SEE) test standards include the JESD57, ASTM F1192, and ESCC No. 25100 [10]–[12]. These test standards provide top level guidance for single-event testing in general. NASA has recently published a more detailed test guideline targeted specifically at current nonvolatile memories [13]. However, the rapid advancements in nonvolatile memory technologies necessitate continued revisions and updates to existing test methods.

II. EXPERIMENTAL

A. Device Description

The MT29F128G08CBECHR6 is a 128 Gb single die multilevel cell (MLC) NAND flash memory built on Micron’s 16 nm CMOS process. The device is available in a plastic encapsulated ball grid array (BGA) package.

B. Test Facility

We carried out heavy ion irradiation at the Lawrence Berkeley National Laboratory (LBNL) Berkeley Accelerator Space Effects (BASE) Facility. The beam energy was 10 MeV/amu. Table I shows the characteristics of the utilized ions.

C. Test Setup

We used a custom-built printed circuit board with microcontroller and Flash BGA footprint as the test fixture. The microcontroller used for the test is an ARM Cortex-M4 (Freescale Kinetis MK20DX256VLH7) operating at 120 MHz. The microcontroller is directly connected to the I/O pins of the Flash memory under test.

For example, traditional single-event testing often use fluences ranging from $10^6$ to $10^7$ ions/cm$^2$ for a single exposure, consistent with recommendations in JESD57, ASTM F1192, and ESCC No. 25100. Those fluence levels provided sufficient statistical confidence for most integrated circuits in the past. However, the standards have not kept up with cutting edge technologies. The continued shrinking of feature size and increase in bit density for advanced memory and processor devices may warrant an increase in test fluence for adequate ion coverage of all the sensitive areas on a die, unless the architecture is repetitive and the radiation response of the transistors in the exposed region are representative of the entire device. With that said, existing test protocols are also predicated on the assumption that SEE probability remains constant with fluence. We explored the effects of variations in the test fluence, and observed an inverse dependence for the single-event upset (SEU) cross section. The cross section decreases as fluence increases, which we believe is due to the different upset probabilities for the memory cells.
TABLE I  

<table>
<thead>
<tr>
<th>Ion</th>
<th>LET (MeV·cm²/mg)</th>
<th>Range in Si (μm)</th>
<th>Energy (MeV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>0.9</td>
<td>306</td>
<td>108</td>
</tr>
<tr>
<td>Ne</td>
<td>3.5</td>
<td>175</td>
<td>216</td>
</tr>
<tr>
<td>Si</td>
<td>6.1</td>
<td>142</td>
<td>292</td>
</tr>
<tr>
<td>Ar</td>
<td>9.7</td>
<td>130</td>
<td>400</td>
</tr>
<tr>
<td>Cu</td>
<td>21.2</td>
<td>108</td>
<td>659</td>
</tr>
<tr>
<td>Xe</td>
<td>49.3</td>
<td>148</td>
<td>1232</td>
</tr>
</tbody>
</table>

memory was exposed to the heavy ions. The test data patterns included counter (data = address), 00, FF, AA and 55. The test modes included unpowered, static ON (standby), dynamic read, and dynamic erase/program/read/read. The supply voltages are 3.3 V for Vcc and Vccq. The test was carried out at ambient temperature. We irradiated two samples.

III. RESULTS

Figure 3 shows the SEU cross section as a function of effective LET for devices that were irradiated in the unpowered (static off) condition. The data points represent the average cross section for ion fluence ranging from $10^5$ to $10^7$ ions/cm². We irradiated the entire die, but read and/or programmed 2 blocks per run for the majority of the test. We found that testing 1 to 10 blocks produced fairly identical cross sections. Each block is 67 Mb, with approximately 4,000 to 5,000 intrinsic errors (∼ 0.05%). The intrinsic errors reflect the small noise margin between the logic levels. The proportion of the intrinsic errors remained constant throughout the heavy ion test, thus confirming negligible contribution from cumulative dose. The number of SEU for each run is obtained from subtracting the pre-irradiation errors (intrinsic errors) from the total post-irradiation errors.

Single-bit upsets (SBU) dominated the SEU response. We also observed single-event functional interrupt (SEFI) during static ON and dynamic tests, and two functional failures during dynamic read/write/erase tests. The functional failures were isolated to the block level. They occurred at tested LETs of 21.2 and 58.8 MeV·cm²/mg. No failure was observed for dynamic read or statically biased tests. In this paper we focus on the characteristics of upsets in the memory array.

A. Fluence Dependence

Figure 4 shows the cross section decreasing with increasing fluence for various LETs. We would point out that as the fluence decreases below $10^5$ ions/cm², the intrinsic errors begin to dominate the radiation-induced errors. For example,
irradiation with Ar to a fluence of $10^5$ ions/cm$^2$ produced approximately 350 SEU per block, which is approximately 15% of the pre-irradiation intrinsic errors. The proportion of SEU to intrinsic errors is 22% for irradiation with Xe to the same fluence of $10^5$ ions/cm$^2$. As a result, we did not investigate fluences less than $10^5$ ions/cm$^2$.

Figure 5 shows the cross section data at two fluences for each logic level. Figure 5 illustrates that each logic level has similar upset sensitivity, a characteristic that is consistent with Micron’s previous generation 25 nm MLC NAND flash [14]. The figure also shows that the fluence dependence is similar for each program level.

Heavy ion-induced cell upsets in floating-gate flash memory are susceptible to annealing at room temperature [15], [16]. Bagatin et al. showed the annealing characteristics of cell upsets after heavy ion irradiation for 70 nm and 90 nm floating-gate flash [15]. The devices in that study showed annealing of approximately 5% of the floating cell errors 1 hour following irradiation. In comparison, we observed reductions of 20% to 80% in the cross section from a fluence of $10^5$ to $10^7$ ions/cm$^2$, for different LETs. The irradiation exposure time typically varied from 1 to 10 minutes. The measurements were performed immediately after irradiation. We considered the possible influence of annealing during irradiation in our results, and examined the effects of different flux levels. For example, irradiation with Ar to a fluence of $5 \times 10^6$ ions/cm$^2$, at a flux of $6.4 \times 10^3$ ions/cm$^2$/sec. and $7.1 \times 10^4$ ions/cm$^2$/sec. for a duration of 783 and 70 seconds, respectively, produced an identical cross section of $2.6 \times 10^{-11}$ cm$^2$/bit. Alternatively, irradiation with similar flux and duration up to different fluence levels produced different cross sections. Figure 6 shows the number of errors from two blocks as a function of irradiation time, for irradiation with Ar at different fluence levels. The results in the figure demonstrate that the error count is not a function of irradiation time. The error counts are about the same for different exposure times at a given fluence. Therefore, the effects of annealing for cell upset are minimal across the tested range of fluence levels.
CHEN et al.: HEAVY ION IRRADIATION FLUENCE DEPENDENCE FOR SINGLE-EVENT UPSETS IN A NAND FLASH MEMORY

Fig. 8. Ratio of MBU cross section to SEU cross section as a function of the number of upset bits in a byte.

with LET. Additionally, the proportion of the number of upset bits per byte increases with LET. For example, there was no 5-bit or 6-bit upsets at a LET of 9.7 MeV-cm²/mg. 5-bit upsets appear for normal incident irradiation with Cu for LET of 21.2 MeV-cm²/mg. Then 6-bit upsets occur for normal incident irradiation with Xe for LET of 58.8 MeV-cm²/mg. Moreover, Figure 8 shows the effect of angular irradiation on the number of MBUs. Irradiation with Ar at 60° incident angle (solid square symbols) resulted in enhancement of the MBU to SEU ratio relative to irradiation with Cu at normal incidence (open diamond symbols), even though the two beam conditions have similar effective LET. Incident angle ion strikes produced more upset bits relative to normally incident ion strikes, since the ion track from an angular incident ion perturbs more cells.

Figure 9 shows the normalized cross section as a function of fluence for MBU and SBU, at a LET of 9.7 MeV-cm²/mg. The figure illustrates that the fluence effect is minimal for MBU. While there is approximately 60% reduction in the cross section from 10⁵ to 10⁷ ions/cm² for the SBU cross section, the reduction for the MBU cross section is only about 5%.

IV. DISCUSSION

The SEU cross section of a typical microelectronic device is generally assumed to be independent of the test fluence, based on the premise that the upsets follow Poisson process. So the first error should have no influence on the probability of an error occurring later in the irradiation. However, the flash memory cells exhibit a range of upset sensitivities, due to the variability in the threshold voltage distribution. It is likely that the variability in the upset sensitivities of the cells caused the different upset rates as a function of fluence.

The high density of the memory array leads to relatively poor coverage of the sensitive areas at typical test fluence levels. For example, fluences of 10⁵ to 10⁷ ions/cm² are equivalent to approximately 10⁵ to 10⁷ struck cells out of a total of 10¹¹ cells on a die for this device. Therefore, the pre-irradiation distributions will be different depending on the fluence level. Figure 10 schematically illustrates the cell population at different fluence levels. The solid curve represents the entire distribution for all of the memory cells. The dashed and dotted curves represent the pre-irradiation population of the stuck cells at fluence of 10⁵ ions/cm² and 10⁷ ions/cm², respectively. Figure 11 shows the post-irradiation distributions of the populations at the different fluence levels. The tails represent the putative shifts in the distributions after irradiation, based on studies of previous generation NAND flash devices [19], [20]. Heavy ion irradiation can cause 1) a secondary peak in the distribution, and 2) spreading out in the tail of the distribution. Heavy ion irradiation has negligible effect on the main population of cells with higher threshold voltages. The vulnerable cells
lie in the end of the population consisting of lower threshold voltages. Those relatively softer cells are more easily upset at low fluences. As the fluence increases, heavy ion irradiation exposes a larger sample of the population with higher threshold voltages that are less vulnerable to SEU. Therefore, the upset cells comprise a smaller percentage of the total number of exposed cells at a higher fluence than at a lower fluence. This is illustrated in figure 11. As the fluence increases from $10^5$ to $10^7$ ions/cm$^2$, the secondary peak also increases. However, the increase in the secondary peak is much less than the increase in the primary peak of the distribution, representing the exposed cells population. Consequently, the cross section decreases with increasing fluence. The upset probability decreases over time due to the infant mortality effect. The soft cells with lower threshold voltages represent the early failures with ion fluence, similar to the infant mortality population.

Furthermore, the fluence effect is more significant at lower LET, as shown in Figure 7. Irradiation with a higher LET ion causes the tail to spread out more than for a lower LET ion [19], [20]. So with a higher LET ion, we are able to upset a larger sample of the population with higher threshold voltages. The same population would not be affected by lower LET ions. As a result, the magnitude of the fluence dependence decreases for increasing LET.

The MBU characteristics further illuminate the phenomenon. We found that the upset probability of MBU remains relatively constant over fluence, while that of SBU decreases with fluence more significantly, as shown in Figure 8. The MBU upset threshold is typically higher than that for SBU. It would require a higher amount of deposited charge to cause threshold voltage shifts in multiple cells leading to a MBU. So the fluence effect is generally isolated to single cell upsets.

The phenomenon raises questions regarding current test standards and typical test methodologies with implications for hardness assurance. Traditional test methodology of irradiating to a fluence of $10^6$ to $10^7$ ions/cm$^2$ may underestimate the actual on-orbit event rate for such a device. The cumulative heavy ion fluence for most missions will be relatively low. So the on-orbit upset rate will be more accurately predicted by testing at lower fluence levels. Furthermore, the operating conditions of the flash in its application can influence the significance of this effect. If the application constantly writes to the flash and corrects the upset bits, then the memory is perpetually in a state similar to a fresh device, where the most vulnerable cells have not been depleted. In that case, testing to low fluence levels will more accurately predict the on-orbit rate. On the other hand, if the memory is rarely written to on-orbit, the errors will accumulate, and the upset rate will be higher at the start of a mission than at the end of a mission. So a space system carrying such a device can potentially experience a higher upset rate earlier in the mission than later in the mission. To account for this effect during SEE qualification of flash memory, we should systematically test at various fluence levels and correlate with the mission environment.

It is worthwhile to evaluate other flash memory technologies, because of the known variable distribution of cell upset sensitivities in flash. One constraint may be that as we continue to reduce the test fluence, the intrinsic errors will begin to overwhelm the radiation-induced errors. With that said, the enhancement in the upset rate from a fluence of $10^5$ to $10^7$ ions/cm$^2$ is not significant for this device. Also, the results showed that the effect on MBU is minimal. Therefore, a basic error correction algorithm can correct most of the SEUs in a typical mission. It may be worthwhile to evaluate the proton susceptibility, even though previous generation flash memories have not exhibited significant proton sensitivity. The cumulative proton fluence in LEO orbits is considerably higher than the heavy ion fluence, so that it would be meaningful to investigate the fluence dependence phenomenon for this technology. Additionally, it would be of interest for the space community to examine the impact of technology scaling for this effect.

V. CONCLUSION

We evaluated the SEE performance of Micron’s 16 nm NAND flash memory. We found that the SEU cross section varied inversely with fluence. We attribute the response to the variability of the cell upset sensitivities. So the cells near the low end of the distribution with lower threshold voltages will upset early on at relatively low fluence levels. As the fluence increases, a smaller proportion of the total cells will be upset, leading to a reduction in the cross section. The LET dependence of the fluence effect further provides evidence that a high LET ion is able to upset a larger portion of the cells, leading to a relatively smaller reduction in the cross section at a higher fluence. The LET dependence further showed the upset characteristics of different populations of the memory cells at different fluence levels.

The results shown here introduce a novel problem in radiation testing of a high density memory device with a
non-constant upset rate, which contradicts the traditional assumption that SEE follows a Poisson process. If the error rate is high enough that they cannot be corrected via error correction code, then this phenomenon will force us to reconsider the traditional approach for SEE testing of flash memories.

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REFERENCES


