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Evaluation of the Radiation Susceptibility of a 3D NAND Flash Memory

Dakai Chen[1], Edward Wilcox[2], Raymond Ladbury[3], Christina Seidleck[2], Hak Kim[2], Anthony Phan[2], and Kenneth LaBel[3]

1. Previously with NASA GSFC, Code 561, now with Analog Devices, Inc., Milpitas, CA 95035
2. ASRC Space and Defense, Inc., Seabrook, MD 20707
3. NASA GSFC, Code 561, Greenbelt, MD 20771

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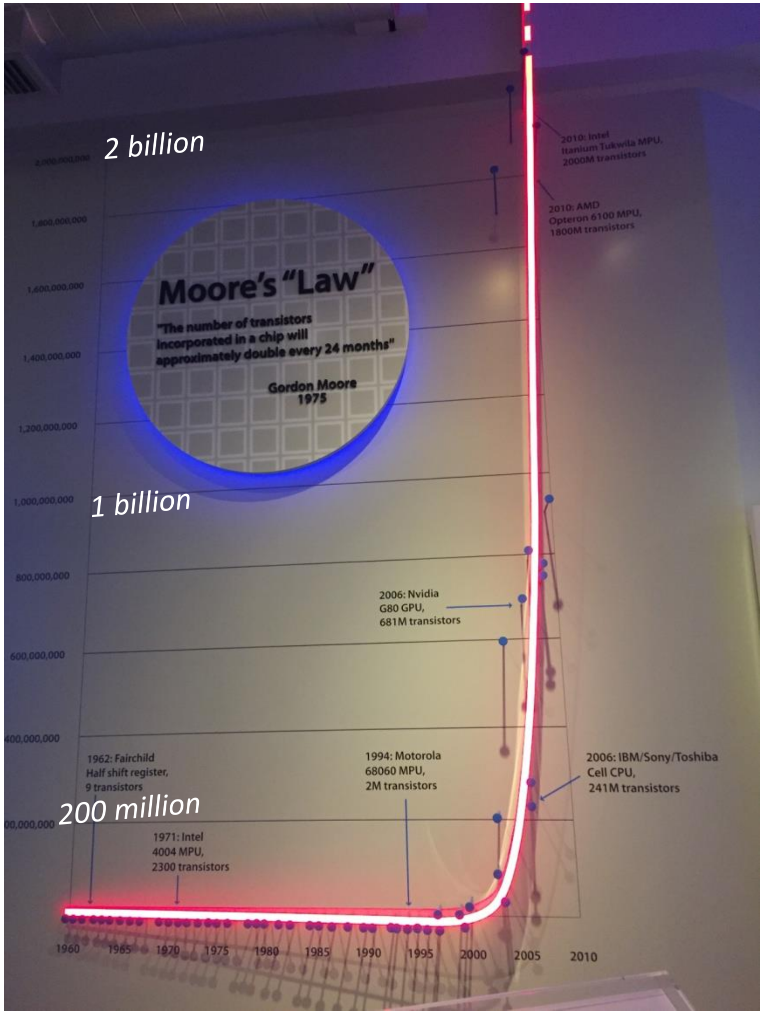
Acronyms

- three dimensional (3D)
- multiple-bit upset (MBU)
- Massachusetts General Hospital (MGH)
- multiple-level-cell (MLC)
- negated AND or NOT AND (NAND)
- single-event functional interrupt (SEFI)
- single-event upset (SEU)
- silicon (Si)
- single-level-cell (SLC)
- total ionizing dose (TID)

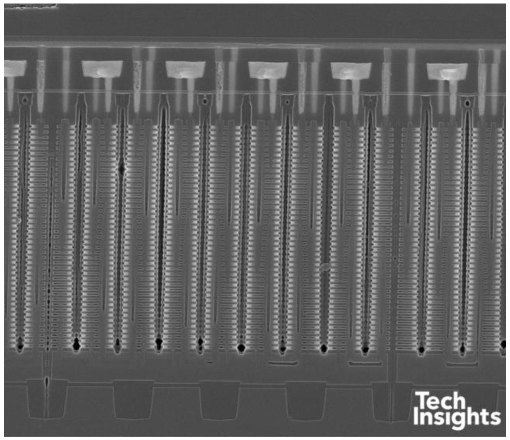
MOTIVATION

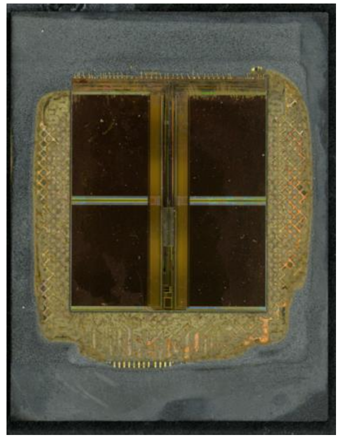


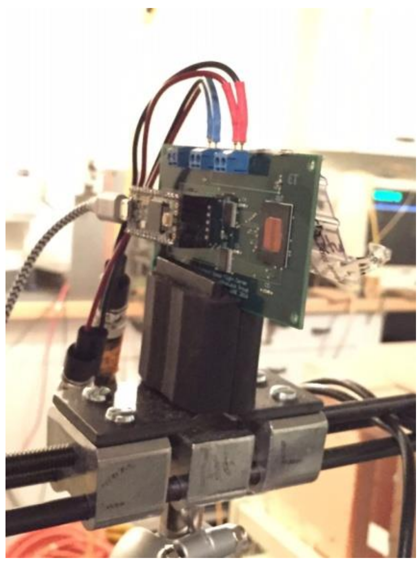
- Samsung introduced the V-NAND in 2013 as planar flash has reached design limits [1]
- In Q3 2017, 3D NAND flash will exceed 50% of total NAND market for the first time [2]
- Samsung, Toshiba, Micron, and China's new entrant Yangtze River Storage plan to release 64-layer, and Hynix developing a 72-layer 3D NAND flash late 2017 to early 2018
- NASA, ESA and other parties in the space industry have implemented state-of-the-art NAND flash into flight missions [3], [4]
- Impact on single-event upset (SEU) including multiple-bit upset (MBU) sensitivity? Other mechanisms?

1. Samsung Electronics, "Samsung 3bit V-NAND memory boasts higher density to enhance capacity" Samsung Electronics Co., Ltd, South Korea, August, 2015.
2. https://www.electronicsweekly.com/news/business/3d-nand-becomes-dominant-flash-memory-q3-2017-04/
3. T. R. Oldham et al., "TID and SEE response of advanced Samsung and Micron 4G NAND flash memories for the NASA MMS mission," *IEEE Radiation Effects Data Workshop,* pp. 114–122, Jul., 2009.
4. M. Fabiano and G. Furano, "NAND flash storage technology for mission-critical space applications," *IEEE Aerospace and Electronic Systems Magazine*, vol. 28, no. 9, pp. 30–36, Oct. 2013.

DEVICE AND EXPERIMENTAL



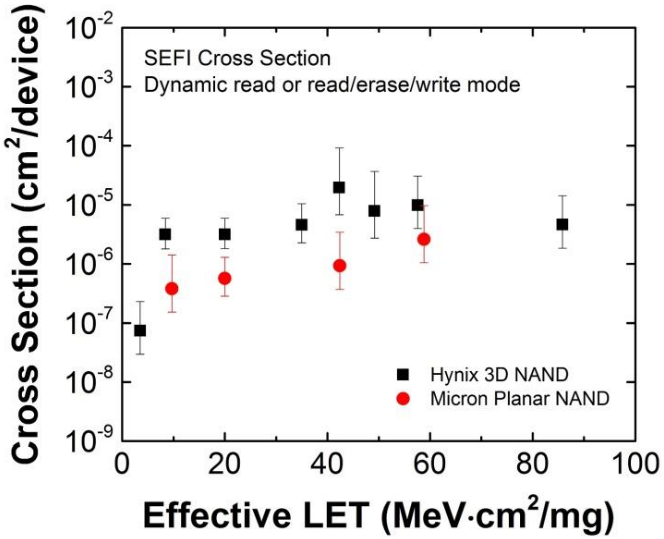


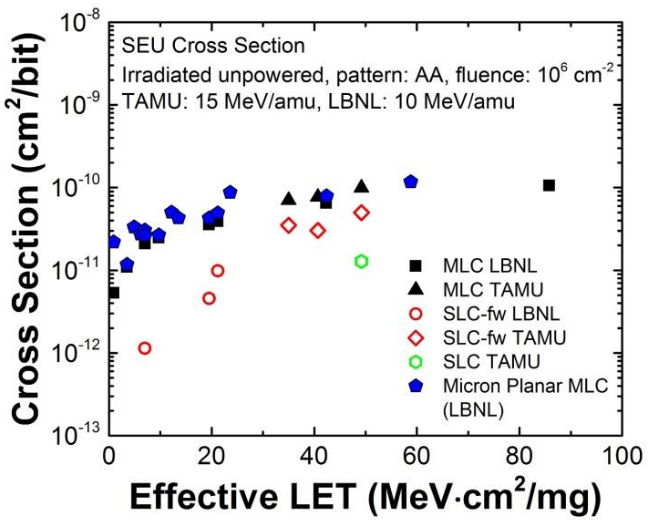


- Device under test
  - Hynix 128 Gb single die (40 nm) 3D NAND with gate-all-around charge-trap flash [1]
  - Micron 128 Gb single die (16 nm) planar NAND
- ARM Cortex-M4 Microcontroller and custom PCB mounted with flash
- Test Facility
  - Heavy ion testing at Lawrence Berkeley National Laboratory and Texas A&M University
  - High energy proton testing at Massachusetts General Hospital (MGH)
- Test modes
  - Static, dynamic read, dynamic read/read/erase/write
  - Patterns: All 0's, 1's (FF), checkerboard (AA and 55)

1. J. Choe. (2016). *SK Hynix in the Marketplace.* [Online]. Available: http://www2.techinsights.com/about-techinsights/articles/SK-hynix-3D-NAND-in-the-marketplace

SEFI AND SEU CROSS SECTIONS





- Single-event functional interrupt (SEFI) observed during static on and dynamic tests
  - Power cycle can recover in most cases
- SEU cross sections similar to the Micron planar NAND in multiple-level-cell (MLC) storage mode
- Single-level-cell (SLC) mode produced significantly lower SEU cross sections
  - Plain SLC mode showed the least SEU susceptibility

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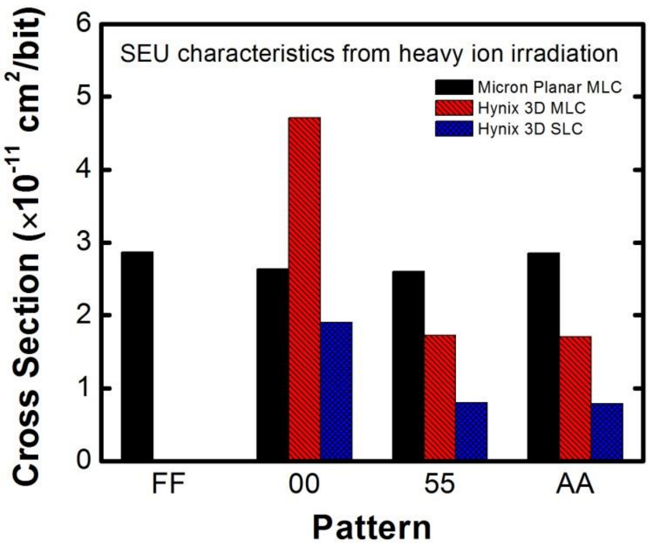
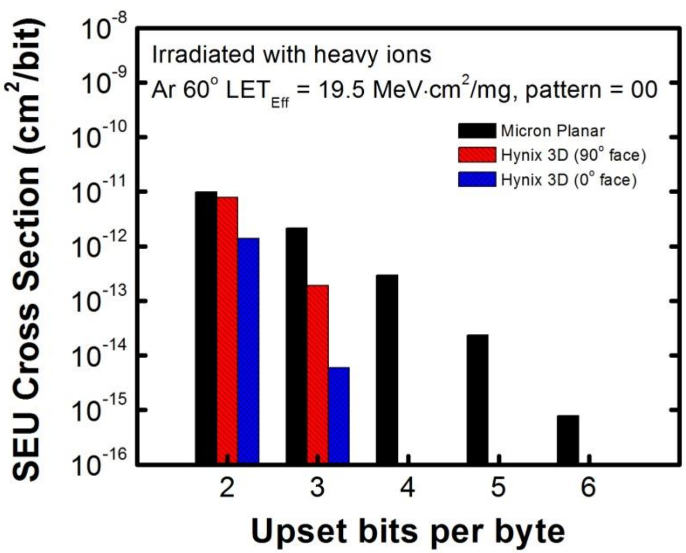
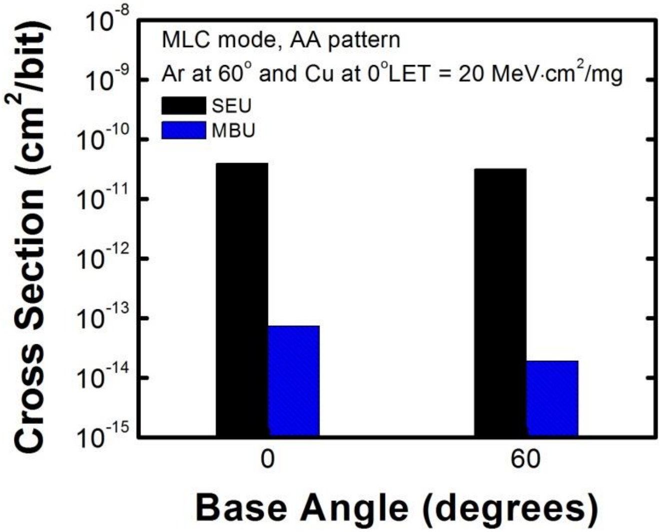
PATTERN DEPENDENCE

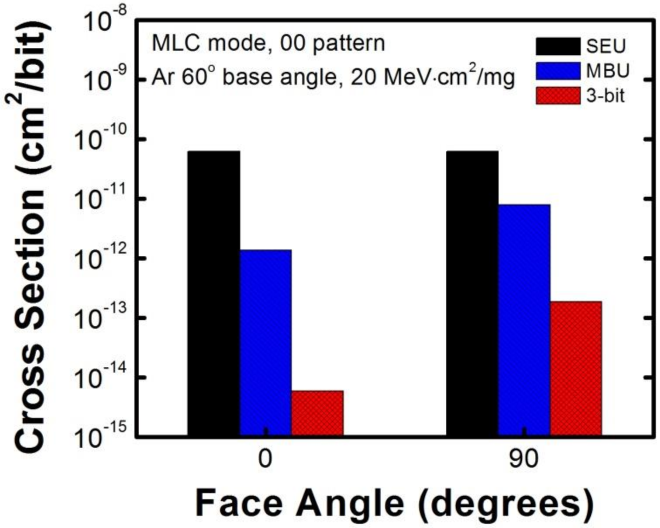


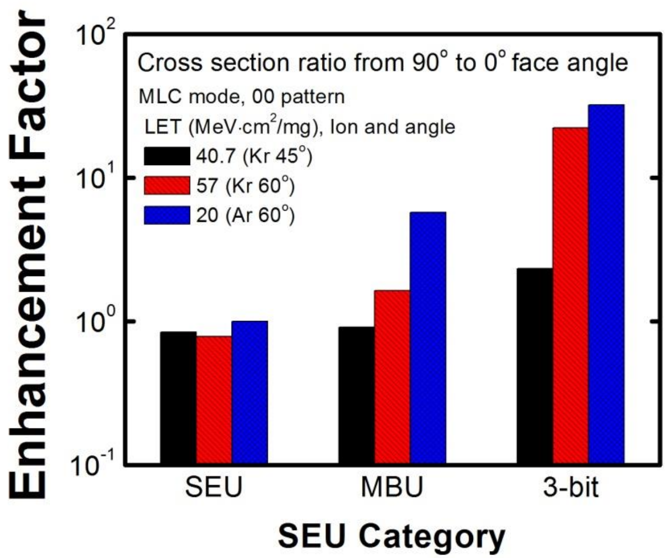


- Unique pattern dependence relative to the Micron planar NAND reflects different threshold voltage distribution schemes between the technologies
- Significant enhancement in SEU cross section for all 0's relative to checkerboard
- 3D NAND showed lower sensitivity to MBU relative to the planar NAND
  - Higher noise margin between program levels
- Enhanced MBU sensitivity at 90^o to 0^o face angle

ANGULAR EFFECTS

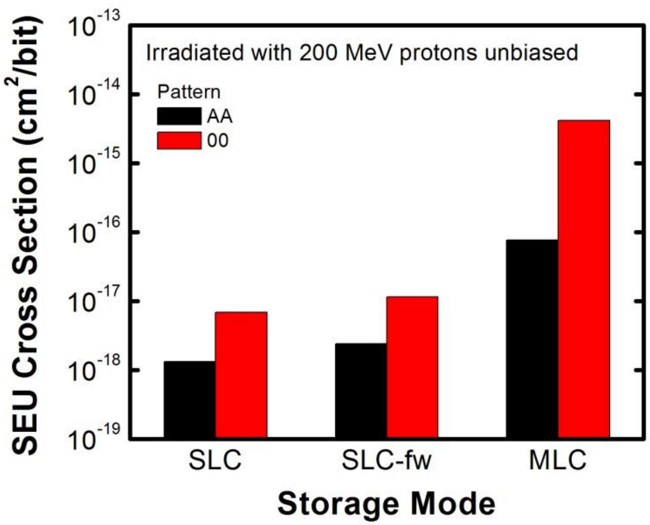


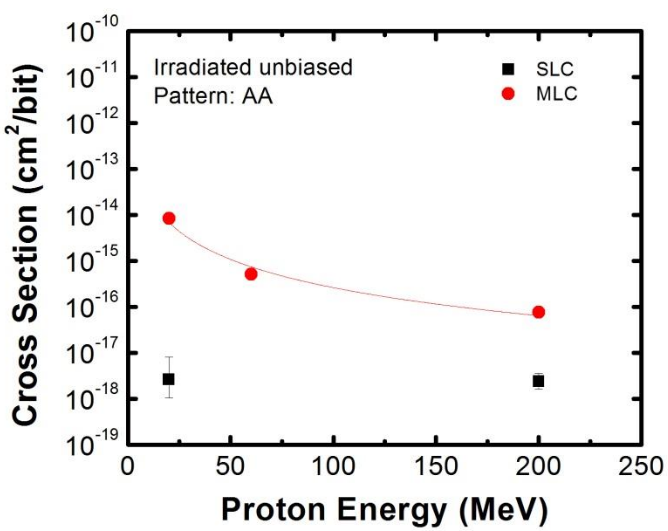




- Cross section decreased slightly from normal incidence to 60° base angle for the same LET
- MBU cross section showed enhancement from 0° to 90° face angle
- Enhancement from 90° to 0° face angle more significant with increasing number of upset bits per byte
- Enhancement from 90° to 0° face angle more significant for higher base angle (60° vs. 45°)

PROTON IRRADIATION

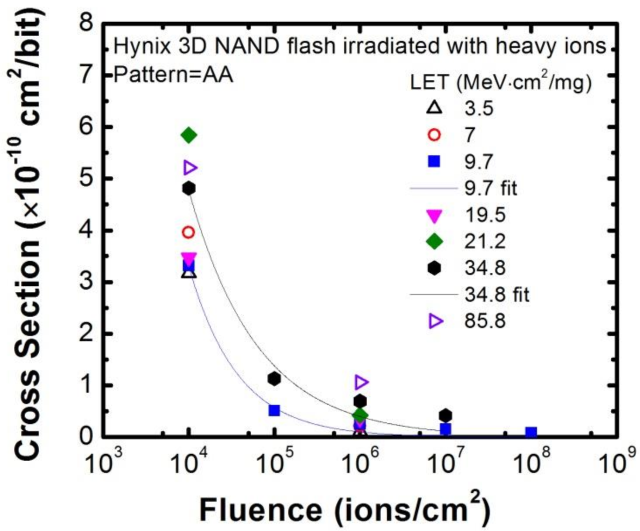


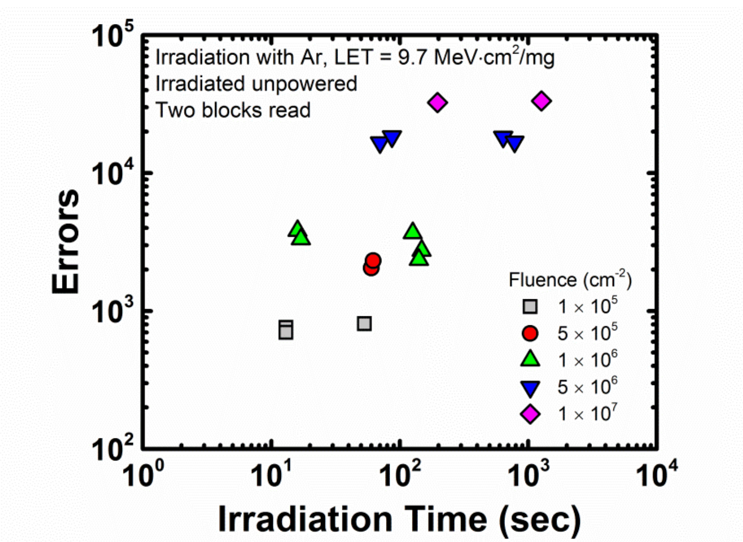


- SEU sensitivity to protons is significantly lower than heavy ions
- Similar pattern dependence and mode sensitivity
- Cross section increased for decreasing proton energy, similar to 41 nm Micron planar NAND flash [1]
  - Increase in the number of proton-induced secondaries with low LET
  - SEU LET threshold for MLC < 0.9 MeV·cm^2/mg, while for SLC is between 3.5 and 7 MeV·cm^2/mg

1. M. Bagatin et al., "Proton-induced upsets in SLC and MLC NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4130 – 4135, Dec. 2013.

FLUENCE DEPENDENCE

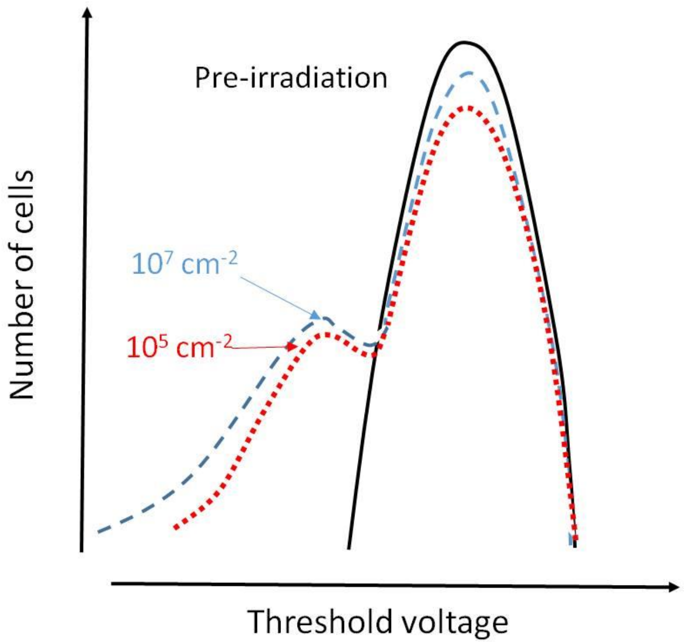




- Cross section decreased for increasing fluence, similar to that observed for the 128 Gb Micron planar flash [1]
- Influence of dose on SEUs?
  - 1 krad(Si) or less for each run
- Annealing of SEUs?
  - Annealing on orders of hours [2]
- Irradiation runs with different durations, but the same fluence, resulted in similar cross sections
- ***Annealing and TID had negligible impact***

1. D. Chen et al., "Heavy ion irradiation fluence dependence for single-event upsets in a NAND flash memory," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 332–337, Oct. 2016.
2. Bagatin et al., "Annealing of heavy-ion induced floating gate errors: LET and feature size dependence," *IEEE Trans. Nucl. Sci.*, vol. 57, No. 4, pp. 1835–1841, Aug. 2010.

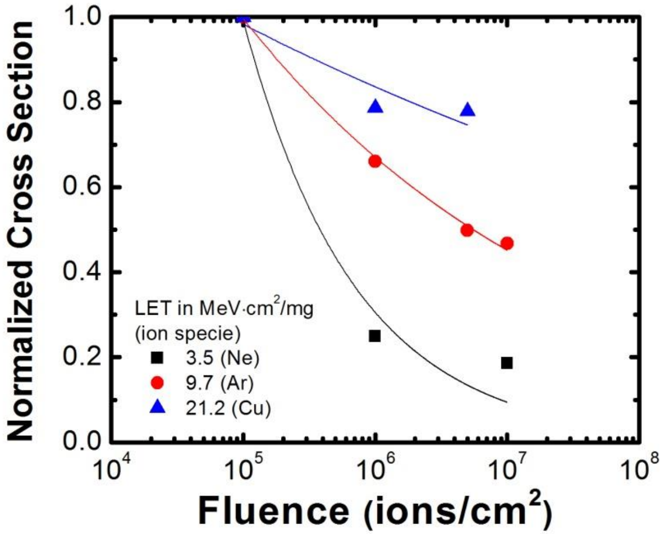
FLUENCE DEPENDENCE

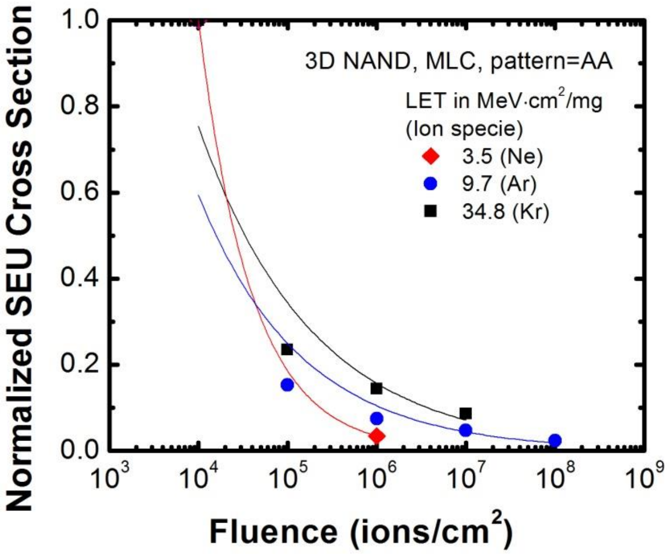


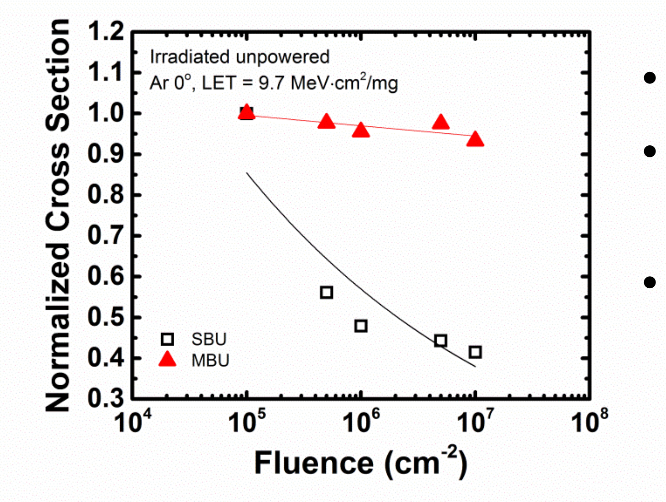
- Attribute to the variable threshold voltage distribution of high density NAND flash
- High density results in poor coverage at typical irradiation fluence levels
- Cells with lower threshold voltages will be vulnerable to upset, while the majority of the population with higher threshold voltages are not susceptible to SEU
- We increasingly encounter a proportionally higher population of robust cells at a higher fluence than at a lower fluence, leading to the decrease in cross section with increasing fluence

1. G. Cellere, et al., "Anomalous charge loss from floating-gate memory cells due to heavy ions irradiation," *IEEE Trans. Nucl. Sci.*, vol. 49, No. 6, pp. 3051–3058, Dec. 2002.
2. S. Gerardin, et al., "Heavy-ion induced threshold voltage tails in floating gate arrays," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3199–3205, Dec. 2010.

FLUENCE DEPENDENCE







- Fluence effect more significant for lower LET ions
- Higher LET ions can upset a larger population with higher threshold voltages
- Fluence effect much more significant for single-bit upset than for MBU

CONCLUSION

- The more relaxed noise margins of 3D NAND leads to benefits in the SEU performance relative to planar NAND of similar performance and density
- Lower MBU sensitivity with less upset bits per byte
- Evaluation of MBU susceptibility requires irradiation at base and face angle orientations
- SEU cross section varied inversely with fluence, indicative of a variable SEU rate during mission
- Relatively robust against proton-induced SEE, characteristic of response of traditional planar NAND