



Quad Flat No-Lead (QFN) Evaluation Testing

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
Pasadena, California

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California



Quad Flat No-Lead (QFN) Evaluation Testing

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Success

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
Pasadena, California

NASA WBS: 724297.40.43
JPL Project Number: 104593
Task Number: 40.49.02.35

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

<http://nepp.nasa.gov>

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

Copyright 2017. California Institute of Technology. Government sponsorship acknowledged.

Acknowledgments

The author would like to acknowledge many people from industry and the Jet Propulsion Laboratory (JPL) who were critical to the progress of this activity including the Rochester Institute of Technology (RIT). The author extends his appreciation to program managers of the National Aeronautics and Space Administration Electronics Parts and Packaging (NEPP) Program, including Michael Sampson, Ken LaBel, and Dr. Douglas Sheldon, for their continuous support and encouragement.

Table of Contents

1.	Objectives and Products.....	1
2.	QFN Packaging Technology	2
2.1	Introduction	2
2.2	Single Chip Packaging Trends and QFN	3
2.3	QFN Packages and Assembly	4
3.	QFN Assemblies and Reliability.....	7
3.1	As assembled build	7
3.2	Reliability under Thermal Aging Plus Thermal Shock (TS) Cycles (– 55°C /125°C)....	12
3.3	Failure Analysis	16
3.4	Reliability under TSC only (– 55/100°C)	17
4.	Conclusions.....	19
5.	Acronyms and Abbreviations	19
6.	References.....	21

1. Objectives and Products

Quad flat no-lead (QFN) packages are used in industry electronic hardware systems. Industry roadmaps projected wider use of these types of packages for high reliability applications, especially small satellites with radio frequency (RF) needs. This report presents a summary of literature surveyed followed by the reliability results of a number of QFN packages. It covers the test matrix approaches, the description of the packages, the board materials, and the surface finish, assembly approaches, and thermal cycle tests and failure analyses results.

Thermal cyclings were performed in the temperature ranges of -55°C to 125°C and -55°C to 100°C . X-ray, optical, and scanning electron microscope (SEM) images were presented for the as-assembled QFNs and after 1488 and 200 thermal shock cycles, respectively. Daisy-chain resistances changes were monitored per IPC 9701 at intervals for documenting failures. Additionally, failure or no-failure conditions, were performed by X-sectioning the representative QFN assemblies for solder joint condition. Failure analyses with optical images were also presented.

Key Words: quad flat no-lead, QFN, bottom termination component, BTC, MLF, IPC 7093, solder joint reliability, thermal cycle, thermal shock cycle, tin-lead solder

2. QFN PACKAGING TECHNOLOGY

2.1 Introduction

As with many advancements in the electronics industry, consumer electronics is driving the trends for electronic packaging technologies toward reducing size and increasing functionality. Microelectronics are meeting the technology needs for higher performance, reduced power consumption and size, and off-the-shelf availability. Due to the breadth of work being performed in the area of microelectronics packaging/components, this report limits its presentation to board design, manufacturing, and processing parameters on assembly reliability for leadless (e.g., quad flat no-lead (QFN) or a generic term of bottom termination component (BTC)) packages. This style of package was selected for investigation because of its significant growth, lower cost, and improved functionality, especially for use in an RF application.

The roadmap industry societies [1-3] present the status of microelectronics technology and industry needs. For example, the International Manufacturing Initiative (iNEMI) roadmap [1] shows component (package) trends—their decline and growth. Table 1-1 shows the component trends to smaller surface mount components and flip chip (versus wire bonded) using the relative growth rate of different single chip package types as baseline. It clearly shows that some single-chip packages, such as dual-in-line package (DiP) and wire-bond ball grid array (BGA), are projected to have negative growth while flip chip, direct chip attachment/wafer-level chip-scale packaging (DCA/WLCSP) and QFN components are projected to grow at a 15% compounded average annual growth rate (CAAGR).

Table 1-1. World Wide Semiconductor Package Volume (billions of units) (iNEMI [1]).

Package Style (Bn Units)	2010	2011	2016	CAAGR 2016/2011	% of IC 2016
DIP/SOT	5.3	4.3	3.9	-1.9%	1.4%
SO/TSOP/SOT	83.0	80.8	108.4	6.0%	37.8%
QFP/LCC	19.0	18.3	24.5	6.0%	8.6%
QFN	19.6	20.5	46.0	17.0%	16.1%
Wire Bond FBGA	8.0	8.2	12.6	8.9%	4.4%
Stacked FBGA	6.2	6.8	10.9	9.8%	3.8%
BOC	12.0	12.5	15.5	4.4%	5.4%
Wire Bond BGA	1.4	1.3	0.8	-7.9%	0.3%
COB (Wire Bond)	7.2	7.7	11.3	8.0%	3.9%
Flip Chip FBGA	0.8	1.6	8.1	39%	2.8%
Flip Chip BGA/PGA/LGA	1.1	1.1	1.6	7.1%	0.6%
DCA/WLCSP	12.9	14.5	29.2	15.0%	10.2%
COG/COF	8.6	9.2	13.7	8.3%	4.8%
Total Wire Bond	161.7	160.3	233.8	7.8%	81.6%
Total Flip Chip	23.4	26.4	52.6	14.8%	18.4%
IC TOTAL	185.1	186.7	286.4	8.9%	100%

The literature survey indicates the following:

- The BTC/QFN packaging size and I/O have significantly increased. Now, packages comparable to fine pitch BGA (FPBGA) are being evaluated.
- Significant design, process, and reliability data are available for conventional QFN components, but data are lacking for multi-row QFNs. Recently released specifications such as IPC 7093 [22], have helped to ease wider use of BTC/QFN packages.
- IPC 7093 [22] committee identifies two key issues in BTC: (1) providing the appropriate amount of solder paste and (2) ensuring solder-joint reliability is met.

- Reliability data is lacking; therefore, it is recommended to test evaluate BTC packaging technologies to characterize behavior for insertion in low-volume and high-reliability applications.

2.2 Single Chip Packaging Trends and QFN

Extensive work [4–10] has been carried out to understand the technology implementation of area array packages for high-reliability applications. Figure 2-1 categorizes single-chip microelectronic packaging technologies into three key technologies: (1) the early introduction wire-bonded plastic ball grid arrays (PBGAs) and quad flat no-lead (QFN); (2) advanced flip-chip BGA (FCBGA) and ceramic column grid arrays (CGAs); and (3) smaller foot print chip scale/wafer level (CSP/WLP), and leadless quad flat no lead (QFN), multi-row QFN, advanced QFN (aQFN); and land grid array (LGA) packages. There are numerous variations of packages. Only design, assembly, and reliability of conventional and advanced QFN packages are discussed in detail.

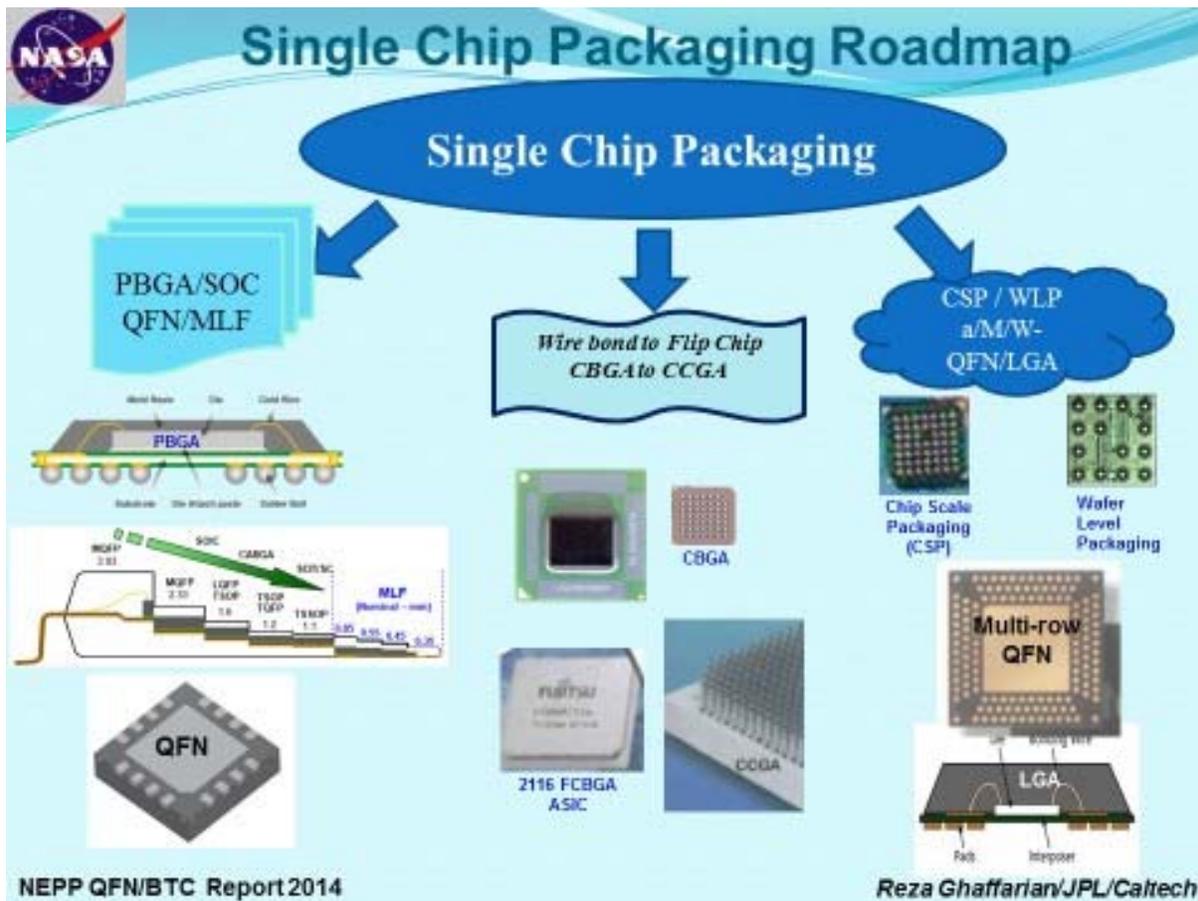


Figure 2-1. Microelectronic single-chip packaging technology trend, low and high I/O, coarse and fine pitch, and leaded and leadless configurations.

Leadless packages are generally near a die size similar to array CSPs, which have hidden termination pads, but they are also different. They do not have solder ball spheres, but rather metallized terminations or pads and a large heat-dissipation pad under the package. Leadless packages are also known as bottom-termination components (BTCs) and numerous other nomenclatures (see Table 2-2). The terms include quad flat no-lead (QFN), dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no-lead (DFN), and land grid array (LGA) packages. In addition, new terms were added for the more recently introduced improved versions. These include the advanced QFN (aQFN) and array QFN packages, which generally have multiple row terminals accommodating a higher number of inputs/outputs (I/Os). The

number of I/Os approaches that of CSP/FBGA packages with the advantages of lower cost for portable and telecommunication applications.

The new I/O configuration of QFNs with an extra internal heat-sink pad will add new requirements for design, assembly, rework, and reliability limits, which are significantly different from array CSP packaging technologies. Since there are no leads or balls in leadless packages to compensate for distortion from package or board warpage, these packages require much more control than those of CSPs in design and assembly processes. The new requirements add challenges in the second-level assembly and reliability.

Inspection for assembly integrity verification and quality control has become even more challenging than those difficult conditions for CSPs. The outer terminations could be inspected visually, but we are still unable to determine integrity under the terminations. For the heat-sink pad, the only voiding condition can be determined with nondestructive tools such as X-ray. This chapter summarizes the literature surveyed covering these aspects of leadless packaging technologies, as well as second-level reliability and correlation to workmanship defects such as voids to reliability [11-20].

Table 2.2. Typical leadless packaging styles, nomenclatures, and package supplier.

QFN Style	Definition	Reference
MLF/QFN	Micro-lead frame Quad flat no-lead package	[11, 12]
DRMLF	Dual-row MLF	[13]
aQFN	Advanced QFN	[14]
Array QFN	Array QFN	[15]
DFN	Dual flat no-lead package	[16]
NBA-QFN	No bump array QFN	[17]
TQFN	Thin QFN	[18]
VQFN/WQFN	Very thin QFN	[19]
LGA	Land grid array	[20]

2.3 QFN Packages and Assembly

In a 2003 paper [21], A. Syed and K. WonJoon stated that within the last few years, the QFN package has taken the industry by storm, and that one billion parts had already been shipped. Figure 2-2 shows a number of early generation leadless packaging configurations including the MicroLeadFrame® package (MLF®), which was introduced more than a decade ago.

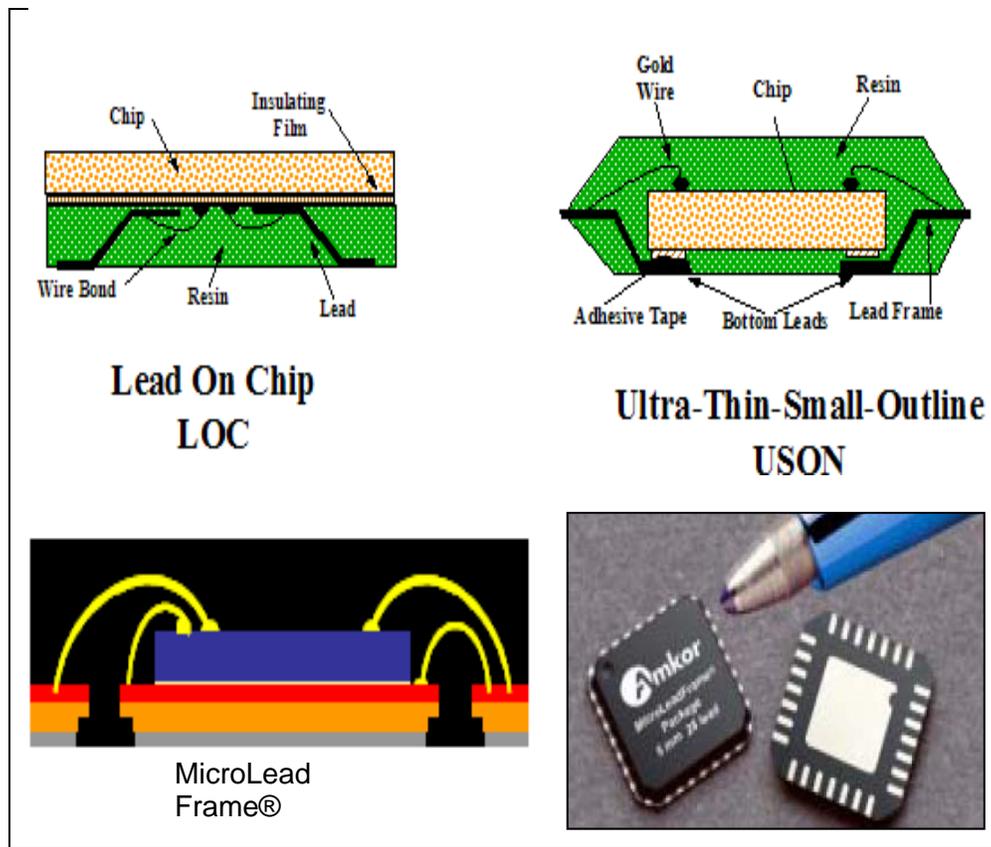


Figure 2-2. Examples of early generation of leadless packages including MLF® package.

The MLF® is a near-CSP plastic encapsulated package with a copper lead frame substrate. It is a leadless package where electrical contact to the printed circuit board (PCB) is made by soldering the peripheral lands on the bottom surface of the package to the PCB, instead of the conventionally formed perimeter leads such as thin small outline package (TSOP). For MLF, the large conductive bottom pad improves the thermal and electrical properties of the package. Note the top images show earlier versions of the leadless packages such as lead on chip. There are no bottom heat-spreader pads in the early version of leadless packages.

The exposed die-attach pad on the bottom efficiently conducts heat to the PCB and provides a stable ground and electrical connections through conductive die-attach material. The design also allows enhancement of electrical performance by enabling the standard 2 GHz operating frequency to be increased up to 10 GHz with some design modifications.

It is common for the QFN package supplier to perform some experimental trials to develop guidelines for the PCB pattern design and document them in the application notes. For example, a QFN package supplier published the first revision of its application notes in September 2002 [21].

Figure 2-3 shows a PCB pad pattern design recommend for the QFN. As is apparent, the design requires that the lands on the package bottom side are to be rectangular with rounded edge on the inside. Since the package does not have any solder balls, the electrical connection between the package and the motherboard is made by printing the solder paste on the motherboard and reflowing it after component placement. In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and solder paste printing.

The target audience of the IPC 7093 is composed of managers, designers, process engineers, operators, and technicians who deal with the processes of electronic design, assembly, inspection, and repair. The IPC committee accepts that even though the document is not a complete recipe—refer to package supplier application notes and literature—it identifies many of the characteristics of robust and reliable assembly processes and provides guidance information to component suppliers regarding the issues being faced in the assembly processes. The IPC committee identifies two key issues in BTC: (1) providing the appropriate amount of solder paste; and (2) ensuring solder-joint reliability is met.

Providing an appropriate solder amount requires effective pad design, which is becoming challenging since most current QFN packages have fine pitch pad design; therefore, there is very limited room available for the optimum pad configuration. The pad designer should also consider the soldering reflow process because during assembly, liquid solder buoyancy of the individual small pads competes with the larger heat-sink pad solder surface tension. If these two competing forces become unbalanced, they will cause processing defects.

3. QFN ASSEMBLIES AND RELIABILITY

3.1 As assembled build

The scope of QFN packages are wide and need to be narrowed for those that are now mature. As QFNs are integrated for high-reliability applications, a continual need for reliability data for standard environmental stress screening (ESS) test methodologies is needed. However, ESS is rarely tested until failure, and little is learned on the mechanistic failure modes of the devices from this type of stress testing. One typical ESS test methodology is based upon IPC-9701A thermal shock test condition TC4; -55°C to $+125^{\circ}\text{C}$ and TC5, -55°C to $+100^{\circ}\text{C}$.

To determine the effects of QFN assemblies under two severe thermal stress conditions, QFNs with various sizes were used for assembly onto PCBs. Two daisy-chain board design from two suppliers were used. However, the assembly was done in one facility to remove the effect of this as a potential variable from the test matrix design. Figure 3-1 shows a representative test vehicle assembly (TV), which also includes images at higher magnification taken from various sections. Each daisy-chain package configurations ends with two probing pads for daisy-chain resistance measurement. The printed circuit board surface finish was electroless nickel immersion gold (ENIG) with 0.062 inch in PCB thickness.

The test matrix variables included eutectic tin-lead solders and a number of QFN sizes (see Fig. 3-2). The QFN package types were from 16 to 68 I/Os, sizes from 5x5 mm to 10x10 mm, and pitches from 0.5 mm to 0.8 mm. Figure 3-3 shows representative images of the QFN solder joints at a higher magnification. The integrity of solder joints is apparent even though it is difficult to confidently project their reliability due to smallness of solder joints and additional interconnection under the package. Therefore, apparent solder joint integrity alone is not sufficient to determine integrity. In addition, visual inspection was also performed on selected assemblies to determine the quality of solder joints, and (if daisy-chain results can be confirmed) by visual inspection. Generally, lack of proper solder joint formation was the key for daisy-chain opens. X-section was performed after thermal cycling for failure analysis and confirmation of daisy-chain conditions (failure or no failure).

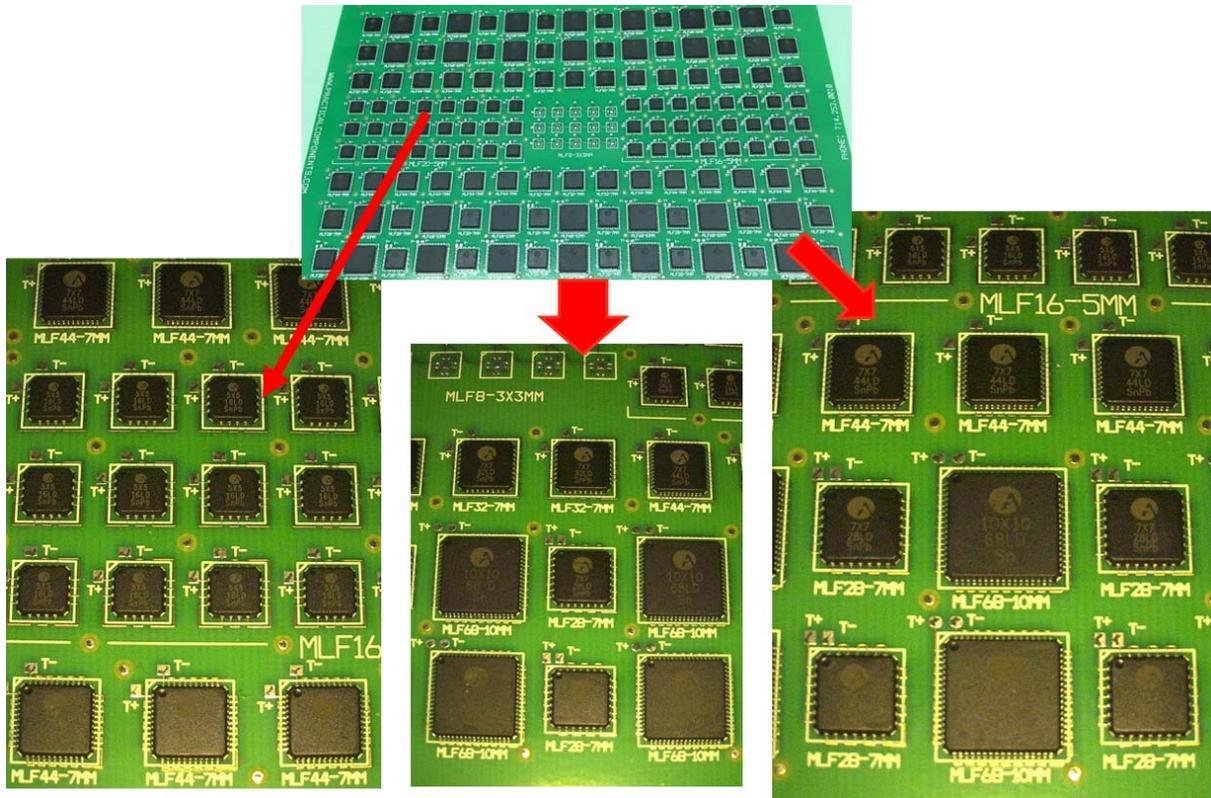


Figure 3-1. QFN daisy-chain assembled onto ENIG PCB finish with 0.062 inch PCB thickness. Assembled by a supplier.

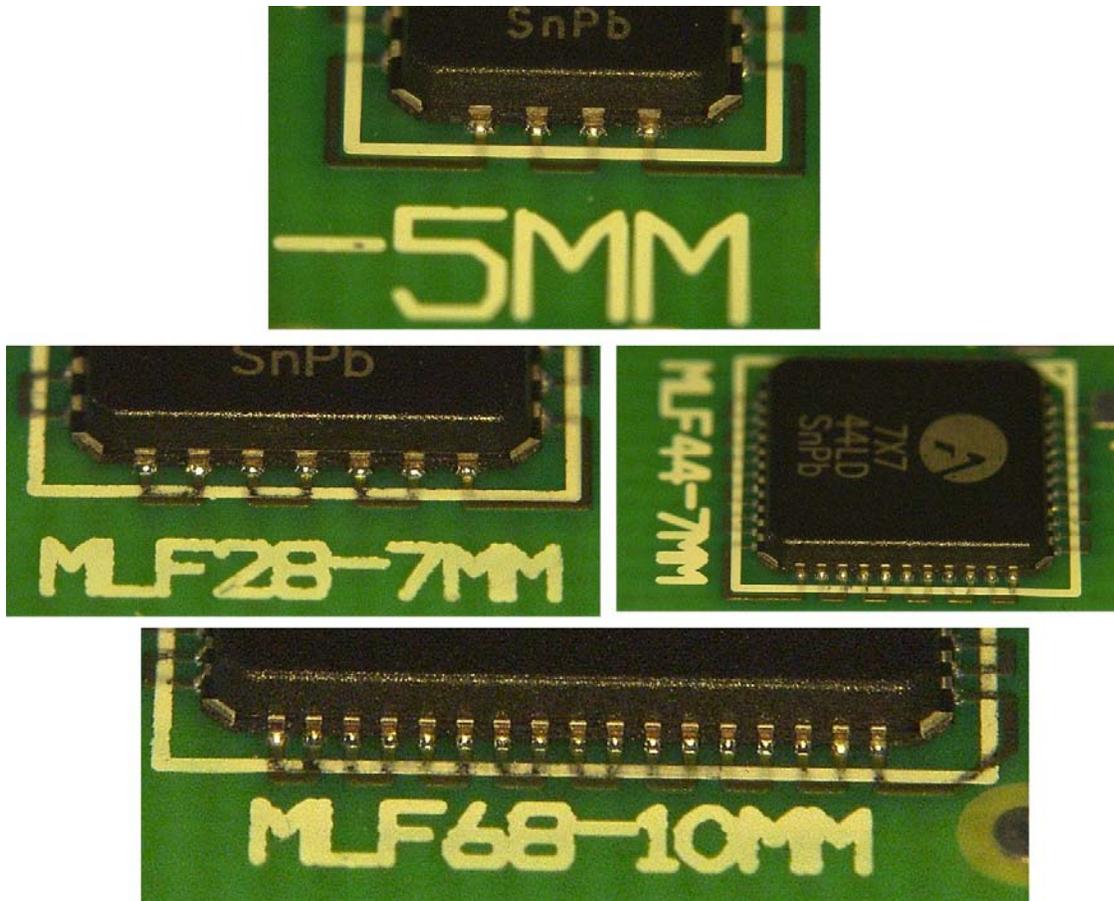


Figure 3-2. Representative of the optical images of various QFN parts including MLF16-5mm², MLF28-7mm², MLF44-7mm², and MLF68-10mm².

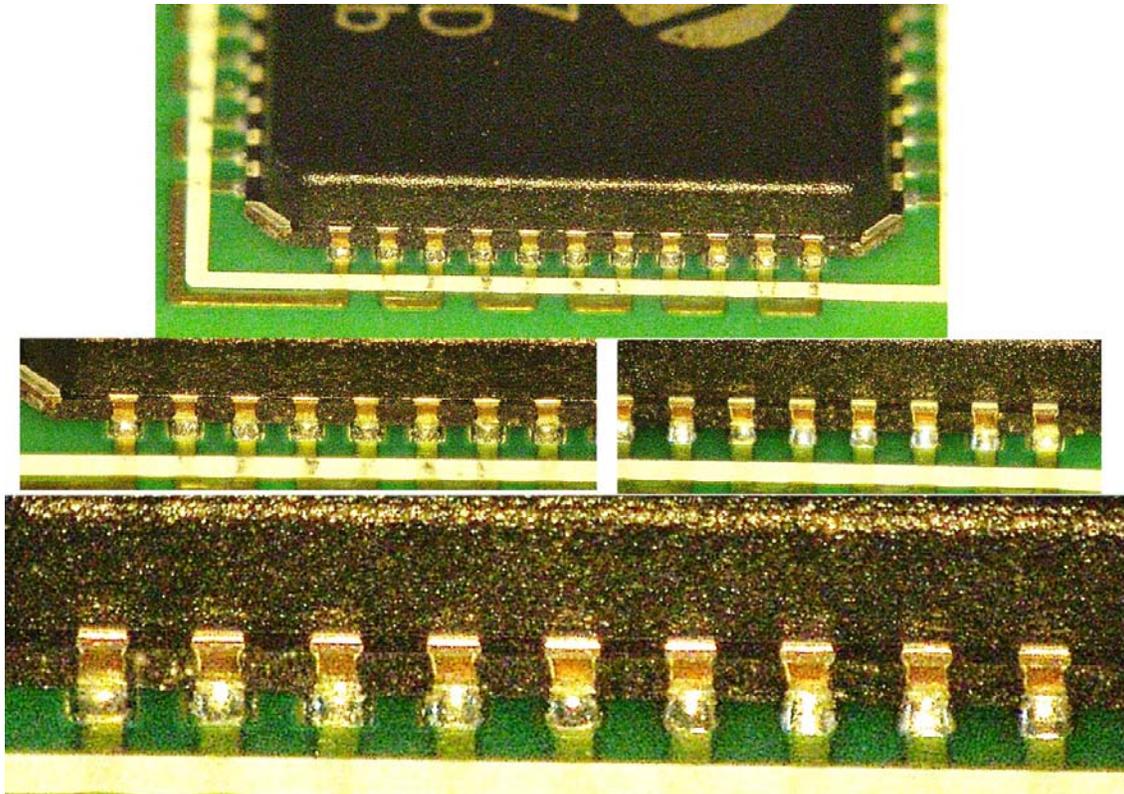


Figure32-3. Representative optical images of a number of QFN assemblies showing solder joint formation and exposed copper.

All the QFN packages had daisy-chain patterns for checking opens after assembly and for checking opens during reliability evaluation. This allowed users to determined condition of interconnections after assembly. A number of packages showed opens after build. These were documented and were not considered for reliability evaluation.

The real time 2D X-ray of the two assemblies revealed no shorts or excessive solder balling and is considered to be acceptable. This build was repeated one more time and achieved acceptable quality results. Figure 3-4 shows a number of X-ray images representative of corners and centers of the assemblies with various sizes of MLFs. Figure 3-5 had enhanced one X-ray image to better delineate the two MLF sizes. Voids at the ground center pads are apparent and their levels are within the IPC specification.

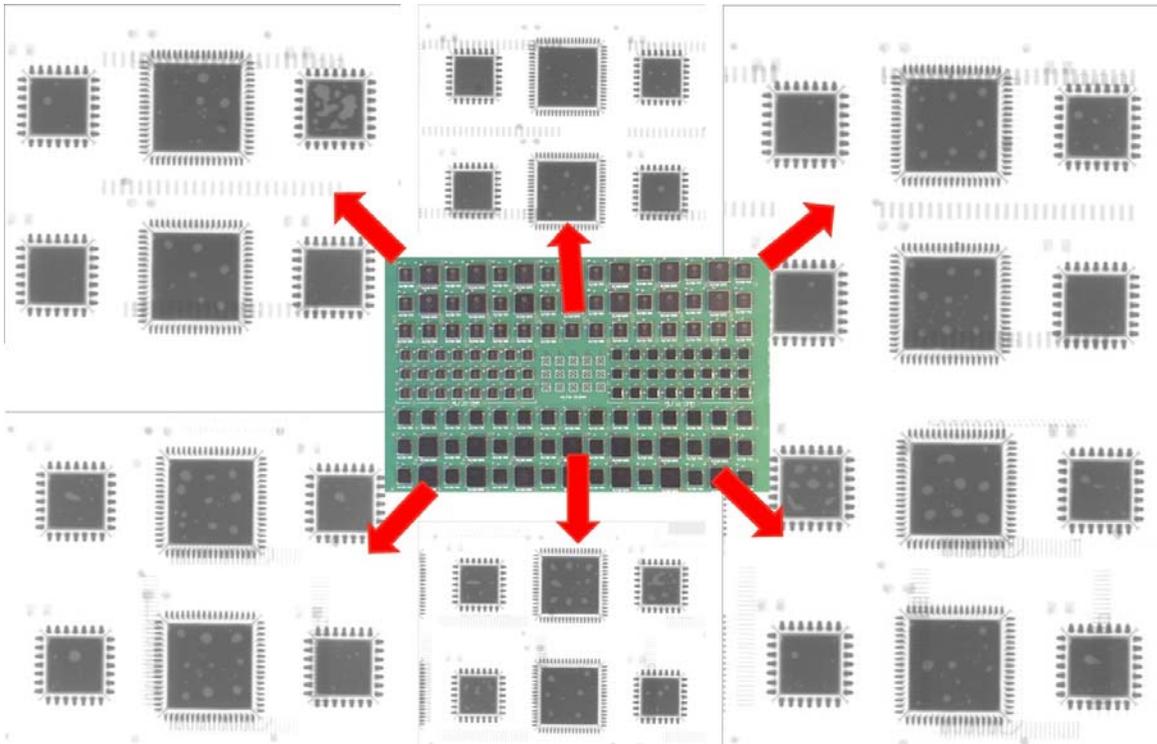


Figure 3-4. X-ray photomicrograph images of corner and center one QFN assembly showing various QFN sizes and level of voids at the their ground pads.

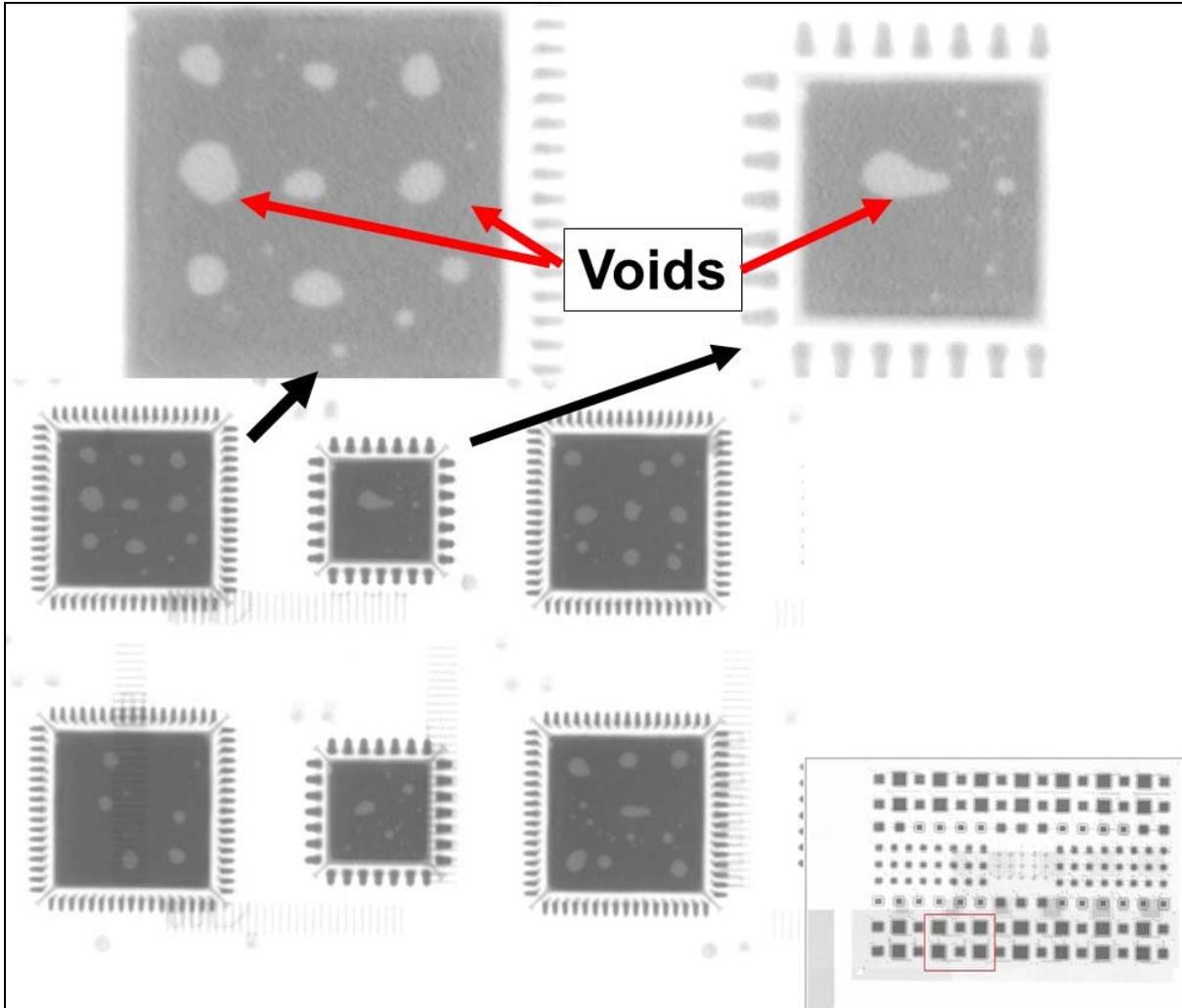


Figure 3-5. X-ray photomicrograph images of a section of the A test vehicle with plastic two QFN sizes showing void levels at the ground pads.

3.2 Reliability under Thermal Aging Plus Thermal Shock (TS) Cycles (- 55°C /125°C)

One QFN assembly was subjected to 250 hours of isothermal aging prior to thermal shock cycles. Thermal cycle testing was conducted in the range of -55°C to +125°C as specified in the IPC 9701, but violating the maximum ramp requirement of less or equal than 20°C/min. Figure 3-6 shows a typical profile with dwell times of more than 10 minutes at the hot and cold temperature. It also includes an image of chamber fully loaded with different types of QFN assemblies.

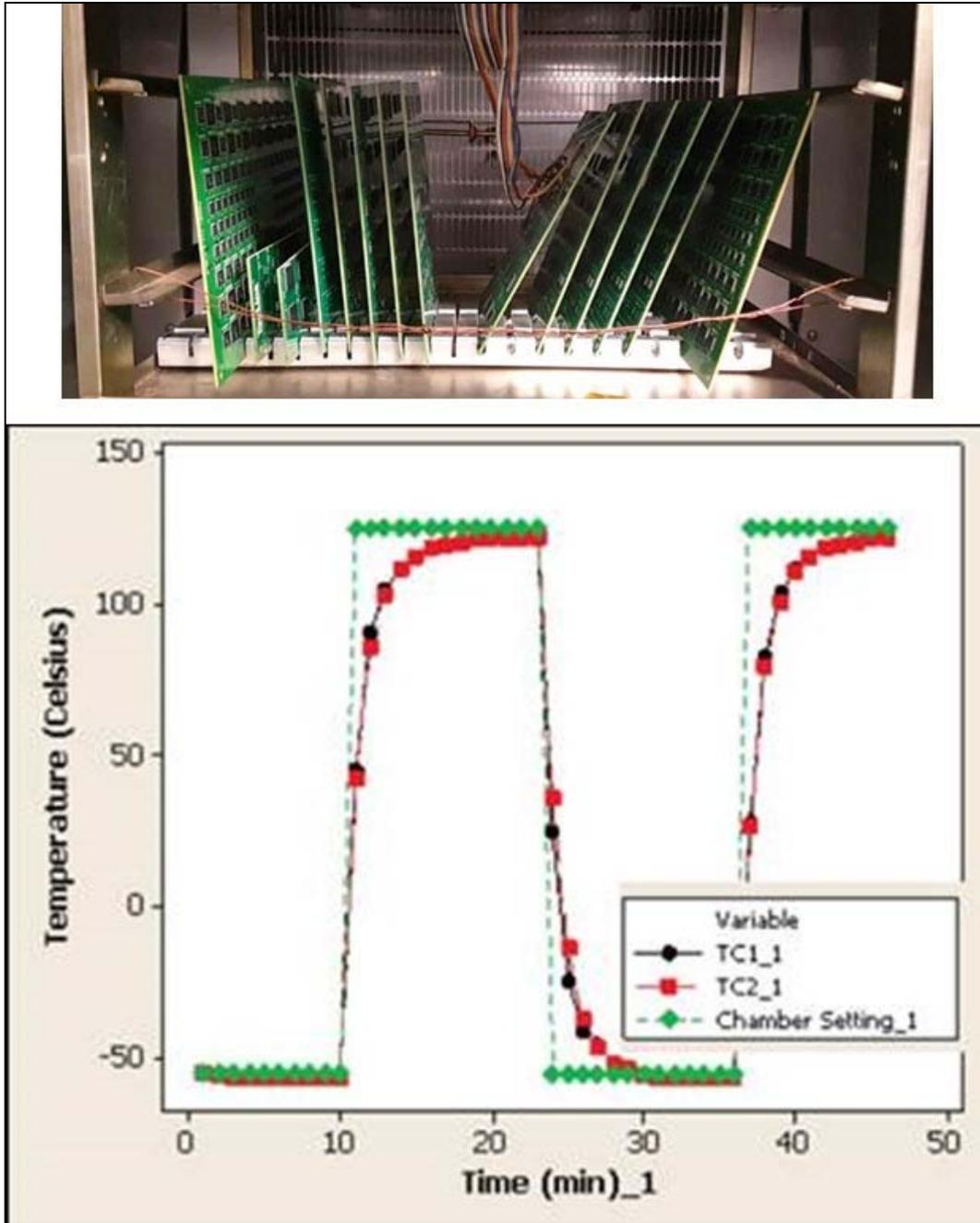


Figure 3-6. A representative thermal shock cycle profiles (-55/125°C) (bottom) and chamber with type A and B samples.

Table 3-1 lists the number of accumulative failures for three different failed MLF sizes under only TS cycles. The daisy-chains were measured after “as received” and at the intervals of 186 cycles, currently at its 5th intervals, a total of 1166 cycles. Only these sizes had failures to 1166 thermal shock cycles. As expected, the number of failures depended on the size of MLF packages. Only one failure for the MLF16-5 mm-0.8 (16 terminations, 5 mm² size, and 0.8 mm pitch), which detected at 1166 cycles; whereas the MLF28-7 mm-0.8 (28 terminations, 7 mm² size, and 0.8 mm pitch) had five failures, one detected at 744, and 4 at 1166 TS cycles. The MLF68-10mm-0.5, the largest MLF part had a total of 17 failures at 1166 TS cycles, one at 558 cycle, five at 930, and eleven at 1166.

Table 3-1. The cumulative failures for different MLF package sizes under thermal shock cycle alone (-55/125°C).

QFNs Cycles	MLF16-5-0.8 Total # of Failures	MLF28-7mm-0.8 Total # of Failures	MLF68-10-0.5 Total # of Failures
1x186= 186	0	0	0
2x186= 336	0	0	0
3x186= 558	0	0	1
4x186= 744	0	1	1
5x186= 930	0	1	6
6x186=1116	1	5	17

Types and location of MLF failures are shown in Figure 3-7. Even though failures are dependent on the MLF sizes, there is no apparent correlation with the location of package on the board, as is expected.

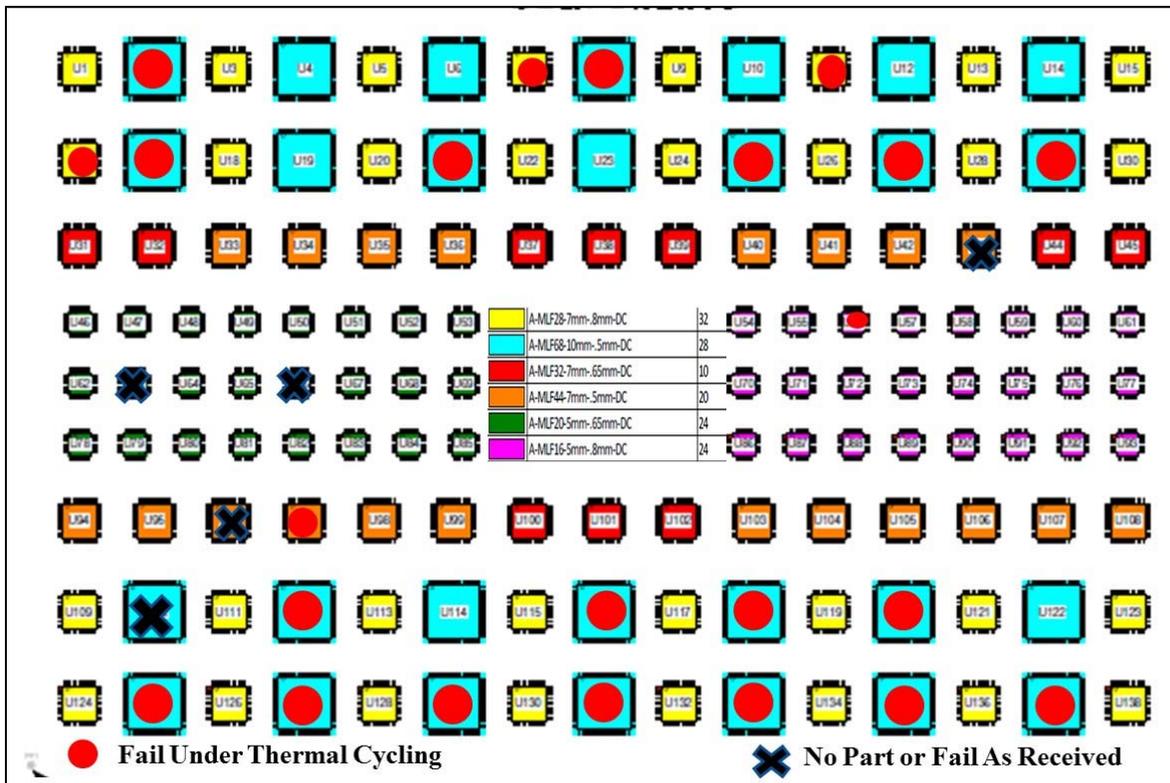


Figure 3-7. Schematic MLF failure location and package size at 1166 thermal shock cycle only (-55/125°C).

The QFN assemblies with 250 hr age plus 1166 thermal shock cycles, the accumulative number of failures are shown in Table 3-2. To compare with Table 2, it included results for the MLF16-5mm-0.8 and MLF28-7mm-0.8. These packages showed no failures under the combined condition whereas they showed a few failures under TS cycles alone. However, the MLF68-10 mm-0.5 (68 terminations, 10 mm² size, and

0.5 mm pitch) showed two failures at 930 and eleven additional failures, a total of 13 failures at 1166 TS cycles. This is the only package that failed after combined aging and TS cycles,

Table 3-2. The cumulative failures for different MLF package sizes under 250 hr isothermal aging plus 1166 thermal shock cycles (– 55°C /125°C).

Age+Cycles	QFNs	MLF16-5-0.8 Total # of Failures	MLF28-7mm-0.8 Total # of Failures	MLF68-10-0.5 Total # of Failures
1x186= 186		0	0	0
2x186= 336		0	0	0
3x186= 558		0	0	0
4x186= 744		0	0	0
5x186= 930		0	0	2
6x186=1116		0	0	13

Types and location of MLF failures for the combined conditions are shown in Figure 3-8. Only the large packages failed contrary to TS cycles alone that showed two other package size failures. It appears that a short term aging had improved resistance to thermal shock cycles for tin-lead eutectic solder, but possibly the “as assembled” quality also could be a contributor. Much larger sample sizes are required to verify the validity of this findings.

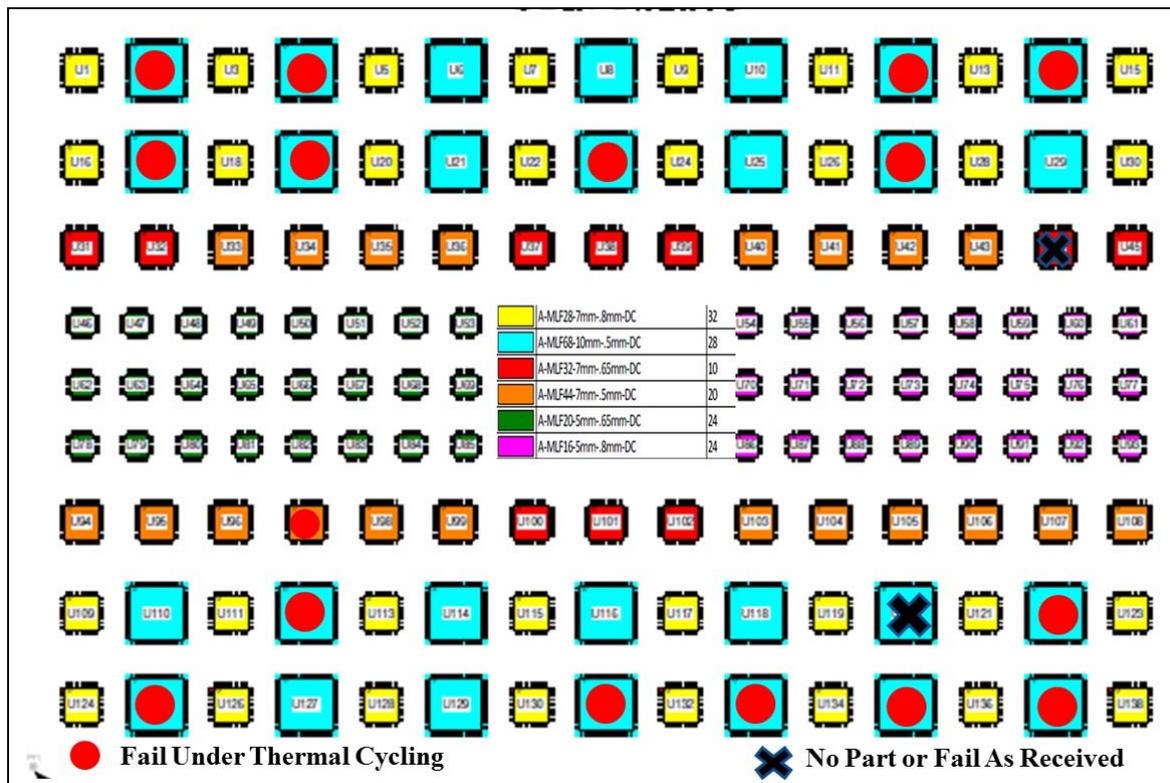


Figure 3-8. Schematic MLF failure location and package size at 1166 thermal shock cycle only (– 55/125°C).

3.3 Failure Analysis

In addition to daisy-chain monitoring at thermal shock cycle intervals, failure analysis was performed by optical and cross-sectioning to verify levels of damage, microcracking, and full cracking (open). Figure 3-9 shows one row of microstructural condition for MLF with 28 termination, size of 7 mm^2 , and 0.8-mm pitch that showed no daisy-chain failures after 1116 cycles. A number of assemblies were X-sectioned after 1488 cycles. It clearly shows no failure even though signs of minor microcracking are apparent. Figure 3-10 shows representative solder joints, corners, adjacent to corner, and center, for MLF, 68 pads, 10 mm^2 , and 0.5 mm pitch that showed a large number of failures after 1166 cycles. X-section is after 1488 cycles. A number of solder joint interconnections at the left side of a package row were failed. There were no failures at the right side of the row. The signs of cracking reduced to microracking from the left to the right of this row.

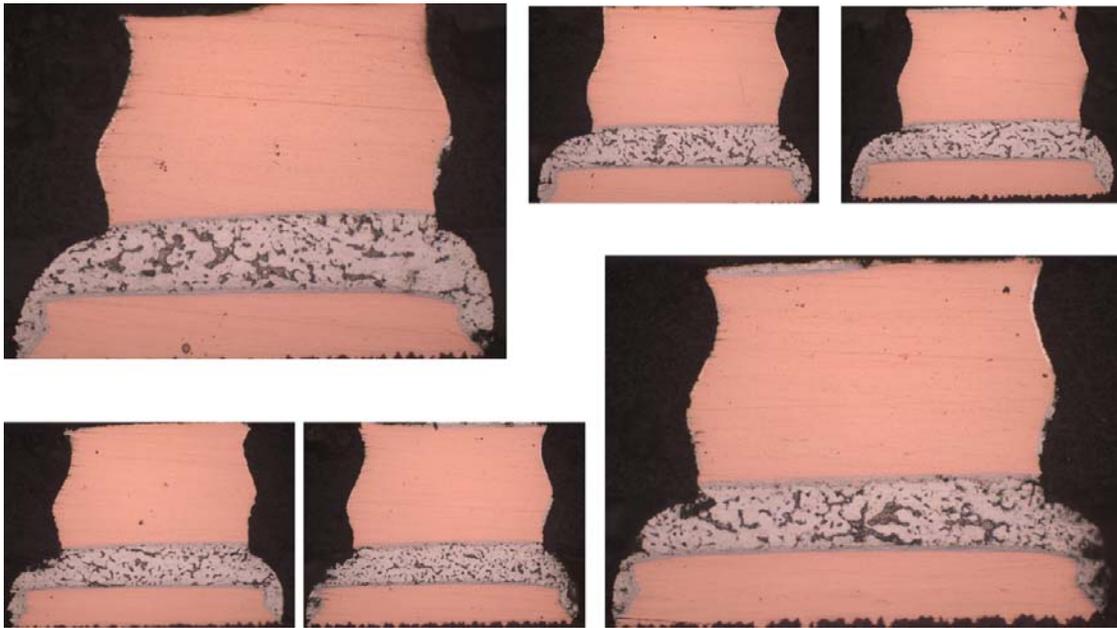


Figure 3-9. Microstructural images of MLF28-7 mm^2 -showing some signs of microcracks after 1488 thermal shock cycle only (-55/125°C).

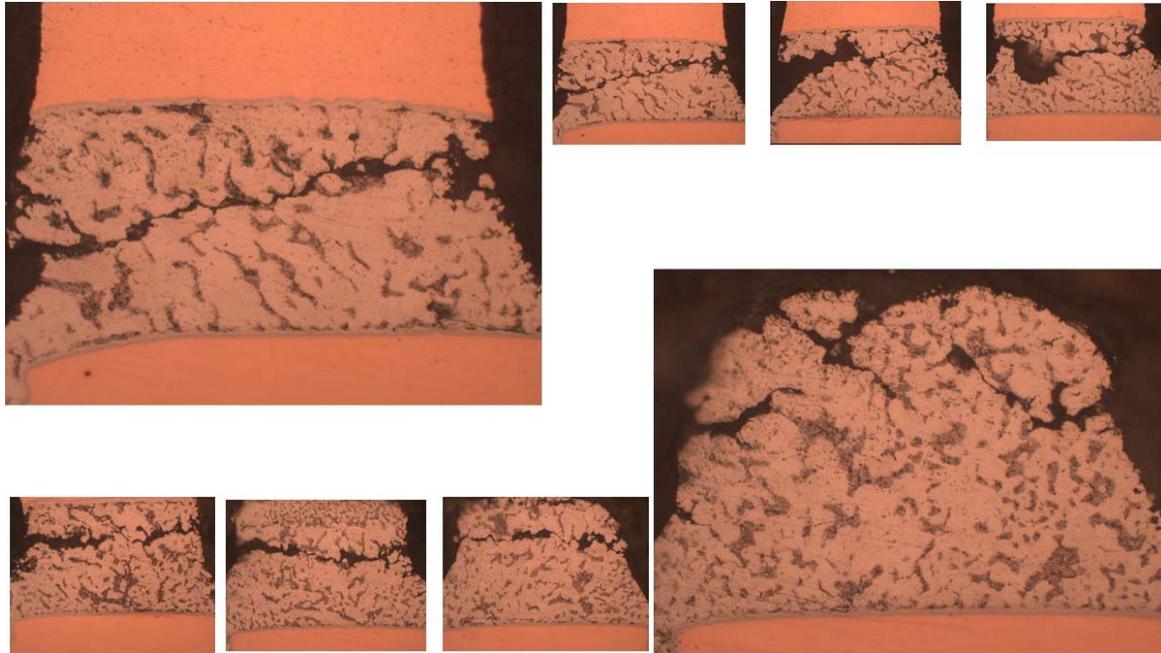


Figure 3-10. Microstructural images of the failed MLF68-7 mm-10 mm showing some signs of microcracks and cracks after 1488 thermal shock cycle only ($-55/125^{\circ}\text{C}$). Extensive cracks confirms early failure of this QFN.

3.4 Reliability under TSC only ($-55/100^{\circ}\text{C}$)

QFN assemblies were also subjected to a milder thermal shock cycles. The temperature range of -55°C to $+100^{\circ}\text{C}$ as specified in IPC 9701, but violating the maximum ramp requirement of less than or equal to $20^{\circ}\text{C}/\text{min}$. Figure 3-11 shows a typical profile with dwell times of more than 10 minutes at the hot and cold temperature.

Daisy-chain resistances were measured after assembly and at 100 thermal cycle intervals. After 200 thermal cycles, there were no daisy-chain resistance changes, indicating no failures. We did not continue further thermal cycling since by this time we had gathered failure data for harsher thermal shock cycle conditions. This milder profile requires a larger number of cycles than the harsher cycle condition in order to get a reasonable number of failures. The long-time required cycling extended beyond the scope of testing time allocation and cost; therefore, thermal cycling was not continued.

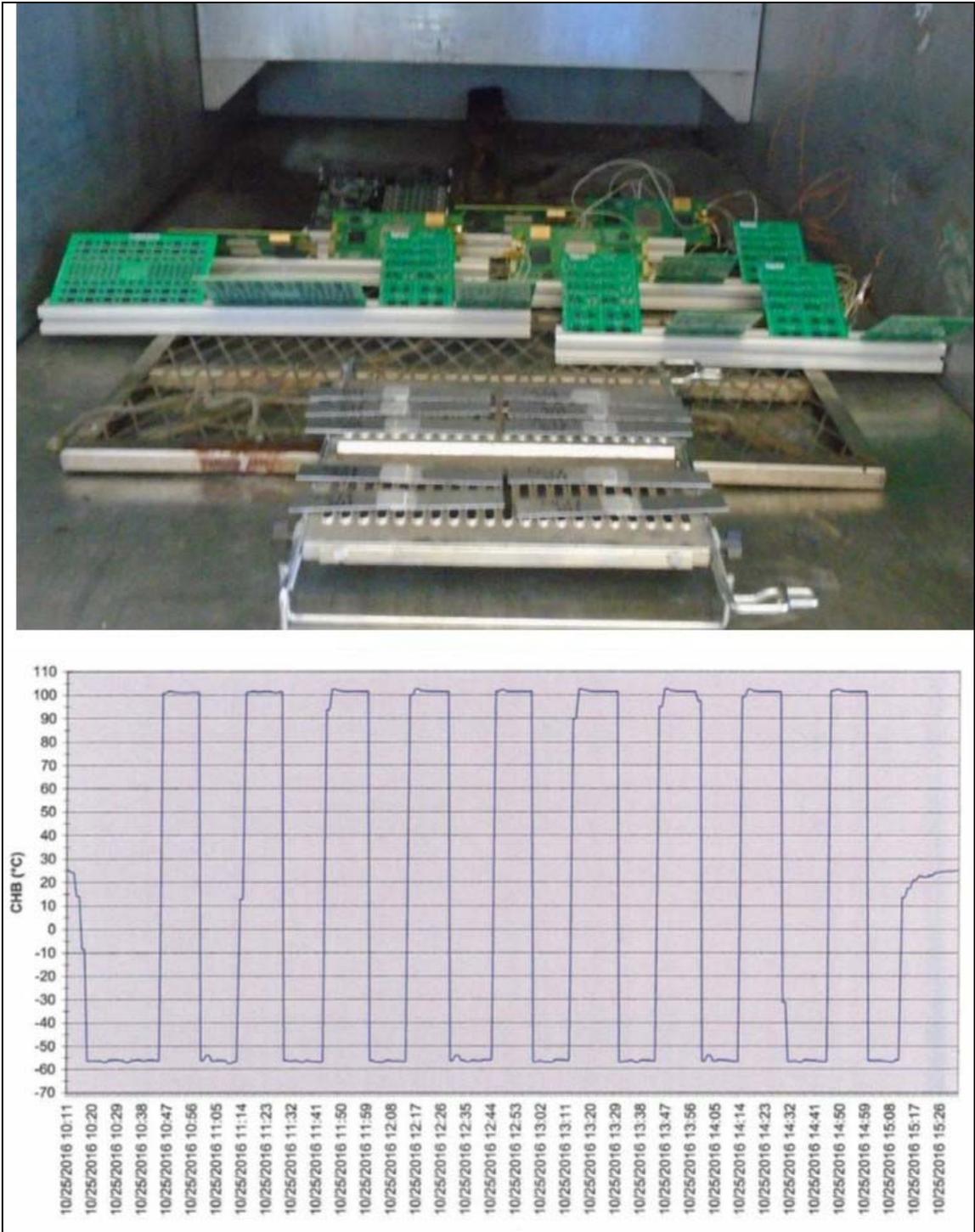


Figure 3-11. A representative thermal shock cycle profile (- 55/100°C) (bottom) and chamber with test vehicles.

4. CONCLUSIONS

This report addressed the effects of numerous variables on assembly reliability of QFN packages with different sizes. Assemblies were subjected to two harsh thermal shock/cycle conditions with the test results summarized in the following:

- No failure to 200 TS cycles ($-55^{\circ}\text{C}/100^{\circ}\text{C}$) for single-sided assemblies with tin-lead solder QFN assemblies.
- A large number of failures for MLF 68 I/O under 1166 thermal shock cycles only (-55°C to 125°C) and combined with 250 hours of isothermal aging at 125°C with subsequent 1166 TS cycles.
- It appears that initial isothermal aging improved resistance to subsequent thermal shock for tin-lead solder assemblies, but this must be confirmed by testing of a larger sample size.
- Failure analysis by cross-sectioning confirmed the observation made by daisy-chain monitoring. The failed MLF68 showed a number of solder joints with full cracking whereas MLF28 showed only minor microcracking.

The test results showed that the thermal shock cycle reliability of QFN depends on the size and thermal shock cycle profiles. The report presented the test results for tin-lead solder interconnection of single-sided boards, which are used for tin-lead high reliability applications. Understanding key current technology status for QFN and advanced QFN packaging technologies (along with test verification for quality assurance and reliability) are important in risk reduction for their use in high-reliability applications.

5. ACRONYMS AND ABBREVIATIONS

aQFN	advanced quad flat no-lead
Bn	billion
ASIC	application-specific integrated circuit
BGA	ball grid array
BTC	bottom termination component
CAAGR	compounded average annual growth rate
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
COF	chip on flex
COG	chip on glass
CGA	column grid array
CMOS	complementary metal oxide semiconductor
COB	chip-on-board
CSP	chip scale package
CTE	coefficient of thermal expansion
DCA	direct chip attachment
DFN	dual flat no-lead package
DiP	dual-in-line package
DOE	design of experiment
DRMLF	dual-row micro-lead frame
DRQFN	dual-row quad flat no-lead

EMS	electronics manufacturing services
ENIG	electroless nickel immersion gold
ESS	environmental stress screening
FBGA	fine pitch ball grid array]
FCBGA	flip-chip ball grid array
FCOB	flip chip on board
FEA	final element analysis
FPBGA	fine pitch ball grid array
HCTE	high coefficient of thermal expansion
HDP	high-density package
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
iNEMI	International Electronics Manufacturing Initiative
I/O	input/output
IPC	Association Connecting Electronics Industries
ITRS	International Technology Roadmap for Semiconductors
JPL	Jet Propulsion Laboratory
KGD	known good die
LCC	leadless chip carrier
LGA	land grid array
LOC	lead on chip
MEMS	micro-electro-mechanical systems
MLF	micro lead frame
MRQFN	multi-row quad flat no-lead
MtM	more than Moore
NBA	no-bump array
NASA	national aeronautics and space administration
ODM	original design manufacturer
OEM	original equipment manufacturer
PBGA	plastic ball grid array
PCB	printed circuit board
PGA	pin grid array
PTH	plated through hole
PWB	printed wiring board
QFN	quad flat no-lead
QFP	quad flat package

RDL	redistribution layer
RF	radio frequency
RoHS	(European Union) restriction of hazardous substances
SIA	semiconductor industry association
SiP	system in package
SMT	surface mount technology
SO	small outline
SOC	small outline chip
SOT	small outline transistor
Tg	glass transition temperature
TQFN	thin quad flat no-lead
TS	thermal shock
TSC	thermal shock cycle
TSOP	thin small outline package
TSV	through silicon via
TV	test vehicle
USON	ultra-thin-small-outline
VQFN	very thin quad flat no-lead
WLP	wafer level package
WCSP	wafer level chip scale package
WLCSP	wafer-level chip-scale packaging
WLP	wafer level package
WQFN	wafer quad flat no-lead

6. REFERENCES

IPC Validation Services Documents

IPC 7093: Guidelines for Design and Assembly Process Implementation for Bottom Termination Components

IPC 7351: Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC 7525: Stencil Design Guidelines

IPC-9701. Performance Test Methods and Qualification Requirements for Surface Mount Solder.

- [1] iNEMI, International Electronics Manufacturing Initiatives, <http://www.inemi.org/inemi-roadmap>, accessed June 2017
- [2] ITRS, International Technology Roadmap for Semiconductors, <http://www.itrs.net/>, accessed Mar. 2017.
- [3] IPC, Association Connecting Electronics Industry, <http://www.ipc.org>, accessed Mar., 2017.
- [4] R. Ghaffarian, "Damage and Failures of CGA/BGA Assemblies under Thermal Cycling and Dynamic Loadings," ASME 2013 International Mechanical Engineering Congress and Engineering. IMECE2013, November 15–21, San Diego, California, USA.
- [5] R. Ghaffarian, "Thermal Cycle and Vibration/Drop Reliability of Area Array Package Assemblies," Chapter 22 in *Structural Dynamics of Electronics and Photonic Systems*, eds. E. Suhir, E. Connally, and D. Steinberg Springer, 2011.

- [6] R. Ghaffarian, "Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies with and without Corner Staking," *IEEE Transactions on Components and Packaging Technologies*, vol. 31, issue 2, June 2008.
- [7] R. Ghaffarian, "Area Array Technology for High Reliability Applications," Chapter 16 in *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*, ed. E. Suhir, Springer, 2006.
- [8] R. Ghaffarian, "CCGA Packages for Space Applications," *Microelectronics Reliability*, vol. 46, pp. 2006–2024, 2006.
- [9] R. Ghaffarian, "BGA Assembly Reliability," Chapter 20 in *Area Array Packaging Handbook*, ed. K. Gilileo, McGraw-Hill, 2004.
- [10] J. Fjelstad, R. Ghaffarian, and Y.G. Kim, "Chip Scale Packaging for Modern Electronics," *Electrochemical Publications*, vol. 20, no. 4, p. 47, 2002.
- [11] "QFN (MLF) Package Design Kits for Agilent ADS," Amkor Technology, <http://www.amkor.com/go/customer-center/qfn-mlf-package-design-kits-for-agilent-ads>, accessed Mar. 2017.
- [12] "QFN Package Mounting Guidelines, Atmel," <http://www.atmel.com/images/doc8583.pdf>, accessed Mar. 2017.
- [13] Application Notes for Surface Mount Assembly of Amkor's Dual Row MLF Packages, <http://www.amkor.com/go/packaging/document-library>, accessed Mar., 2017.
- [14] A. Tseng, M., Lin, B. Hu, J.W. Chen, J.M. Wan, S. Lee, and L. Yi-Shao, "Advanced QFN Surface Mount Application Notes development," *12th Electronics Packaging Technology Conference (EPTC)*, 2010.
- [15] "Design Guide 92NLA Array QFN, Texas Instruments," <http://www.ti.com/lit/an/slma006/slma006.pdf>, accessed Mar. 2017.
- [16] "Dual Flat No-Lead Package Family (DFN)," Intersil, <http://www.intersil.com/content/dam/Intersil/documents/mdp0/mdp0047.pdf>, accessed Mar. 2017.
- [17] V. Lin, E. Chen, D. Lee, and C. Chen, "Package Characterization on Advanced NBA-QFN Structure," *5th IMPACT, Oct 2010, Taipei, Taiwan*, 2010.
- [18] "TQFN (Thin Quad Flat No-Lead) Package Family), Intersil, <http://www.intersil.com/content/dam/Intersil/documents/mdp0/mdp0051.pdf>, accessed Mar. 2017.
- [19] StatChiPAC, <http://www.statschippac.com/>, accessed June 2017.
- [20] "Land Grid Array (LGA) Package Rework," *Freescale Semiconductor Application Note*, AN3241, Rev 1.0, 10/2009, http://cache.freescale.com/files/rf_if/doc/app_note/AN3241.pdf, accessed Mar. 2017.
- [21] A. Syed and K. WonJoon, "Board Level Assembly and Reliability Considerations for QFN Type Packages," *Surface Mount Technology Association Proceedings*, 2003 http://www.smta.org/knowledge/proceedings_abstract.cfm?PROC_ID=1350, accessed Mar. 2017.
- [22] *Design and Assembly Process Implementation for Bottom Termination SMT Components*, IPC, Association Connecting Electronics Industry, IPC 7093 Table of content, <http://www.ipc.org/TOC/IPC-7093.pdf>, accessed Mar. 2017.