Microsemi RTG4 Rev C Field Programmable Gate Array Single Event Effects (SEE) Heavy-ion Test Report

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1. INTRODUCTION

The goal of this study was to perform an independent investigation of single event destructive and transient susceptibility of the Microsemi RTG4 device. The devices under test were the Microsemi RTG4 field programmable gate array (FPGA) Rev C. The devices under test will be referenced as the DUT or RTG4 Rev C throughout this document. The DUT was configured to have various test structures that are geared to measure specific potential susceptibilities of the device. Design/Device susceptibility was determined by monitoring the DUT for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing the DUT to a heavy ion beam. Potential Single Event Latch-up (SEL) was checked throughout heavy-ion testing by monitoring device current.

The objectives of this study are the following:

- Analyze DFF behavior in simple designs such as shift registers. Compare SEU behavior to more complex designs such as counters and finite impulse response (FIR) filters. Evaluating data trends helps in extrapolating test data to actual designs.
- Analyze global route behavior – clocks, resets.
- Analyze configuration susceptibility.

2. DEVICES TESTED

2.1 Device Specifics

The DUT part number is: RT4G150-CG1657M. We tested two revision bins: Rev B and Rev C. However, this document will only reference Rev C data. Rev B data has been published in an alternate document.

The following is a list of tested device by lot date code and test date:

- RT4G150-CB1657MSX449, lot date code: 1534 (TAMU2015Dec; LBNL2016Mar)
- RT4G150-CB1657PROTOX463, lot date code: 1548 (TAMU2016Oct; LBNL2016Oct)
- RT4G150-CB1657PROTO, lot date code: 1629 (TAMU 2016Oct-Nov; LBNL 2016Oct)
- RT4G150-CB1657PROTO, LDC 1638 (TAMU 2017March)

The DUT contains 158214 look up tables (4-input LUTs); 158214 flip-flops (DFFs); 720 user I/O; 210K Micro-SRAM (uSRAM) bits; 209 18Kblocks of Large-SRAM (LSRAM); 462 Math logic blocks (DSP or HMACC Blocks); 8 PLLs; 48 H-chip global routes (radiation-hardened global routes); 2 FDDRs; and 6 SERDES channels. Figure 1 is a block diagram illustrating the RTG4's internal components.

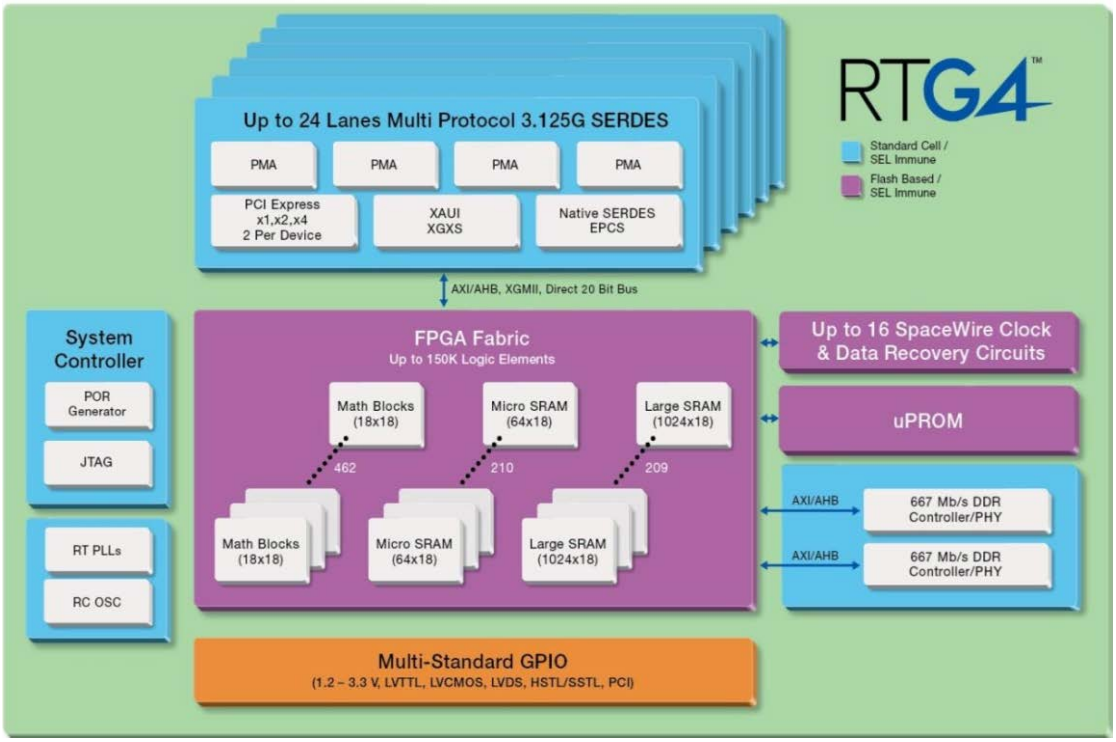


Figure 1: Block diagram of RTG4 internal components.

RTG4 FPGA devices are fabricated using a 65nm Flash technology, which provides industry-leading low power consumption and also provides complete (to be tested) immunity to radiation-induced configuration upsets. Consequently, if the configuration is deemed to be 100% immune, the RTG4 devices never lose their functionality in the harsh space radiation environment. An additional advantage of Flash technology is that the configuration of the FPGA is retained through power cycles, unlike SRAM-based FPGAs, meaning that no companion devices are required for code storage, relieving board space, and eliminating additional component cost. Figure 2 is an illustration of one flash based configuration cell.

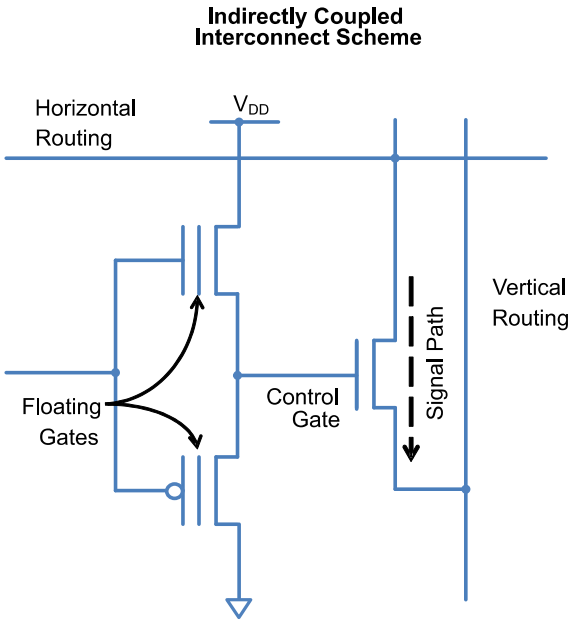


Figure 2: Directly coupled interconnection scheme for Microsemi RTG4 flash configuration cells.

In addition, the manufacturer has implemented Single Event Effect (SEE) Radiation Hardened by Design (RHBD) circuitry that is available to the user such as: localized triple mode redundancy (LTMR) at each flip-flop; and hardened global routing networks (such as clocks). Figure 3 is an illustration of LTMR.

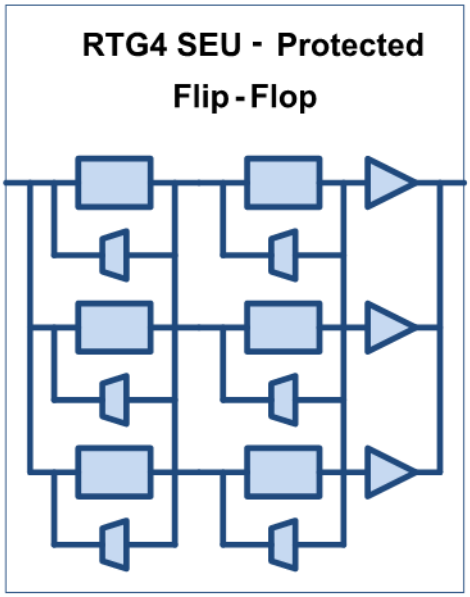


Figure 3: Localized TMR DFF scheme. Microsemi refers to it as self-correcting TMR (STMRFF).

3. BACKGROUND

Testing a Flash-based FPGA requires the user to test SEU behavior in the following device components: Configuration hardness, data path susceptibility, global structures and hidden logic (Single Event Functional Interrupt (SEFI) susceptibility).

3.1 Cross Sections

SEU cross sections (σ_{seu}) characterize how many upsets will occur during a radiation test. Generally a σ_{seu} is calculated by counting the number of observed upsets during irradiation and normalizing it (dividing by) the particle fluence:

General Terminology for heavy-ion testing:

- Flux: Particles/(sec-cm^2)
- Fluence: Particles/cm^2

$$\sigma_{SEU} = \frac{\text{Number of Upsets}}{\text{Fluence}} \quad (1)$$

SEU cross sections are calculated at several linear energy transfer (LET) values (particle spectrum) as in equation (1). Particle flux-settings are determined per LET. It is desired to test with the highest flux in order to achieve acceptable SEU statistics. However, if the flux seems to overwhelm the device during a test, the flux is lowered. Proper flux is determined such that flux rate does not influence the number of errors observed during a test at a given LET.

3.2 Divide and Conquer Test Approach

An FPGA is a complex device with a variety of components containing varying susceptibilities to SEUs. Accordingly, tests are conducted such that components are isolated in order to develop an understanding of each of the component's SEU characteristics [1][2]. REAG categorizes FPGA components and their susceptibilities as follows:

$P(fs)_{error}$: system or design σ_{seu}

$P_{configuration}$: Configuration σ_{seu}

$P(fs)_{functionalLogic}$: data path σ_{seu}

P_{SEFI}: hidden logic and global route σ_{seu}s

All σ_{SEU}s are calculated independently. It is important to note that configuration upsets (if the configuration bit is used by the design and enabled) will cause an upset in the functional operation. However, we denote this type of upset as a configuration upset not a functional logic upset. Functional logic upsets are categorized as malfunction that occurs due to SEUs affecting DFFs or combinatorial logic elements in the programmable user space.

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI} \quad (2)$$

3.3 Configuration Test and Analysis

Configuration SEUs are checked by performing a verify function via Microsemi Libero software. The software does not return an error count. It returns a pass-fail indication. This is deemed an acceptable evaluation because flash-based configuration is considered to have negligible susceptibility to SEUs. This has been shown with ProASIC3 SEU testing.

Configuration upsets may or may not cause a design (system level) error. If a configuration bit, that has changed state because of an SEU, is being used by the design and is in an enabled path of logic, then there is a chance that the changed state will cause system malfunction. Dynamic testing is required to investigate configuration upsets and their impact on system level functionality; i.e., this is not considered a configuration test – it is considered a dynamic functional test. In general, Configuration SEUs that directly affect active circuitry have error signatures that resemble stuck faults. This is because the flash configuration cannot be scrubbed; nor will a power cycle correct non-volatile configuration errors. The device will have to be reconfigured in order to correct configuration SEUs.

3.3.1 Dynamic Test and Configuration Analysis

Dynamic testing concentrates on evaluating the SEU susceptibility of the design under analysis (DUA) during accelerated radiation testing. Such testing requires the DUT to be operating and its outputs to be monitored during irradiation. Deviations from expected values are reported and noted as error responses.

This is a challenging study because, as previously mentioned, the complexity of the FPGA devices has various components with different error signatures and susceptibilities. The component contribution to overall design σ_{seu}s was given in equation (2). If tests are not constructed to isolate these components during the test and analysis phase, radiation data can be convoluted and difficult to process.

3.4 Data Path and Global Upset Investigation:

3.4.1 RTG4 Expected Single Event Upsets and Error Rate Calculation

Following convention, the bit-error rates (dE_{bit}/dt) published in the Microsemi datasheets are calculated from shift register SEU characterization. It is important to note that DFF upsets are both corrected and masked by the LTMR circuitry. Therefore, the most significant upsets in the RTG4 device are due to transients; i.e., combinatorial logic data path SETs captured by DFFs. It has been shown that SET capture by a DFF tends to be directly proportional frequency [2][3]. As a result, radiation tests are performed at various frequencies to determine trends. Each radiation test counts the number of upsets observed during irradiation. The SEU cross section per test is defined to be the number of observed upsets normalized by the particle fluence per test. The goal is to use the SEU cross sections to calculate bit error rates per frequency. Error rates ($dE_{bit}(fs)/dt$) calculated per test design and frequency are extrapolated to predict error rates ($dE(fs)/dt$) of space-flight FPGA circuitry as noted in equation 3.

$$\frac{dE(fs)}{dt} < \frac{dE_{bit}(fs)}{dt} * (\#UsedDFFs) \qquad (3)$$

3.4.2 Test Circuits used for Establishing SEU Cross Sections and Error Rates

Shift registers are the most common test circuit used in SEU radiation testing. Shift registers are considered to have a linear data path because each node only has one input and one output (i.e. fanout = fanin = 1). Due to the decrease in transistor geometries and capacitive node loading it has come to question if the calculated shift register dE_{bit}/dt can be applied to complex circuits. In other words, will the predicted system error rate be accurate using shift register data as parameters? As an example, counter architectures are not linear. They contain nets with fan-out and fan-in >1. The fan-out will change both the capacitive loading of cells and the utilization of routing resources within FPGA fabrics. Depending on the rise/fall time and width of a Single Event Transient (SET) the capacitive loading of a cell can filter away the SET. On the other hand, a SET that is not filtered can fan-out to multiple nodes and can have the effect of a multiple bit upset. As noted, variations of SET signatures exist and will depend on design topology and operational parameters.

Understanding the various upset event probabilities and their effects are essential when designing critical applications and predicting error rates. As a response, a more in-depth approach to SEE characterization of complex circuits has been developed and has been performed by NASA Goddard Radiation Effects and Analysis Group (REAG) on RTAXs and ProASIC3 FPGA devices. The testing technique incorporates testing shift registers and counters. The information extracted from the previous RTAXs-family and ProASIC3 evaluations has been used to develop the RTG4 study as follows:

1. In the RTAXs FPGAs, upsets were observed to be generated via the combinatorial logic data path not from the LTMR'd DFFs. Consequently, SET propagation and transient capture is the most significant source of DUT SEEs.
2. Global route SETs were observed in the ProASIC3 devices at low LET values.
3. Global route SETs were not observed in the RTAXs devices until high LET values – but were still rare events.
4. With the RTAXs FPGAs, the potential for SET propagation through chains of combinatorial logic was attenuated at low Heavy Ion (HI) LET values. It was observed that after approximately 8 levels of logic, the SEE cross section (due to SET attenuation) decreased at low LET values. Emphasis is placed on the fact that this error signature only occurred at low LETs. This is because at Low LET values, generated SETs have less energy. Consequently, these low energy SETs do not have enough power to propagate through multiple levels of combinatorial logic gates.
5. SET propagation was not attenuated at higher HI LET values. As N increased, the SEE cross section increased (as expected) at higher LETs.
6. Circuits with higher fan-in to DFFs can produce lower threshold LETs cross sections. Hence, the error rate will be higher.
7. In the RTAXs FPGAs, as frequency increased, the SEE error cross section increased. This is because most of the upsets occurred from captured SETs in the design data paths and not the LTMR'd DFFs.
8. ProASIC3 configuration is flash memory. Flash configuration SEUs were extremely rare events.

3.5 NASA DUT Preparation Plan

NASA has four populated boards with RT4G150-CG1657M devices. There are two boards that contain RTG4 Rev B FPGAs; and two boards that contain RTG4 Rev C FPGAs. The parts (DUTs) were thinned using mechanical etching via an Ultra Tec ASAP-1 device preparation system (illustrated in Figure 4). The Ultra Tec ASAP-1 system is a proven process previously used successfully on both Virtex-5QV and Virtex-5 parts. The parts have been successfully thinned to 70um – 90um. As previously mentioned, only Rev C FPGA SEE data is provided in this document.

Figure 4: Ultra Tec ASAP-1 device preparation system

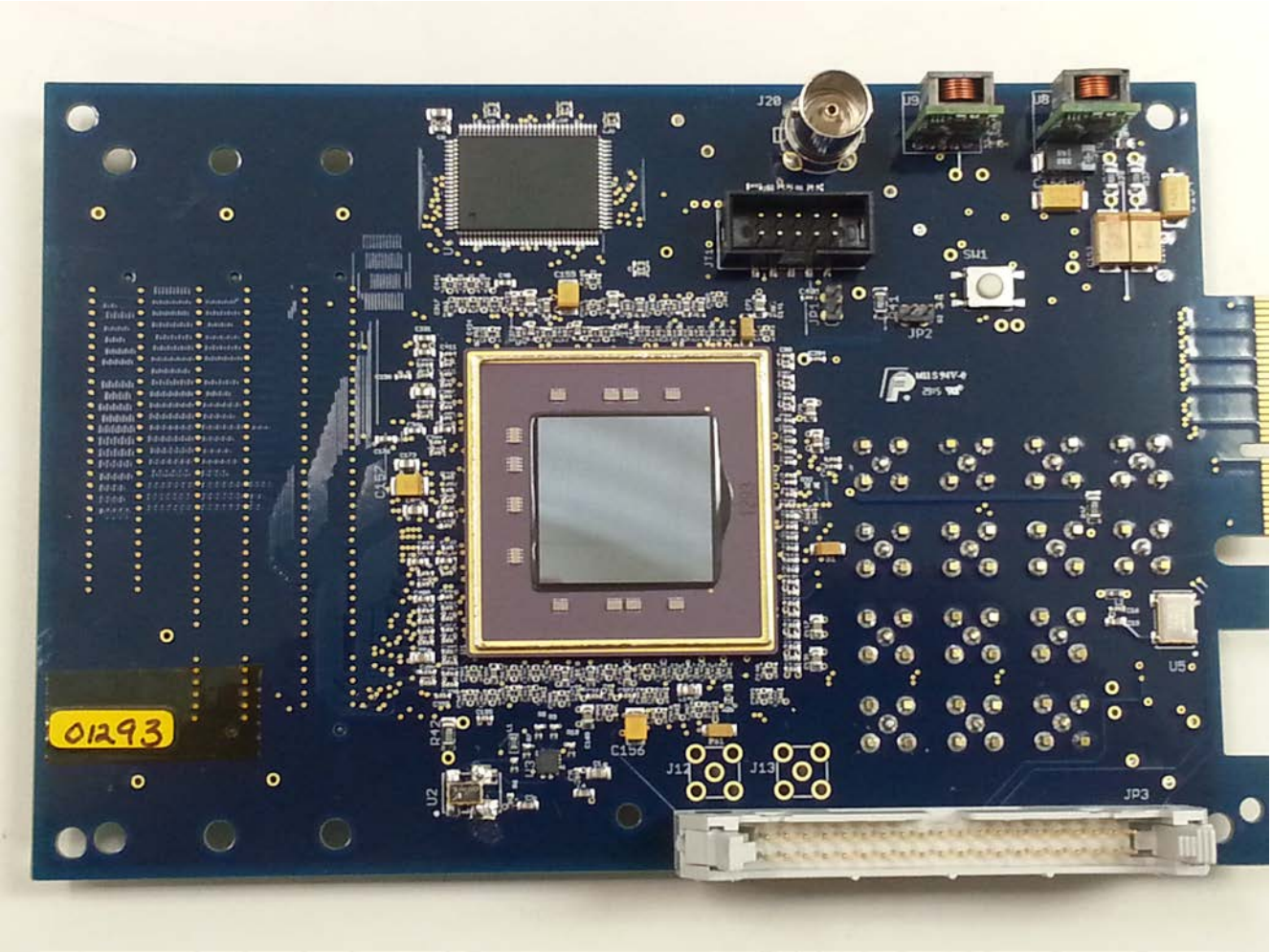


Figure 5: Top side of DUT daughter board with de-lidded and thinned DUT.

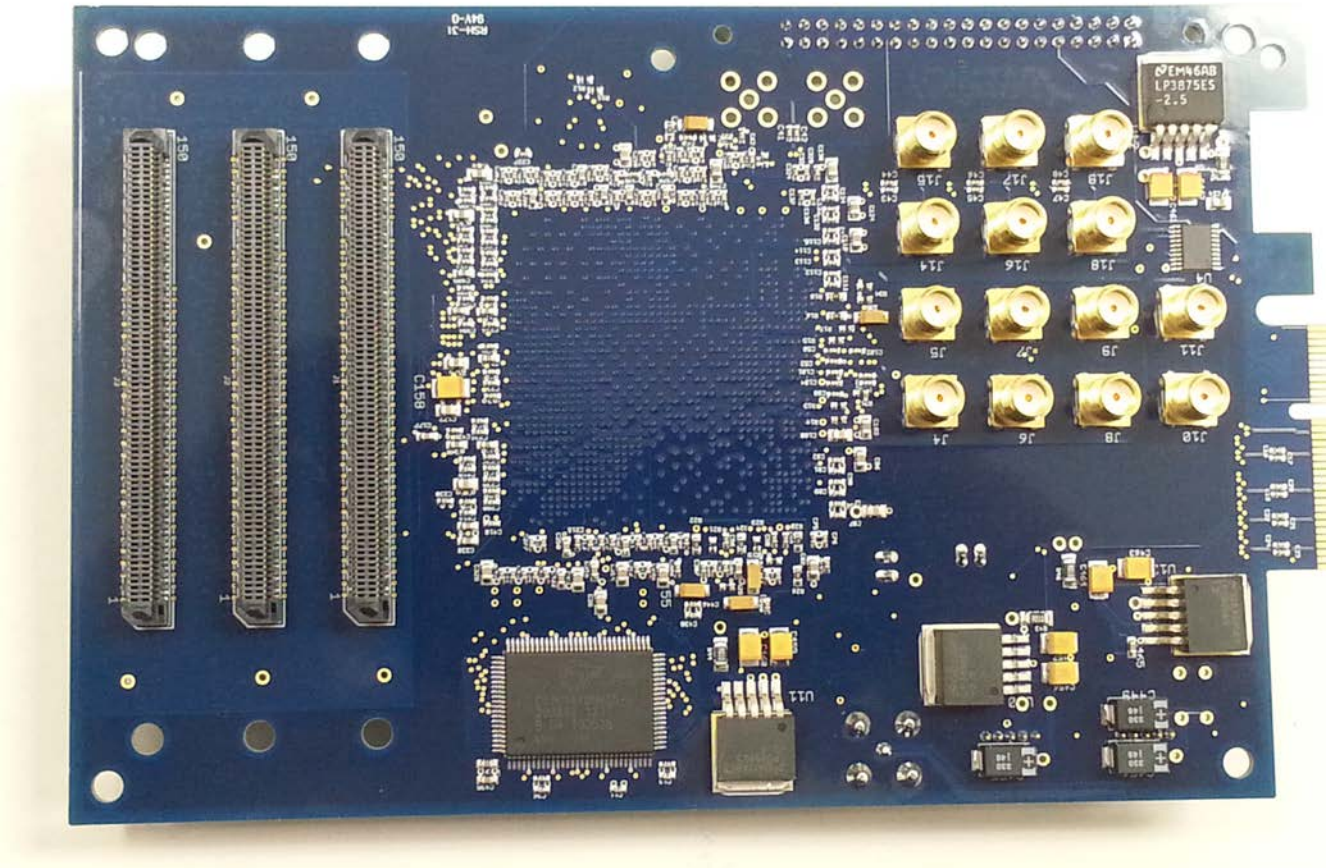


Figure 6: Bottom side of DUT daughter board with de-lidded and thinned DUT.

4. TEST PROCEDURES AND BEST PRACTICES

4.1 Functional Control

Types of DUT functional input control: clocks, resets, and data inputs.
Concerns and Challenges:

- Synchronizing inputs and managing skew between inputs. Challenging with high frequencies.
- Operating the device in a realistic manner:
  - Do not over-load the device with unrealistic stimulus during radiation testing. If the device is operating in states that would never occur, then radiation data will not be characteristic.
  - Do not under-load the device during radiation testing. If the device is underperforming, this means that a large amount of circuitry is not operating. This produces operational states with a large amount of logic masking; consequently, radiation data will not be characteristic.

4.2 Monitoring Functionality

The following are general practices for monitoring FPGA functionality during heavy-ion testing.

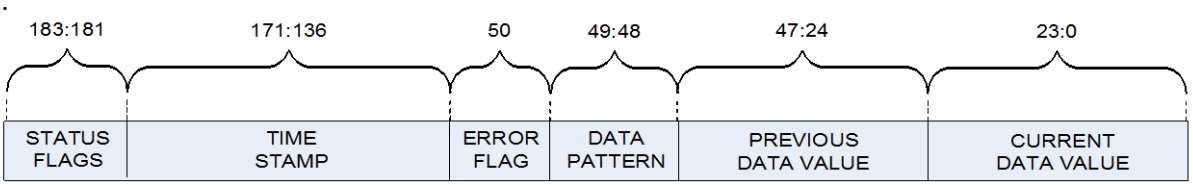
- Compare DUT outputs to expected values

  - Visually (only recommended as a supplement); i.e., watching the error indication on the error detection equipment (e.g., logic analyzer);
  - Custom comparison circuitry (Low Cost Digital Tester: LCDT).
- Differentiate upset types: e.g., clock tree SET, flip-flop (DFF) SEU, combinatorial logic (CL) captured SET, or configuration faults.
- Count SEUs (upset statistics): After the upsets have been detected and differentiated, they need to be counted. The higher the number of upsets, the better the statistics.

4.3 Automated Data Capture and Messaging

The following are general practices for data capture during heavy-ion testing.

- Reliable data capture:
  - Follow synchronous design rules – which include how to capture asynchronous signals.
  - Determine minimal sampling frequency (when applicable).
  - Understand the limitations of the automated test equipment with respect to the DUT (e.g., memory-storage space, I/O voltage, I/O interface, and speed).
- Once erroneous data are captured, they should be packaged and stored (e.g., sent to a host PC). Example of package fields:
  - Timestamp,
  - Expected value, and
  - Received value.



Field	# of Bits	Description
Current Value	24	Current captured data (cycle N)
Previous Value	24	Previous captured data (cycle N-1)
Data Pattern	2	Unused: data pattern is always checkerboard
Error Flag	1	Unused
Time Stamp	32	Cycle counter. Must multiply by the DUT frequency to convert to time. Used to determine error burst sequences
Status	3	Indicates type of error record: "001" is a timeout – one of the shift clocks not detected "011"Out of timeout – all shift clocks are recovered "000" Error or non-error – current value does not equal previous value "010" Debug check – command was sent to check value settings

Figure 7: Sample Message from the LCDT to the Host PC. Message describes the SEU and Includes a Timestamp

4.4 Monitoring DUT Power and SEL Investigation

The following are general practices for monitoring DUT power.

- Use of power supply monitors.
- Use of an automated monitor/capture system is beneficial. Provides the ability to store and perform post processing on power data. Great for identifying particular error signatures.
- Power glitching or Single Event Latch-up (SEL) can cause the system to cease operation or be damaged. Hence it is best practice to separate test vehicle power from DUT power.
- It is also ideal to have current limiting circuitry for the test vehicle and the DUT.

4.5 Investigating SEFIs

We look for particular error signatures to determine SEFI occurrence:

- Read-back of configuration returns a fail.
- Unable to connect to the device to read-back – assume problem in the configuration interface.
- Global SEFIs in functional logic – not performed during static read-back.
  - Reset correction: clock tree or reset tree (global routing).

P_{SEFI} is calculated using equation (4). Test until upset occurs and record the fluence.

$$\sigma_{SEFI} = \frac{1}{(fluence)} \tag{4}$$

The following sections describe the construction of the LCDT including communication interfaces with the DUT and user PCs.

5. TEST HARDWARE (TEST SYSTEM)

In this study, a test system refers to the NEPP (NASA Goddard developed) LCDT3 and a custom daughter card containing the DUT.

5.1 Pictures of the Test System

Figure 8 and Figure 9 are pictures of the RTG4 populated DUT board connected to the LCDT tester.

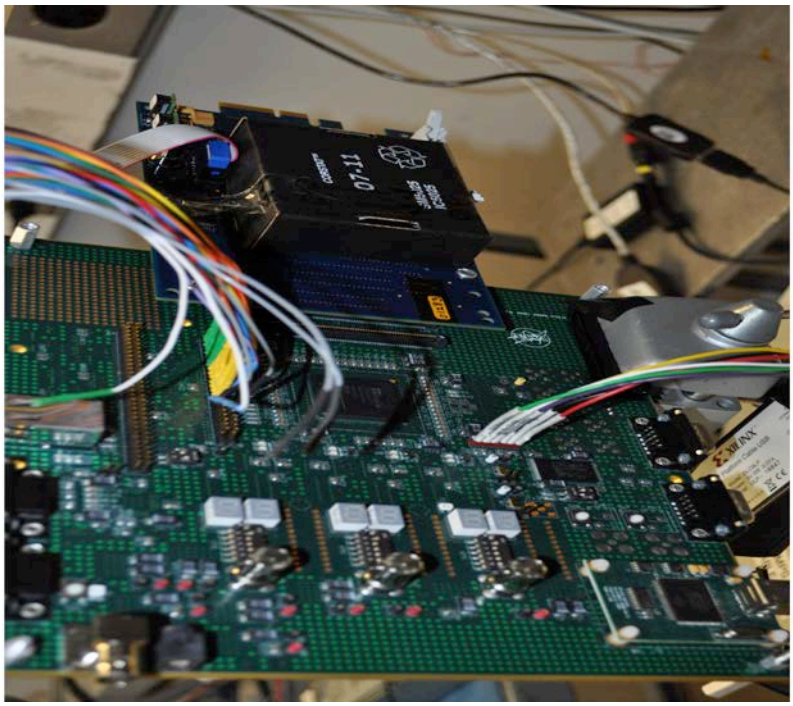


Figure 8: Test Setup - Connected LCDT3 and Daughter Card (1)

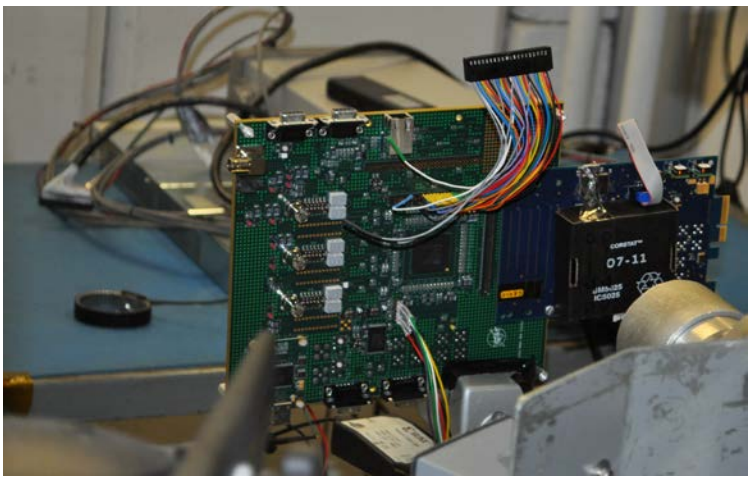


Figure 9: Test Setup - Connected LCDT3 and Daughter Card (2)

5.2 LCDT Architectural Overview

As previously mentioned, the test system consists of a Mother Board (FPGA Based Controller/Processor) and a daughter board (containing DUT and its associated necessary circuitry). The DUT controller/processor is instantiated as a sub component within the LCDT. A block diagram is illustrated in Figure 10.

The objective of this DUT controller/processor is to supply inputs to the DUT device and perform data processing on the outputs of the DUT. The LCDT communicates with a user controlled PC. The

user PC interface is LabVIEW. LabVIEW code was designed to send user specified commands to the motherboard and receive information from the motherboard. Please see Documents: “LCDT” and “General Tester” for further information concerning the LCDT functionality. The LCDT is connected to the DUT as shown in the following block diagram.

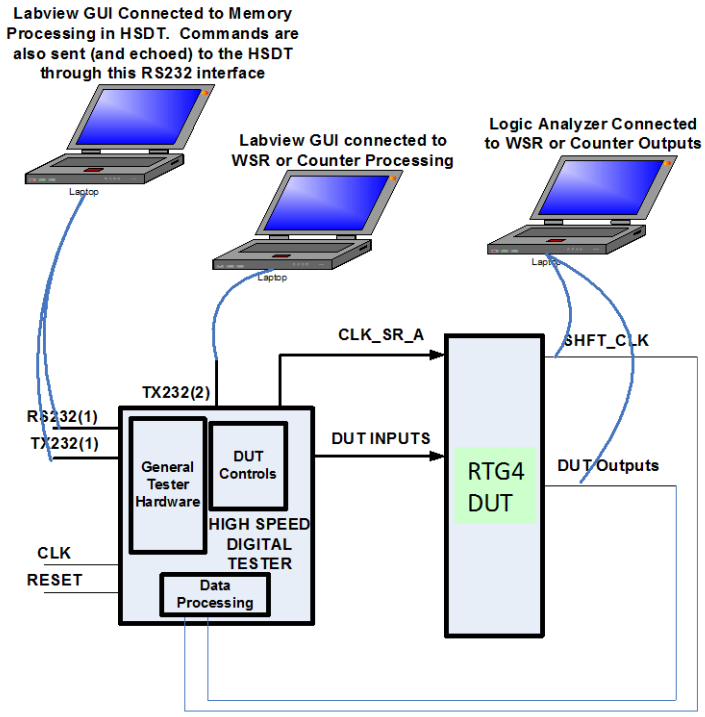


Figure 10: System Level Tester Architecture for the DUT configured as a counter.

5.2.1 RS232 communication from the LCDT to the Host PC

All RS232 communication from the LCDT to the host PC is prefaced with a header. Information from the LCDT to the Host PC is one of the following listed in Table 1: an alive-timer, a command echo, or an Error Record.

Table 1: A list of the LCDT to Host PC RS232 Header bytes. Only the LCDT uses header information. The host PC sends pure commands to the LCDT without headers.

Header	Description
00 FA F3 20	Alive Header No data bytes follow (i.e. only the header is sent from the LCDT to the PC)
00 FA F3 22	Command Echo. 4 data bytes follow that represent the command that was previously sent from the Host PC to the LCDT.
00 FA F3 21	Data Error Record: 23 bytes follow.

5.3 RS232 communication From the Host PC to the LCDT

Communication from the host PC to the LCDT does not contain a header. Information sent from the host PC to the LCDT are commands and are all 4 bytes in length The interface is controlled by a user GUI designed with LabVIEW software.

5.3.1 User GUI

Commands are sent by typing specific values into LabVIEW fields or controlling LabVIEW on/off buttons listed on the screen.

5.3.2 User Interface and Command Control

The user controls the tests via a LabVIEW interface running on a PC. The PC communicates with the LCDT with a RS232 serial link. The format of communication is a command/Data 4 byte word.

Table 2 : Summary of Commands Used in DUT Tests

Command #	Command	D0	D1	D2	Description
01	Reset LCDT	n	n	n	Resets Tester and DUT (stops DUT clocks and makes DUT reset active)
03	Reset Counter	N	N	n	RESETS Counters without resetting tester circuitry (only used in counter tests)
02	Start Testing	N	N	N	Starts the DUT clocks
A0	Clock divider	y	y	n	D0 (LSB) and D1 (MSB) are the Clock frequency divider of 100mhz. The synthesized LCDT3 clock output is sent to the DUT. This signal is the DUT's system clock. Default=0 (no division)
91	Pattern Selection	y	n	n	Only used in WSR tests: D0 = 0=> all 0's D0 =1 => all 1's D0 >1 => checkerboard
06	WSR Halt command	n	n	n	Stops the DUT clocks. Does not perform a reset.

6. DUT TEST STRUCTURES AND DYNAMIC ACCELERATED TESTING

In this study, we started with simple test structures; increased complexity per test structure; study trends; and then tried to make sense out of the convoluted data obtained from complex test structures.

Test Structure Considerations Taken from the NASA Electronics Parts and Packaging (NEPP) FPGA SEU Test Guidelines:
https://nepp.nasa.gov/files/23779/fpga_radiation_test_guidelines_2012.pdf .

Referencing the FPGA SEU Test Guidelines manual, for simple test structures, they should have the ability to flush SEU's (post-detection)… i.e., test circuits should have the ability to keep working after an SEU occurs to increase statistics of each beam run. This helps to increase statistics during testing. In addition, the tester (for these simple test structures) should be robust enough to resynchronize to new DUT expected values caused by SEUs; i.e., expected values should be dynamic based off of impact of SEUs. These statements are not necessarily implementable in a complex system. However, in shift registers and counters; i.e., flushable test systems, it is feasible.

6.1 Challenges for Testing

Microsemi computer aided design (CAD) software is new:

- Place and route is not optimal yet. Hence, it is difficult to get high speed without manual placement.
- Early versions of the CAD tools did not handle some components properly: e.g., asynchronous resets were not tied correctly to components, DSP blocks (HMACCs) had bugs, Memory blocks did not have adequate power ties (such that current would rise during testing), etc. With CAD tool bugs, some test results are deemed useless or expected to change with upgraded CAD tools. This wastes test time.
- Microsemi reports that devices show TID tolerance up to 160 krad(Si). Although, when testing with heavy-ions, dose tolerance will be much higher. TID limits the amount of testing per device. The number of devices is expensive and is limited for radiation testing. A large variety of tests are required.

Current consortium participants:

- NEPP
- Aerospace
- JPL
- Potential: ESA

6.2 Overview of DUT Test Structures

Table 3 is an overview of the DUT test structures that were analyzed in heavy ion testing. Some of the test structure designs were created with variations for trend analysis.

Table 3: Overview of Test Structures

Test Structure	Frequency Range	SEU Flow-Through (Flushable)
Global routes	2 KHz – 150 MHz	N/A
Shift registers (WSR)	100 KHz – 160 MHz	Yes
Counters (Count Array): Parallel independent counters	5 MHz – 100 MHz	Yes
Finite impulse response (FIR) (chain of DSP 18x18 multiplier accumulate blocks (HMACC))	1 MHz - 100 MHz	Yes

6.3 Windowed Shift Registers (WSRs)

6.3.1 General Operation

A windowed shift register (WSR) is based off of the traditional shift register used for SEU testing. The difference between a WSR and a traditional shift register is that the last 4 stages of the shift register are captured into a 4-bit window. This helps with signal integrity and reliability of data capture between the DUT and the tester. Figure 11 illustrates a WSR with and without inverter logic between DFF stages.

A variety of WSR chains were tested and analyzed for SEE susceptibility to heavy ions. WSR variations are based off of the number of combinatorial logic blocks between each DFF stage; the number of DFF stages per chains; DFF SET filter usage; and how the WSR DFFs are connected to global routes. In Figure 11, WSR_0 indicates a WSR with no combinatorial logic gates. WSR_8 indicates a WSR with 8 levels of combinatorial logic gates between each DFF stage. In essence, the number associated with a WSR indicates the number of inverters inserted between each DFF stage. All stages within one WSR chain have equivalent circuits.

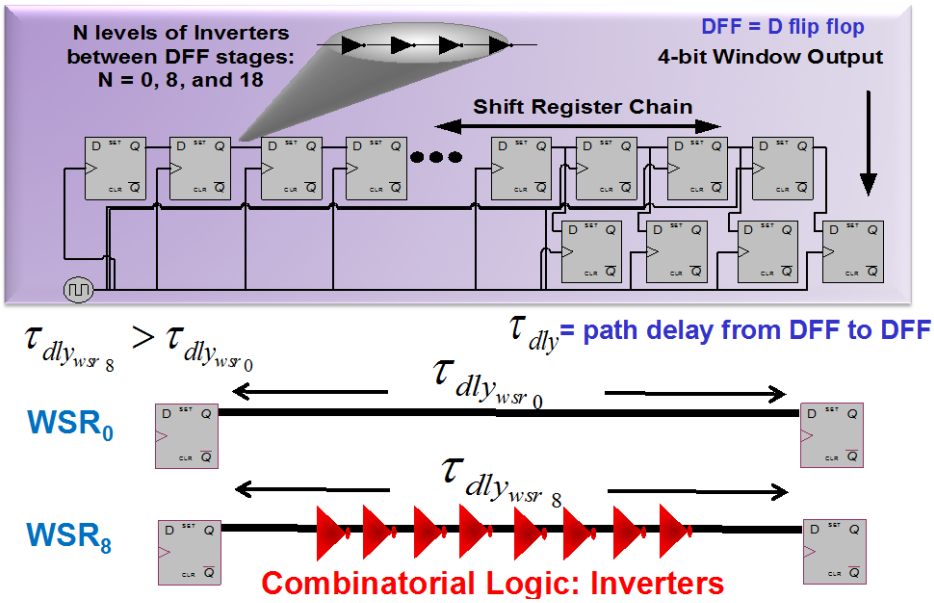


Figure 11: WSR Chains. WSR variations are based off of the number of combinatorial logic blocks between each DFF stage; the number of DFF stages per chains; and how the WSR DFFs are connected to global routes. In this figure, WSR_0 indicates a WSR with no combinatorial logic gates. WSR_8 indicates a WSR with 8 levels of combinatorial logic gates between each DFF stage.

Figure 12 is a timing diagram that illustrates WSR operation under normal conditions.

!

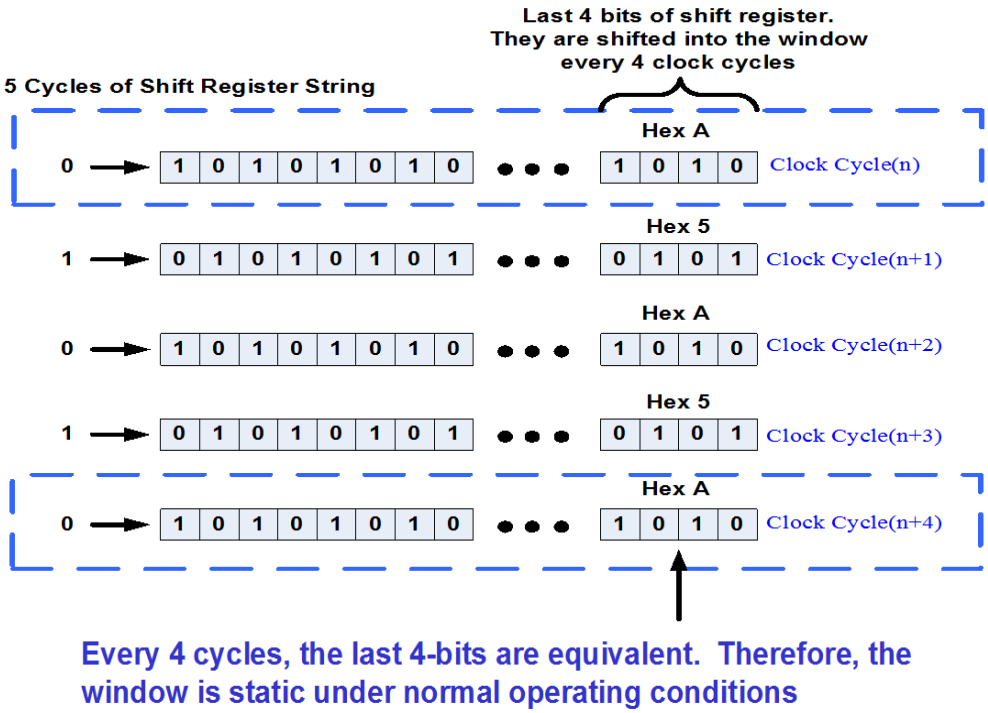


Figure 12: WSR Functional Behavior

6.3.2 WSRs and LCDT Requirements

The following are requirements for LCDT control of the WSR chains:

- LCDT must supply DUT clocks. Clock frequency is command driven by the user and physically controlled by the LCDT.
- Active high Resets (one per WSR chain) – RST_0, RST_4, RST_8, RST_{16}.
- 2-bit MUX control (see Table 4) to select WSR data input pattern:

Table 4: MUX Control Patterns

MUX: Bit1 Bit0	Data Pattern
00	All0's
01	All 1's
10	Checkerboard
11	Checkerboard

6.3.3 WSR SEU Data Monitoring and Capture

- Heartbeat monitoring:
  - DUT heartbeat output will be ¼ the speed of the DUT clock input.
  - DUT heartbeat is oversampled by >4x of the heartbeat speed by the LCDT and is passed through a metastability (synchronizer) circuit. Output of the heart detect metastability circuit is edge detected (rising). The edge is under watchdog to make sure that the system hasn't died.
- Expected data monitoring:
  - Because the window should be static, any change in the window is detected and reported to the host PC. LCDT oversamples the DUT output window in order to potentially detect change.
- Each WSR window is monitored for data change. Data change signifies SEU.
- SEUs are differentiated: single bit, versus stuck, versus burst upsets (global).

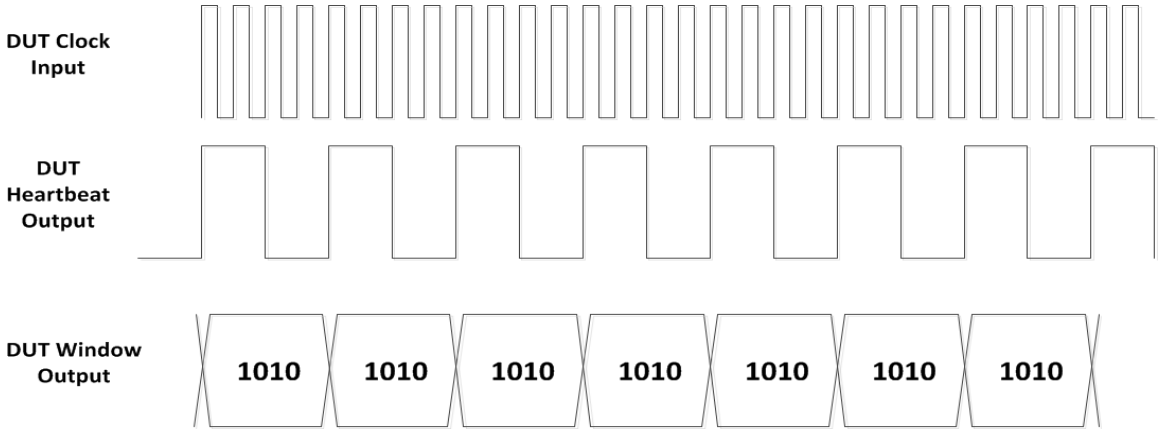


Figure 13: WSR output under normal operation

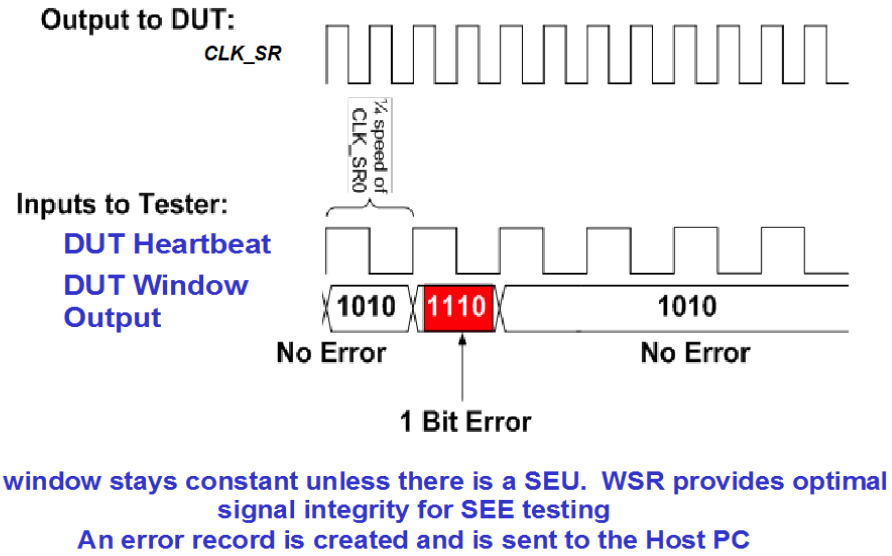


Figure 14: WSR Operation with SEU

6.3.4 WSR Error Reporting Record

Table 5: Error record for First Round of WSR Testing

Record Bit Position	Data Field
15:0	Bad data of current clock cycle
31:16	Data last clock cycle
57:56	Pattern Selection: 00 All 0's 01 All 1's 10 Checkerboard

	11 Checkerboard
60	Chain0 PLL lock (1 – indicates locked; 0 indicates unlocked). Only used for PLL WSR tests.
65	Unused (no PLL for Chain1)
66	Chain2 PLL lock (1 – indicates locked; 0 indicates unlocked). Only used for PLL WSR tests.
67	Chain3PLL lock (1 – indicates locked; 0 indicates unlocked). Only used for PLL WSR tests.
64	Chain0 Heartbeat (indicates if a chain's heart beat is alive): 0 indicates alive, 1 indicates dead)
65	Chain1 Heartbeat (indicates if a chain's heart beat is alive): 0 indicates alive, 1 indicates dead)
66	Chain2 Heartbeat (indicates if a chain's heart beat is alive): 0 indicates alive, 1 indicates dead)
67	Chain3 Heartbeat (indicates if a chain's heart beat is alive): 0 indicates alive, 1 indicates dead)
95:80	Frequency selection for WSR_0
177:146	Timer – clock cycles (granularity of 1 timer clock cycle is equal to DUT operational speed)
183:181	Record indicator: 000: debug 010: SEU error record 100: In timeout (one of the heart beats has died) 101: Out of timeout (one of the heart beats was dead and now has come alive)

6.3.5 Post Processing of LCDT WSR Data Analysis for First Round of Testing

Post processing is performed on all error records (see previous section).

As previously mentioned, error signatures are differentiated between:

- 1-bit errors within a window.
- Multiple-bit errors within a window.
- Burst Errors:

- Clock upsets: error signatures with WSRs generally last nanoseconds to microseconds.
- Configuration-bit upset: error signatures will appear as a stuck fault.

Timestamps and window data values are used to differentiate error signatures during the post-processing phase.

SEU cross sections are calculated for each error signature. They are calculated by counting the number of bits upsets within a window as in (5). Consecutive window upsets are considered part of a burst and are not part of a single bit upset.

$$\sigma_{WSRseu} = \frac{\#WSRerrors}{(fluence)*\#WSR_DFFs} \quad (5)$$

6.4 Global Routes and Microsemi RTG4 Clock Conditioning Circuit (CCC)

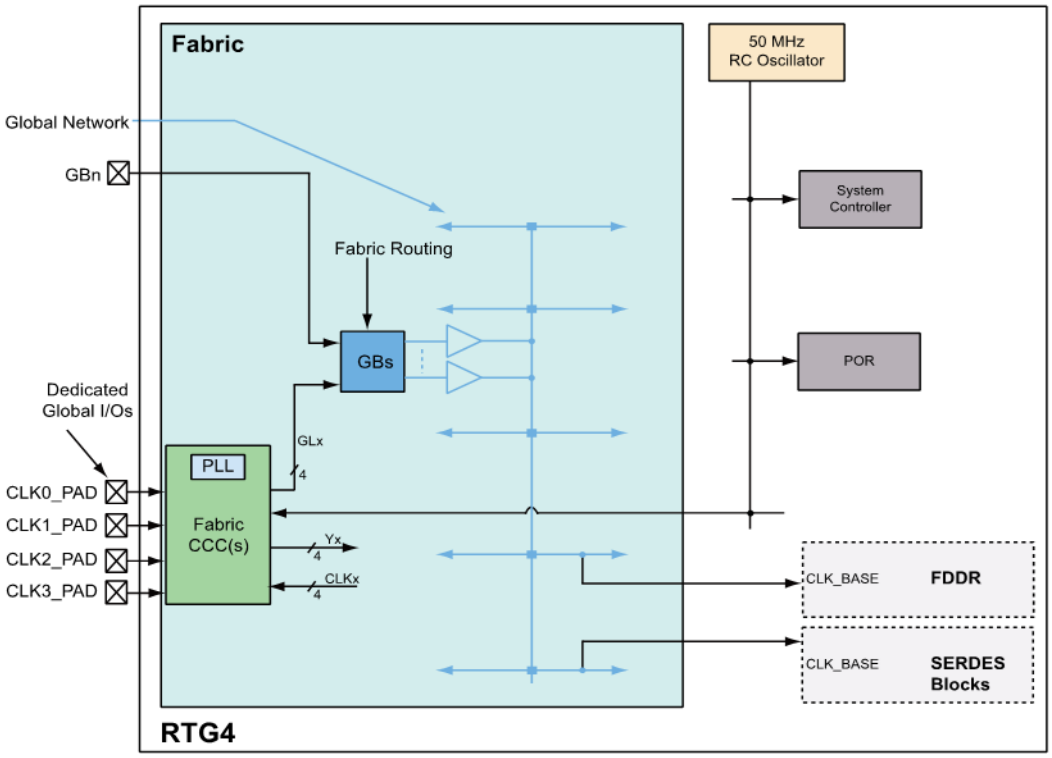


Figure 15: Microsemi clock conditioning circuit. FDDR: Memory Double Data Rate Interface Control; SERDES: Serial-De-serializer; POR: Power on reset; PLL: Phase locked loop; GBn: global network; DGBIO: dedicated global I/O pad

A CLKBUF is a RTG4 internal buffer that connects to a hardened global route. Input to the CLKBUF can only be a dedicated global I/O pad (DGBIO). A CLKINT is a RTG4 internal buffer that connects to a hardened global route. Input to a CLKINT can come from fabric or any input.

CLKINTs are generally used in conjunction with Microsemi clock conditioning circuits (CCC). A CCC block is illustrated in Figure 15.

A variety of designs were created to analyze different global circuit usage.

6.4.1 Resets

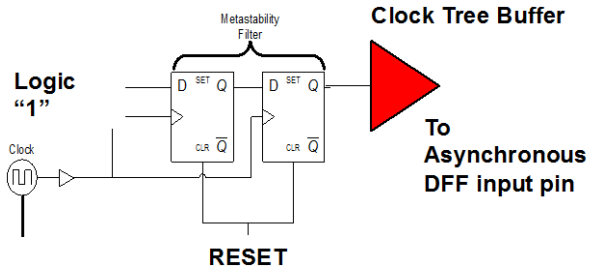


Figure 16: Asynchronous assert synchronous de-assert reset

Asynchronous assert synchronous de-assert (AASD) is the traditional method of reset implementation in NASA driven systems. The AASD reset is illustrated in Figure 16. This is a requirement for the protection of a mission in case of loss-of-clock. Synchronization is performed prior to clock tree connection. The AASD global reset is connected to the asynchronous pin of each DFF; however, it is synchronized to the clock and is hence synchronous. Rev B tests implemented pure AASD via asynchronous reset tree connections to DFFs. AASD was not used in Rev C designs. Rev C designs use a pure synchronous reset.

6.5 DUAs Based on WSR and Global Route Variations – 1st Round of RTG4 Rev C Heavy Ion Testing

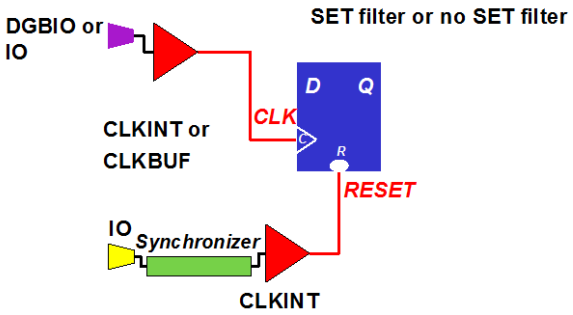


Figure 17: General schematic showing the potential variations in clock connections. The DFF can be configured to have SET filters at their data input pin or not to have SET filters.

In the first round of testing, Rev C WSR designs were varied by combinatorial logic block insertions and clock connections. Clocks are supplied to the DUT from the LCDT tester output to a DUT input pin. The DUT input pin (used for the clock) was either a dedicated clock I/O (DGBIO) or a normal I/O. All clocks are placed on a clock tree. Clocks are place on a clock tree via a RTG4 CLKBUF or CLKINT buffer component. A CLKINT buffer is a hardened clock tree connection via a

buffer for normal I/O pins. A CLKBUF is a hardened clock tree connection via a buffer for DGBIO. All WSR DFF data input pins either have the DFF SET filter turned on or turned off. Figure 17 is a schematic that illustrates potential variations for clock to WSR connections. The following provides more detail per DUT WSR designs used in the 1st round of Rev C heavy ion testing.

6.5.1 Design A: 4 Clock 4 Reset DUA

The "4 Clock 4 Reset" design has four chains: WSR_0 (no inverters between DFF stages), WSR_4 (four inverters between DFF stages), WSR_8 (8 inverters between DFF stages), and WSR_{16} (16 inverters between DFF stages). All chains have 800 DFF stages each. All clocks are connected to CLKINT. Only WSR_0 has a DGBIO. Each WSR chain has it's own synchronized reset. Rev B used a mixture of AASD and pure synchronous resets. Rev C used only pure synchronous resets. No DFF SET filters were configured in Design A. The schematic for Design A is illustrated in Figure 18.

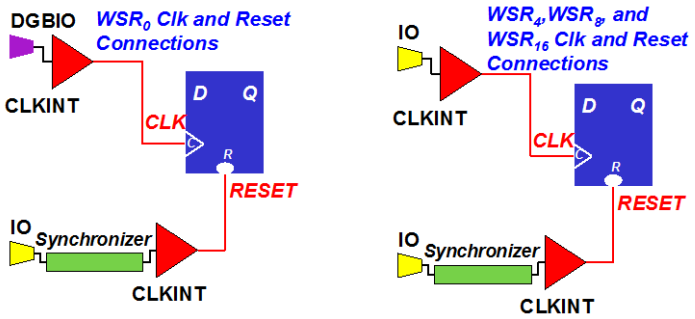


Figure 18: Design A: 4 Clock 4 Reset WSR to Clock connection.

6.5.2 Design B: 4 Clock 4 Reset with DFF SET Filters DUA

The "4 Clock 4 Reset with DFF SET Filters" design has four WSR chains: WSR_0, WSR_4, WSR_8, and WSR_{16}. All WSR chains have 800 DFF stages each. All clocks are connected to CLKINT. Only WSR_0 has a DGBIO. Each WSR chain has its own synchronized reset. Rev C used only pure synchronous resets. DFF SET filters were configured in Design B. The schematic for Design B is illustrated in Figure 18. The only difference between Design A and Design B is the usage of SET filters.

6.5.3 Design C: 4 clk 4 rst Direct CLKBUF DUA

The ": 4 clk 4 rst Direct CLKBUF" design has four WSR chains: WSR_0, WSR_4, WSR_8, and WSR_{16}. All chains have 800 DFF stages each. There are four clocks and each clock is connected to CLKBUF. Each WSR chain has its own synchronized reset. The schematic for Design C is illustrated in Figure 19.

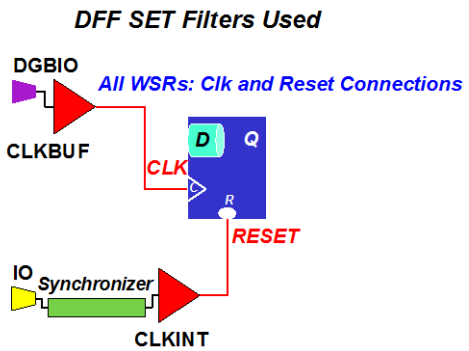


Figure 19: Design C: All WSRs are controlled by DGBIO/CLKBUF. All WSR chains contain DFF SET filters.

6.5.4 Design D: Long Shift Register DUA

The "Long Shift Register" design has 4 chains of WSR_0 (i.e., no inverters between DFF stages): $Chain_0$, $Chain_1$, $Chain_2$, $Chain_3$. Each chain has 20,000 DFF stages each. All clocks are connected to CLKINT. Only 1 chain has a DGBIO connection. The other 3 chains are connected to normal I/O. No resets are used. No DFF SET filters were configured in Design D. The schematic for Design D is illustrated in Figure 20.

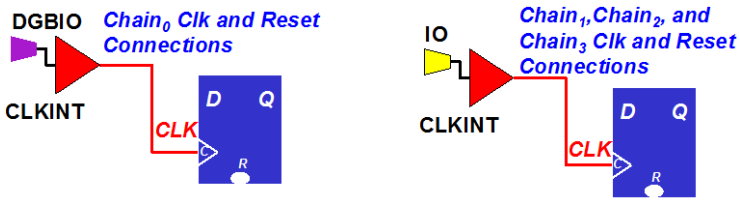


Figure 20: Design D: Long WSR no DFF SET filters.

6.5.5 Design E: Long Shift Register with DFF SET Filters DUA

The "Long Shift Register with DFF SET Filters" design has 4 chains of WSR_0 (i.e., no inverters between DFF stages): $Chain_0$, $Chain_1$, $Chain_2$, $Chain_3$. Each chain has 20,000 DFF stages each. All clocks are connected to CLKINT. Only 1 chain has a DGBIO connection (chain0). The other 3 chains are connected to normal I/O (chain1, chain2, and chain3). No resets are used. DFF SET filters were configured in Design E. The schematic for Design E is illustrated in Figure 20. The difference between Design D and Design E is that Design E has DFF SET filters turned on.

6.5.6 Design F: Large shift register CCC with DFF SET Filters DUA

The "Large shift register CCC with DFF SET Filters" design has 4 chains of WSR_0 (i.e., no inverters between DFF stages): $Chain_0$, $Chain_1$, $Chain_2$, $Chain_3$. Each chain has 20,000 DFF stages each. All chains are connected to a CCC block. All WSR chains use DFF SET filters. No resets are connected to the DFFs in the WSR chains. The schematic for Design F is illustrated in Figure 21.

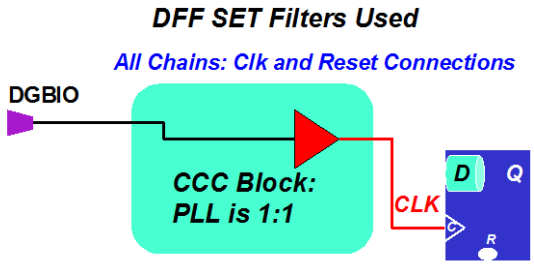


Figure 21: Design F: Large shift register CCC. All DFFs are connected to a clock tree that stems from the RTG4 CCC block. No resets are connected to the DFFs in the WSR chain.

6.5.7 Summary of WSR – Global Route DUA Variations 1st Round of Rev C Heavy Ion Testing

Prior sections described in detail the variations to WSR designs and their global route connections. Table 6 is a list that summarizes all of the WSR designs analyzed during the 1st round of Rev C heavy ion testing.

Table 6: List of WSR Designs for 1st Round Rev C Heavy Ion Testing

Design	Design Name	CLK I/O Pin	Clock Buffer	Reset	Number of Stages	SET Filter
A	4 CLK 4 RST	WSR_0: DGBIO Others: I/O	All CLKINT	All CLKINT	800	OFF
B	4 CLK 4 RSTFILTER	WSR_0: DGBIO Others: I/O	All CLKINT	All CLKINT	800	ON
C	4 CLK 4 RST Direct CLKBUF	All DGBIO	All CLKBUF	All CLKINT	800	ON
D	Large Shift Register	$Chain_0$: DGBIO Others: I/O	All CLKINT	None	20,000	OFF
E	Large Shift Register FILTER	$Chain_0$: DGBIO Others: I/O	All CLKINT	None	20,000	ON
F	Large Shift Register CCC	All DGBIO	All Through CCC	None	20,000	ON

6.5.8 WSR and Global Route Variations Data Capture, Error Records, and Data Processing

WSR designs A-F, as described in section 6.5.7 and Table 6, use the same data capture, error records, LCDT control, and data processing as described in sections: 6.3.2, 6.3.3, 6.3.4, and 6.3.5.

6.6 PLL DUAs Based on WSR and Global Route Variations – 2nd Round of RTG4 Rev C Heavy Ion Testing

The WSR-Global route investigation during the 2nd round of heavy ion testing focused on PLL susceptibility. Although the Microsemi RTG4 has a variety of PLL configurations for the user to choose from, we were limited by heavy ion beam time and selected a limited set of PLL configurations to investigate. Each DUT contains four WSR chains. Each WSR chain is connected to a different type of Clock connection. All WSR chains are WSR_0 (no inserted inverters between DFF stages).

- Chain0: DGBIO connected to a CCC PLL. DGBIO is 50MHz and PLL CCC output (CLKINT buffer) is configured to operated at 120MHz. Hence WSR chain0 internal operation is 120MHz. The CCC PLL is configured to have internal feedback. However, it is not in TMR mode.
- Chain1: DGBIO is directly connected to CLKBUF buffer. DGBIO runs at 120MHz and hence the CLKBUF clock tree is 120MHz. WSR chain1 operates internally at 120MHz. No PLL is used in this chain and the CCC block is bypassed.
- Chain2: DGBIO connected to a CCC PLL. DGBIO is 50MHz and CCC output (CLKINT buffer) is configured to operated at 120MHz. Hence WSR chain2 internal operation is 120MHz. The CCC PLL is configured to have internal feedback. It is not in TMR mode.
- Chain3: There is no DGBIO connection. The clock is generated using the RTG4 internal oscillator (OSC). The OSC inherently runs at 50MHz. The OSC is connected to a CCC PLL with an output of 120MHz. The output of the CCC (CLKINT buffer) runs at 120MHz and hence the WSR chain3 operates at 120MHz. The CCC PLL is configured to have internal feedback. However, it is not in TMR mode.

The Microsemi Libero CAD tool was used to instantiate the WSR PLLs (Chain0, Chain2, and Chain3). The following figures (Figure 22, Figure 23, Figure 24, and Figure 25) depict the CAD tool setup for each of the instantiations. Two windows of control are necessary: a front panel (Figure 22) that controls the frequency synthesis; and a 2nd tab (Figure 23, Figure 24, and Figure 25) that controls the details of the PLL setup (such as feedback, delay taps, clock connections, etc.).

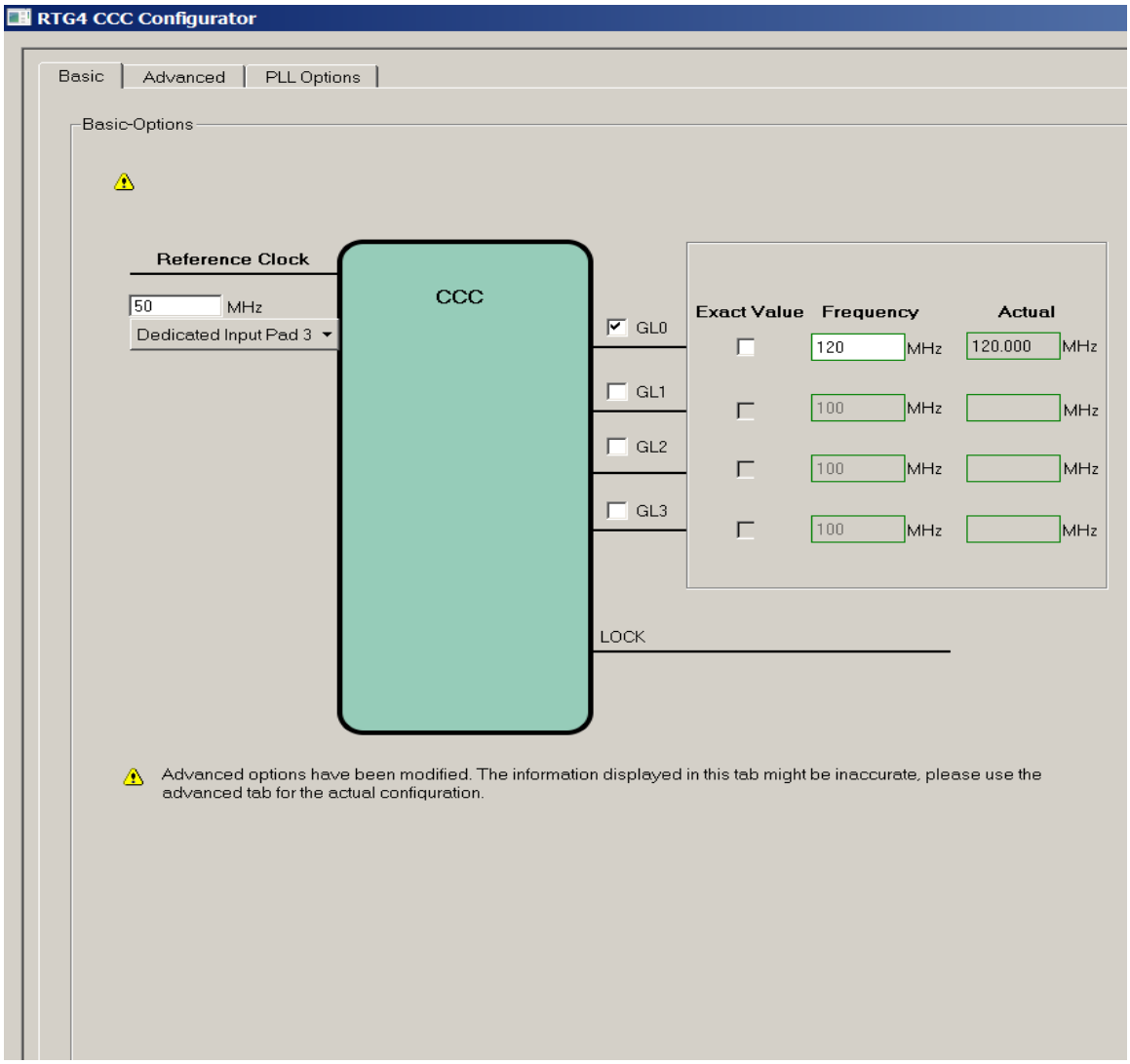


Figure 22: Front panel of CCC configuration in Microsemi Libero CAD tool. 50MHz input from a DGBIO with 120MHz output to a CLKINT buffer

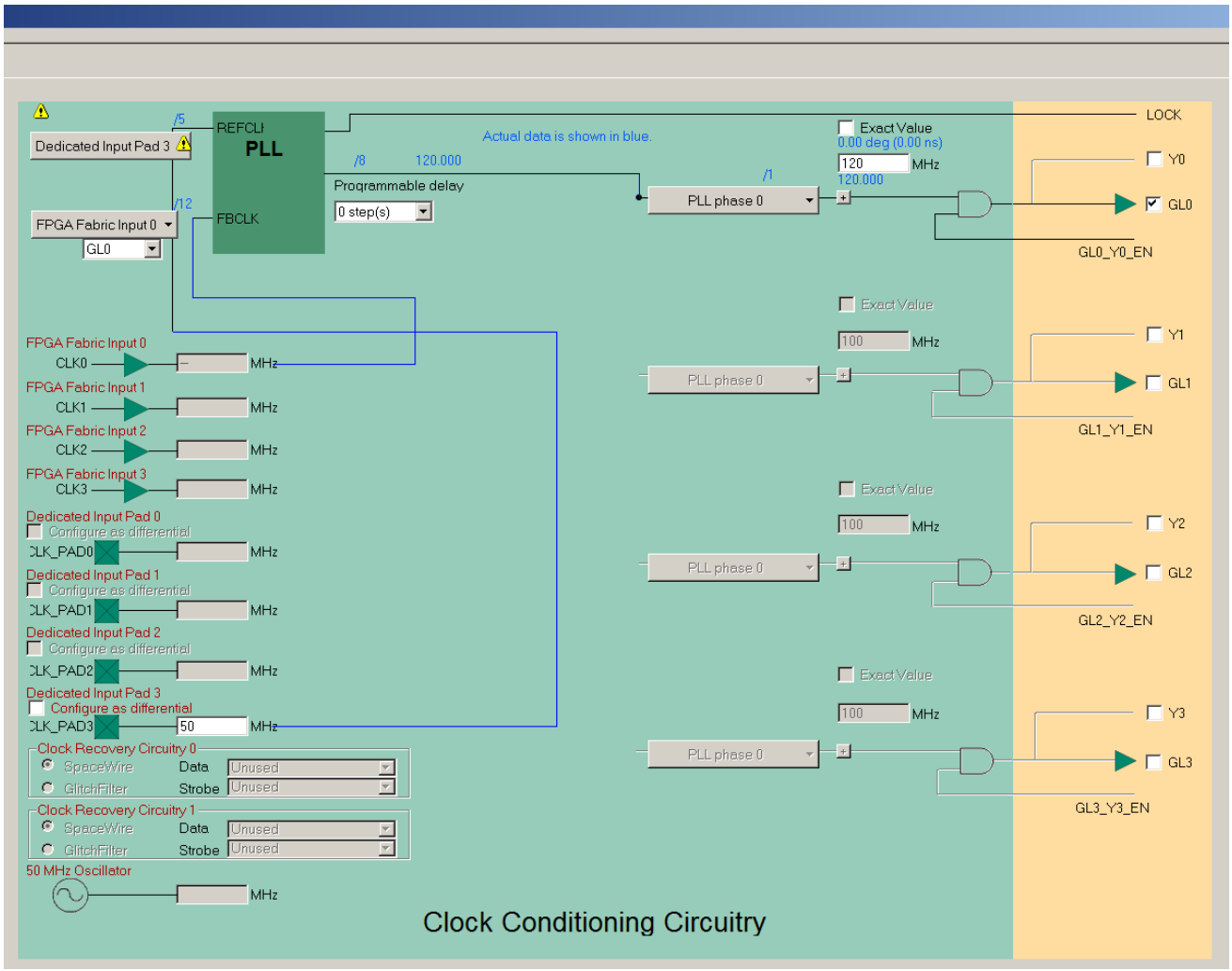


Figure 23: 2nd tab for CCC configuration with internal feedback in Microsemi Libero CAD tool. Chain0 in 2nd round heavy ion testing.

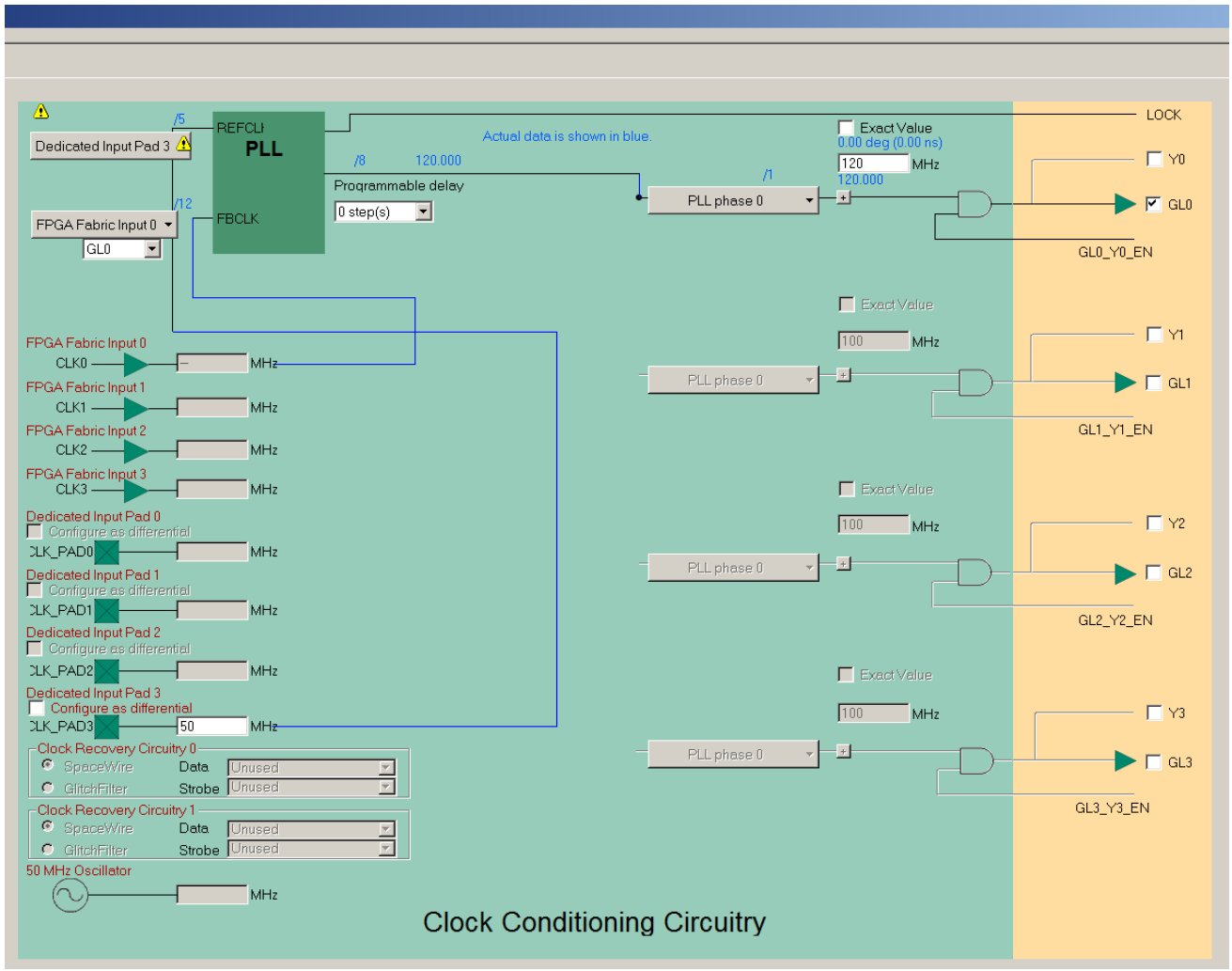


Figure 24: 2nd tab for CCC configuration with external feedback in Microsemi Libero CAD tool. Chain2 in 2nd round heavy ion testing.

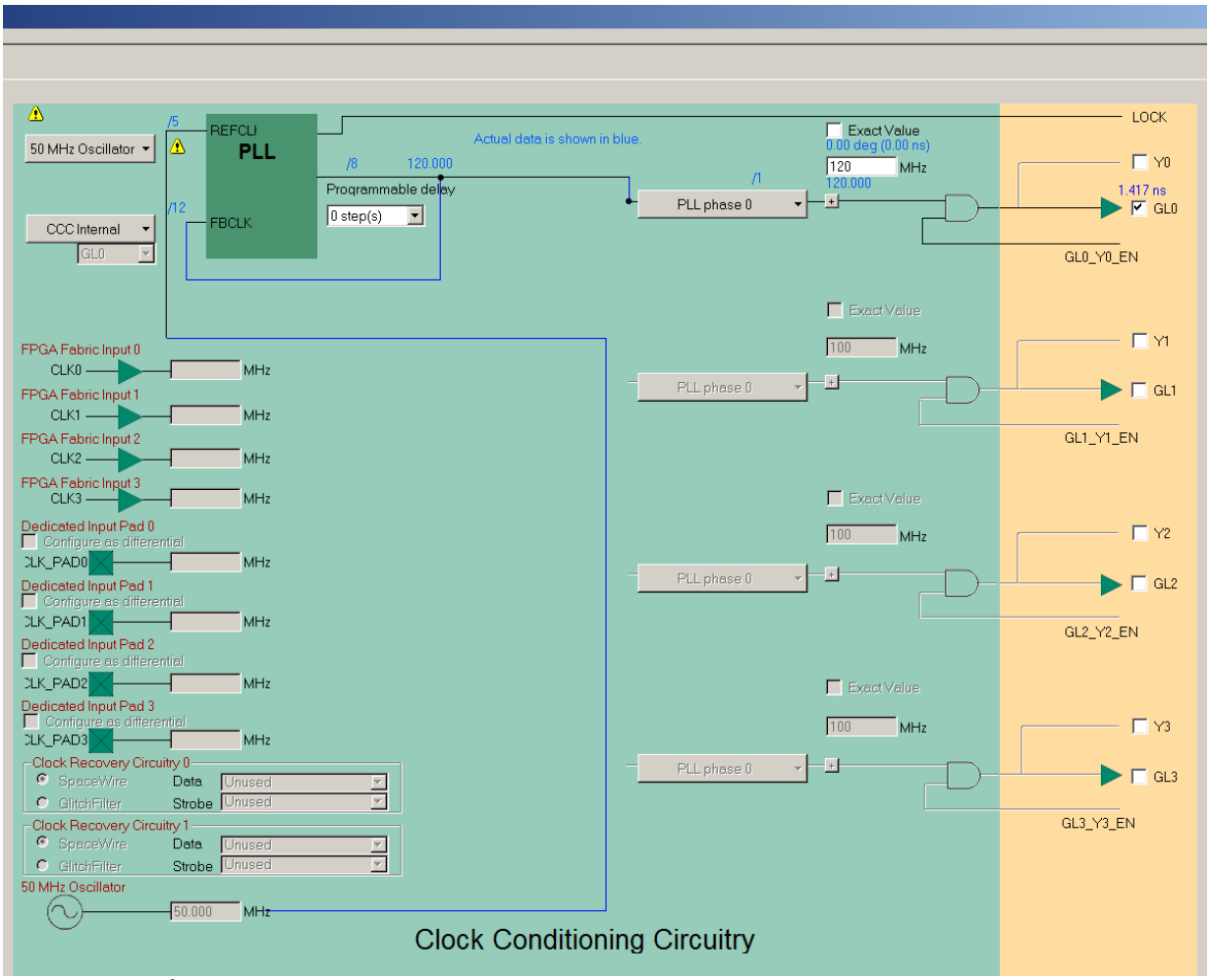


Figure 25: 2nd tab for CCC configuration with OSC as input and internal feedback in Microsemi Libero CAD tool. Chain3 in 2nd round heavy ion testing.

Variations of the DUT containing CCC PLLs were created. The DUTs differentiated by the use of delay taps within the PLL feedback path and the selection of DFF SET filter on or off. Figure 23, Figure 24, and Figure 25 are Microsemi Libero CAD configurations for PLLs with no delay taps (no programmable delays). This version was created with DFF SET filters turned on and DFF SET filters turned off.

One alternate version of this design was created which configured all PLL to use 63 delays taps. The configuration for each of the PLL controlled chains looked similar as what is shown in Figure 23, Figure 24, and Figure 25. The only change is in the programmable delay window. Instead of having the value 0 in the window, the value 63 is used. This version was created with DFF SET filters turned on and DFF SET filters turned off.

Table 7: List of PLL WSR DUAs for 2nd Round Rev C Heavy Ion Testing

Design	Design Name	PLL Frequency: input-CCC output	PLL Feedback	Clock Buffer	PLL Programmable delay	Number of Stages	SET Filter
G	WSR_PLL_1000	$Chain_0$: 50MHz-120MHz $Chain_1$: 120MHz-120MHz $Chain_2$: 50MHz-120MHz $Chain_3$: 50MHz-120MHz	$Chain_0$: Internal $Chain_1$: None $Chain_2$: External $Chain_3$: Internal	$Chain_0$: DGBIO-CLKINT $Chain_1$: DGBIO-CLKBUF $Chain_2$: DGBIO-CLKINT $Chain_3$: OSC-CLKINT	0	1000	OFF
H	WSR_PLL_1000_SET	$Chain_0$: 50MHz-120MHz $Chain_1$: 120MHz-120MHz $Chain_2$: 50MHz-120MHz $Chain_3$: 50MHz-120MHz	$Chain_0$: Internal $Chain_1$: None $Chain_2$: External $Chain_3$: Internal	$Chain_0$: DGBIO-CLKINT $Chain_1$: DGBIO-CLKBUF $Chain_2$: DGBIO-CLKINT $Chain_3$: OSC-CLKINT	0	1000	On
I	WSR_PLL_1000	$Chain_0$: 50MHz-120MHz $Chain_1$: 120MHz-120MHz $Chain_2$: 50MHz-120MHz $Chain_3$: 50MHz-120MHz	$Chain_0$: Internal $Chain_1$: None $Chain_2$: External $Chain_3$: Internal	$Chain_0$: DGBIO-CLKINT $Chain_1$: DGBIO-CLKBUF $Chain_2$: DGBIO-CLKINT $Chain_3$: OSC-CLKINT	63	1000	OFF
J	WSR_PLL_1000_SET	$Chain_0$: 50MHz-120MHz $Chain_1$: 120MHz-120MHz $Chain_2$: 50MHz-120MHz $Chain_3$: 50MHz-120MHz	$Chain_0$: Internal $Chain_1$: None $Chain_2$: External $Chain_3$: Internal	$Chain_0$: DGBIO-CLKINT $Chain_1$: DGBIO-CLKBUF $Chain_2$: DGBIO-CLKINT $Chain_3$: OSC-CLKINT	63	1000	On

6.6.1 PLL DUA Data Capture, Error Records, and Data Processing

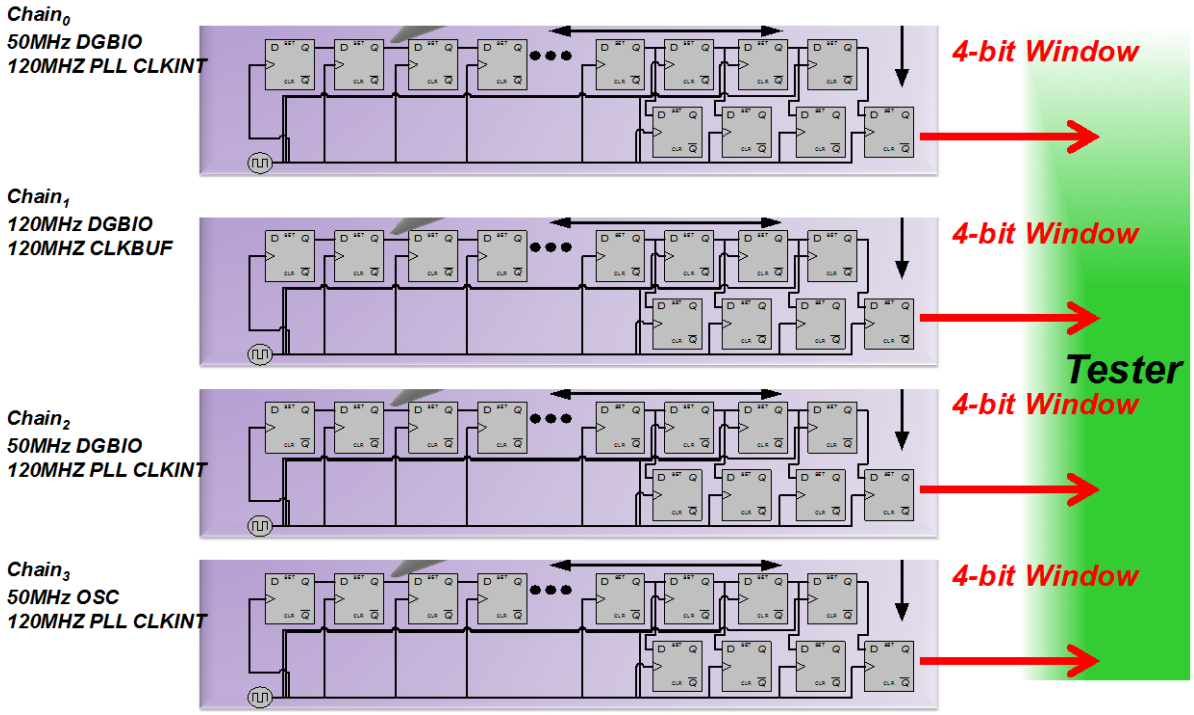


Figure 26: PLL WSR Chains. Four Chains (Chain0, Chain1, Chain2, and Chain3). All WSR chains are WSR_0 with PLL configuration variations as clock sources.

WSR designs G-J, as described in Table 7, use for the most part the same data capture, error records, and data processing as described in sections: 6.3.2, 6.3.3, 6.3.4, and 6.3.5. There are slight changes due to the potential for an SEU to cause the PLL or OSC to become unlocked.

LCDT control is different for PLL tests versus the first round of WSR testing because frequency is not varied in these tests. Chain0 and chain2 require a 50MHz clock pulse from the LCDT. Chain1 requires a 120 MHz clock pulse from the LCDT. Chain 3 requires no clock input from the LCDT because it uses the RTG4 internal oscillator as its clock source. Figure 26 illustrate a DUA with four WSR_0 chains and their configured PLL clock sources.

For the PLL DUAs, the LCDT data capture of the DUT outputs has one additional element. The locked signals of Chain0, Chain2, and Chain3 are continuously monitored during heavy ion testing. The locked signal monitors are edge detectors; subsequently the monitor checks whether the signal transitions from a state='1' to a state='0' (PLL becomes unlocked) or whether the signal transitions from a state='0' to a state='1' (PLL was unlocked and is now locked). The error record bit positions for PLL locked states can be seen in Table 5.

6.7 Counter Array DUA

During SEU testing, it would be ideal to be able to monitor every element of a complex design for every cycle. This is generally not feasible because it would require a DUT interface to the test vehicle

for every internal DFF node. Therefore, more creative designs and interfaces must be developed so operation during irradiation is unrestricted (fast, continuous, and unobstructed) yet node observation is maximized. Just as important, the tester must be fast enough and robust enough to capture and process the data supplied by the DUT. Processing integrity is very important. Dropped or incorrectly processed data can drastically change error cross sections.

For the SEU testing of the RTG4 Counters, a simple yet effective interface was used (snapshot bank of registers).

6.7.1 Counter Array Implementation

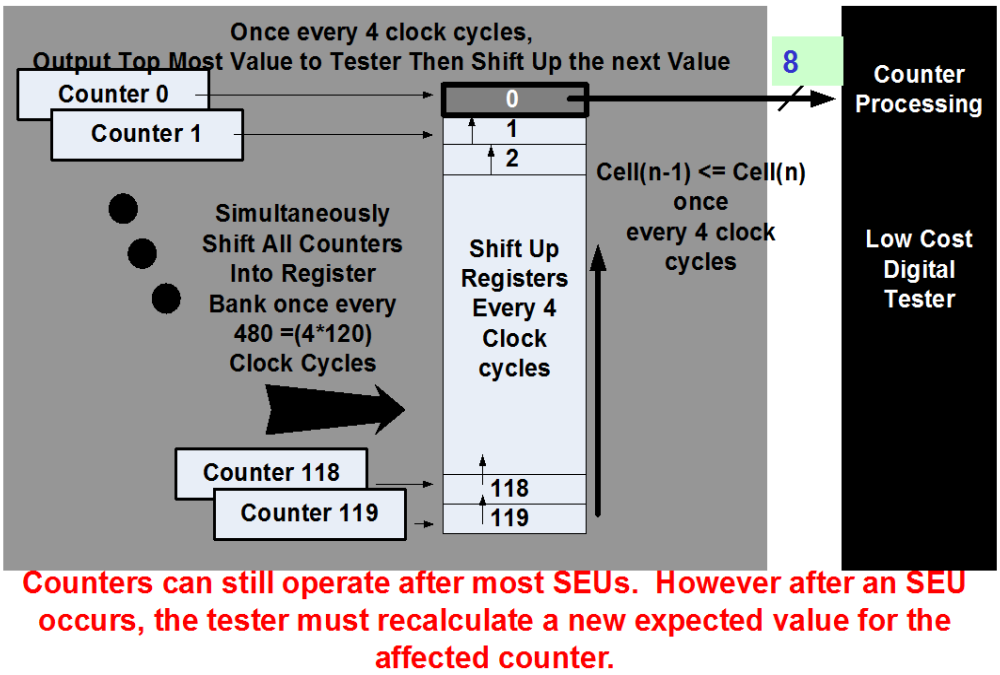


Figure 27: Schematic of the 8-bit Counters and their Output Selection Logic. In this case, the output selection logic is a Snapshot shift register (Shifts up counter values to the output registers every 4 cycles). The DUT uses a 8-bit counter scheme with 200 counters labeled “counter 0” through “counter 199”.

The counter array developed by REAG is illustrated in Figure 27. The array contains 200 counters that were 8-bits wide. Because it is impossible to simultaneously output 200 by 8-bits, requiring 1600 outputs, an output scheme had to be employed that would not compromise the number or speed of the counters yet ensure that each counter is an observable node. Conventional thinking would suggest employing a multiplexer that sequences through the array and selects one of the 1600 counters to be output at a time. Unfortunately, the function of the multiplexer, selecting 200 items, requires many levels of combinatorial logic that can be problematic during radiation testing and will slow down the operation of the circuit. Such a large block of logic can potentially mask the primary objective – i.e., which is characterizing counter SEU susceptibility. Therefore, a novel output methodology had to be established.

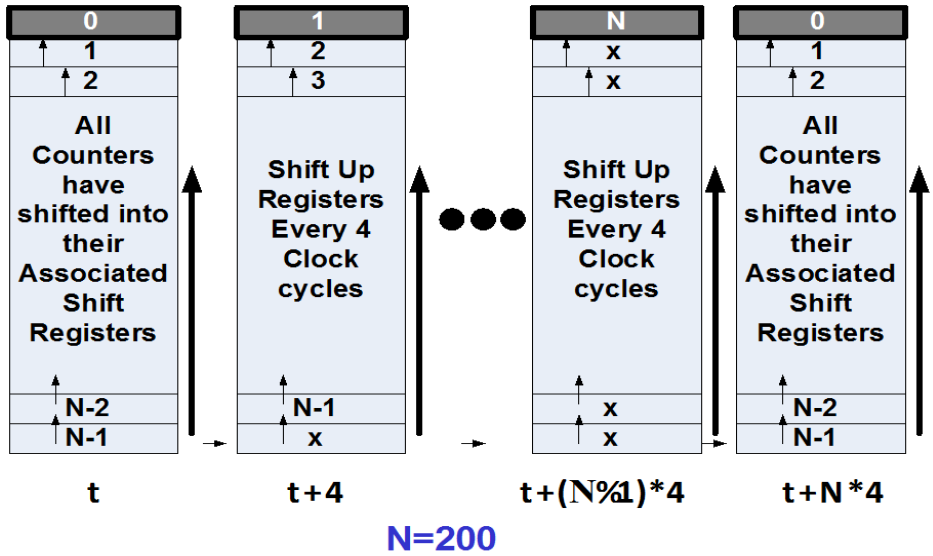


Figure 28: Counter Shift Register Cycles inside a snapshot bank; Values in Snapshot shift registers represent counter labels at a given moment in time. Regarding this figure, if there is an x with the Snapshot register, then it is considered a "don't-care" state. N=200 for the RTG4 Radiation Test.

As an alternative, a "snapshot" solution was implemented. With this methodology, each counter is captured simultaneously at a given time into a bank of snapshot registers. The number of registers is equivalent to the number of counters (i.e. each counter has its own snapshot register). This is illustrated in Figure 28. The top of the register bank (register 0) is the only register that is accessible by the tester and is 8- bits wide. Subsequently, the DUT to tester interface is simplified.

Figure 27 and Figure 28 illustrate the utilization of the snapshot shift register for each clock cycle. The nomenclature pertaining to the counter circuits throughout this document is as follows:

- n: counter label number
- k: snapshot cycle. First cycle out of reset all of the counter values are snapshot (shifted over) to the shift up register bank. K is 0 for this cycle. The next snapshot of counter values is 800 clock cycles later and k will increment to 1.
- $X_{n,k}$ is the counter-n value that was snapshot into the shift up register for snapshot cycle k.

Coming out of reset, each counter has an initial value (X_{n0}) equal to the counter label number (n), e.g. Counter 0 has a reset value of 0 ($X_{0,0}$=0) and counter 199 has a value of 199 ($X_{199,0}$=199). As the circuit comes out of reset, the counter values are loaded into its corresponding snapshot register. The counters continue to increment simultaneously as the shift registers shift counter values up every 4 clocks cycles – illustrated in Figure 28. The purpose of the snapshot register is to output all counters to the tester. The snapshot registers are loaded and then each value is shifted up so each counter-value can reach register 0 (the output window to the tester). After all loaded counters residing in the snapshot bank have reached register 0 (τ+4N= once every 4*200 = 800 clock cycles), all of the counters are reloaded into the snapshot shift register bank.

As a summary, the key of the snapshot output scheme, is that the shift register array has now replaced a huge multiplexer. The benefits are as follows:

1. Counter upsets can easily be identifiable.
2. Counters are incrementing and changing state every cycle. Hence maximum performance can be tested.
3. If a counter becomes upset, it will stay upset and it will eventually be captured during the snap shot period Counters are continuous and are not interrupted due an elaborate output scheme
4. Routing complexity is exclusive to just the counter array
5. The shift register architecture allows for high speed counter testing. A large multiplexer creates long paths of combinatorial logic and significantly slows down system speed.

The state space of the DUT should be deterministic and traversable. Pertaining to equation (6), for a 8-bit counter running at 25MHz and a shift up period of once every 4 clock cycles, it will take a little less than 1s for every state to be reached for all counters. Radiation tests generally last for several minutes. Hence, counter states are considered fully traversed within each test run.

$$\frac{2^8}{f_s} = \frac{256}{100MHz} = 2.56us \qquad (6)$$

6.7.2 Counter I/O Interface and Expected Outputs

Table 8: DUT1 WSR Outputs.

I/O Name	Bits	Direction wrt to DUT	Description
Counter_Shift_CLK	1	OUT	Counter shift Clock
COUNTER	8	OUT	8-bit Counter output
CLK	1	IN	Clock to counter circuitry
RESET	1	IN	Reset to counter circuitry

Table 8 lists the I/O for the counter DUA. The DUT receives a clock (CLK) and a reset (RESET) from the tester. The DUT responds with two primary outputs:

- Counter: 8-bit counter output of DUT. This is the output from the top snapshot register that is forwarded to the tester.
- Counter_Shift_CLK: This output is ¼ the speed of the CLK (input from the tester). It is ¼ the speed indicating the shift speed (as previously mentioned, the snapshot register shifts once every 4-CLK cycles).

The expected output (COUNTER) is purely an increment by 1 starting at value 0. The first COUNTER_Shift_CLK output will pertain to counter 0, followed by counter 1 after 4-CLK cycles, counter 2… up to counter 199. After the value of counter 199 has reached the top of the snapshot register and is output to the tester, a new snapshot is performed (all counters are shifted into their associated snapshot register). After the new snapshot load, the top of the snapshot register bank now has the value for counter 0. Hence, COUNTER_OUT (top of snapshot register) will provide the tester loaded value of counter 0.

With respect to the separate counters, Counter(n) is output every 800 cycles (800 cycles= 1 snapshot cycle). Therefore the counter values that represent each counter will increment by 800 for each snapshot cycle.

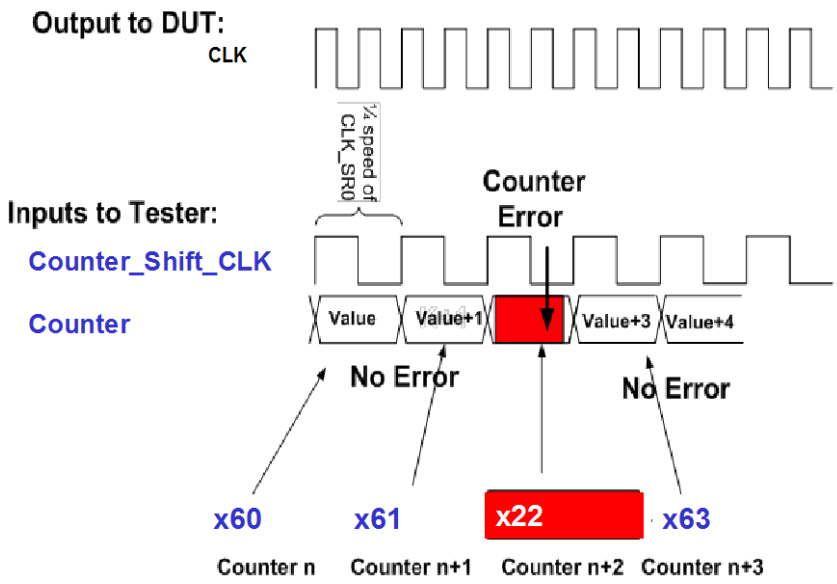


Figure 29: Typical SEE Counter Outputs. Each output represents a value from a different counter in the array. Counter selection is sequential, hence, the counter number and the counter values all increment by 1 each Counter_Shift_Clk cycle.

6.7.3 Counter Array and LCDT Specifics

DUA contains the following:

- 200 8-bit counters
- 200 8-bit snapshot registers

All counters and snapshot registers are connected to the same clock tree and RESET. The clock tree is fed by the CLK input from the LCDT.

The LCDT will send the following signals to the DUT:

- 1 clock
- 1 reset

6.7.4 Processing the DUT Outputs during Testing

The outputs of the DUT are fed to the tester for data processing. The objective of the data processing is to capture data from the DUT, compare to an expected value, and report to the host PC if there is an error. The DUT system clock and reset signals are generated in the LCDT. The following describes how the counter expected values are calculated. As a note, each counter will have a uniquely stored expected value.

6.7.4.1 Counter Array data processing

All counters within the array independently and continuously increment every clock cycle. Their states are captured (snapshot) once every 800 (4*200) clock cycles into a snapshot array. The top most register of the snapshot array is the only interface to the tester.

In order to avoid metastable events due to an error in the output, data is registered twice before evaluation. Both the data and the counter number are expected to increment every 4 cycles and will wrap around at its boundaries as listed in Table 9.

Table 9 Counter Value and Counter Number Wrap around Boundaries

	Bit Width	Wrap Around Value
8 bit Counter	8	2^8-1 (after 2^8-1 next value is 0)

At the beginning of each snapshot cycle (at capture time), each counter should have incremented by either 800MOD8 from the last snapshot capture. If not, then an error record is sent to the LCDT. The tester keeps a copy of each counter value during a snapshot cycle. This copy is kept around as a comparison point for the next snapshot cycle. During the next snapshot cycle, the old copy becomes: “Last counter value” and the current counter value (just captured) becomes the New counter value. The tester is expecting the increment as follows:

Expected Checks: New Counter Value = (Last counter value + 800) MOD 8 … for a 8-bit counter

If this doesn’t occur, an error is registered. The following is a list of potential incorrect counter values and their corresponding sources of error:

- A single-bit (or multiple-bit) upset in a counter,
- An upset while the value is sitting in the snapshot register,
- Configuration SEU or multiple bit upset (MBU),
- Global upset, or
- Catastrophic event

Due to the complexity of this device, error signatures can be convoluted. Consequently, a significant amount of post processing on radiation data is required to differentiate the SEUs.

6.7.4.2 Counter SHIFT_CLK Processing

Regarding the SHIFT_CLK associated with the Counter Arrays, it is used to alert the tester that the counters are alive and new counter data is ready to be taken. The SHIFT_CLKs are always ¼ of the speed of the DUT system clock. SHIFT_CLK can be interpreted as an operation heart-beat.

Due to the interface delays and device latencies and in order to consequently decouple the DUT to tester timing restrictions, the DUT SHIFT_CLK is considered asynchronous to the tester and is sampled using the LCDT system clock (max 50 MHZ). Thus, the tester’s sampling clock will always be 4 times as fast as SHIFT_CLK. The SHFT_CLK is fed into a metastability filter and an edge

detect. This process takes 1 to 2 clock cycles of the sampling clock (detection will be delayed by 1 to 2 sampling clock cycles of the actual edge).

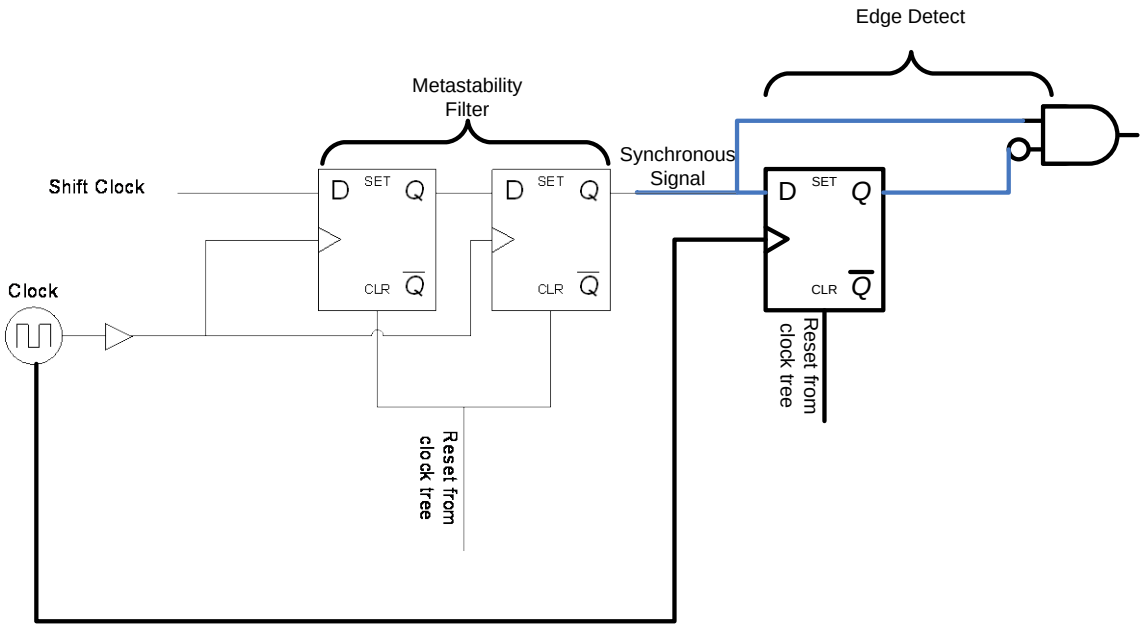


Figure 30: Shift_ClK Capture consists of a Metastability Filter and an Edge Detect

The SHIFT_CLK edge is expected to come at a frequency that is ¼ of the LCDT clock. If the edge is stopped, glitched, or missing, the event is reported to the host PC by the LCDT.

6.7.5 Counter Array Error Record

A significant amount of post processing was performed on this data. Subsequently, the error record should contain enough information to comprehend and differentiate between events.

Table 10: Counter Array Error Record Fields: Yellow indicates Fields generated from Tester capture of DUT Inputs. Other fields indicate values calculated internal to the tester

Field	Bits	Description
Data Cycle N	16	Current DUT output. Error: If it is not an increment of 1 from the previous counter value and not an increment of 2 from the data value received cycle (n-2) No error (recover from error): If it is not an increment of 1 from the previous value but is an increment of the data value received cycle (n-2)

		Otherwise: DUT is in a burst of error
Data Cycle N-1	16	Capture cycle n-1 DUT output (capture cycle n-1 is actually 4 LCDT clock cycles from Data cycle N)
Data Cycle N-2	16	Capture cycle n-2 DUT output (capture cycle n-2 is actually 8 LCDT clock cycles from Data cycle N)
Data Cycle N-3	16	Capture cycle n-1 DUT output (capture cycle n-3 is actually 12 LCDT clock cycles from Data cycle N)
Counter Number	16	LCDT local copy of expected counter number. (0 through 299)
Error Count		
Time Stamp	32	Time that error was observed. Time stamp is a cycle counter. It is later converted to seconds for post processing.
Status flags	3	

6.7.6 Counter Array Post Processing

Each error record was post-processed. Error records (SEUs) were differentiated via the following:

- Bit or multiple-bit upset: This example is illustrated in Figure 3. One counter-bit flips and the counter keeps incrementing as normal from that flipped state. This error signature is attributed to a data-path SEU.
- Snap shot register:
  - A snapshot register bit incurs an SEU. In this case a counter will show up as incorrect for two consecutive snapshot registers.
  - Snap shot register can either stop shifting- in this case the output values will remain constant or become noise
  - Snap shot register can skip a cycle, in this case the counter values will be off the number of skipped shift cycles from their expected values
- Burst of broken counters: Counters stop counting and their values either stay constant or become complete noise. This error signature is attributed to either a misconfiguration or a global upset.
  - Because the counters are flushable, a global structure SEU error can be recoverable by using a reset.
  - Because configuration upsets can only be fixed by performing a full configuration, the associated error signature will appear as a stuck fault.

$$\sigma_{COUNTERSEU} = \frac{\#CounterArray_{errors}}{fluence * \#Counter_ARRAY_DFFs} \qquad (7)$$

6.8 Internal SRAM Memory DUAs

There are two types of SRAM memory that are accessible to a RTG4 user. There are a total of 210K Micro-SRAM (uSRAM) bits and a total of 209 18K blocks of Large-SRAM (LSRAM).

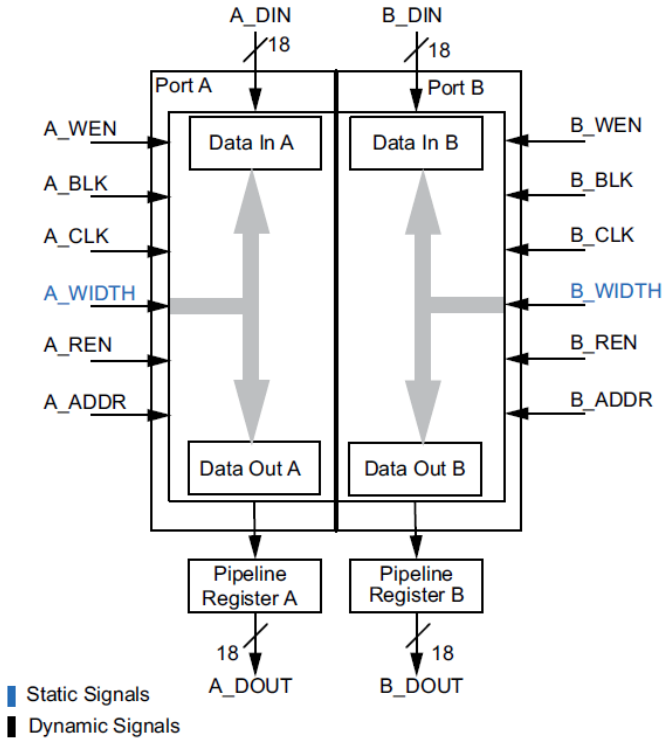


Figure 31: High-level schematic of RTG4 internal SRAM

Figure 31 is a high-level schematic representation of the RTG4 internal SRAM. All SRAMs can be configured as DUAL port and have the capability of single error correct double error detect (SECDED) error detection and correction (EDAC). A high-level schematic representation of the RTG4 internal SRAM with EDAC circuitry is illustrated in Figure 32.

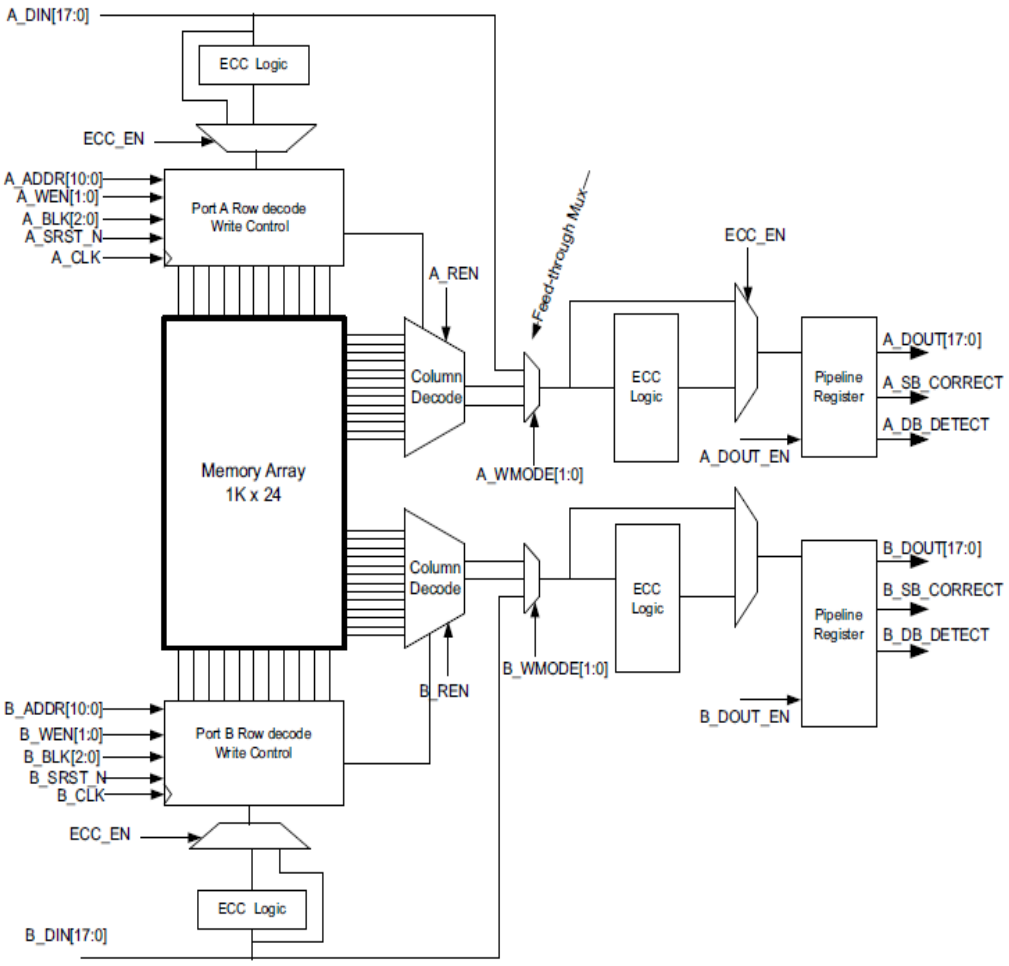


Figure 32: High-level schematic of RTG4 internal SRAM including EDAC circuitry

Address bus and data width are configurable and are limited by the maximum size of the internal uSRAM or the internal LSRAM. The designs used within this investigation have the following parameters:

- uSRAM: 8-bit wide data bus with 1024 address locations. There are two versions of uSRAM designs. One has EDAC and one does not.
- LSRAM: 8-bit wide data bus with 65536 address locations. Due to time limitations, no EDAC was implemented with the LSRAM. However, if time and money permits, additional testing that includes LSRAM EDAC is expected to be performed.

6.8.1 uSRAM DUA Schematic and Configuration Details

The Microsemi Libero tool was used to configure the different memories. Figure 33 is a top-level representation of the uSRAM without EDAC circuitry. Inputs are on the left of the figure and outputs are on the right. Figure 34 is a picture of the Microsemi Libero CAD uSRAM configuration panel. This is the configuration of the uSRAM without EDAC circuitry. Notice the error correction code (ECC) box has the disabled option inside of it.

An uSRAM design was created using DFF SET filters turned on and an uSRAM design was created with DFF SET filters turned off.

The DUA port names are listed in Table 11and are illustrated in Figure 33.

Table 11: uSRAM without EDAC Port Names

Port Name	Operation	Direction	Bus Width
C_WEN	Write enable	Input	1
CLK	Clock	Input	1
C_DIN	Write Data	Input	8
A_ADDR	Write Address	Input	10
B_ADDR	Read Address	Input	10
C_ADDR	Read Address	Input	10
A_DOUT	Read Address	Input	8
B_DOUT	Read Address	Input	8

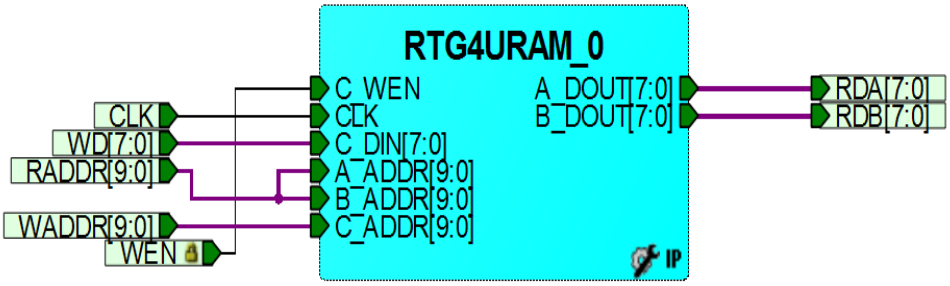


Figure 33: Top level representation of the uSRAM without EDAC circuitry. Inputs are on the left of the picture and outputs are on the right.

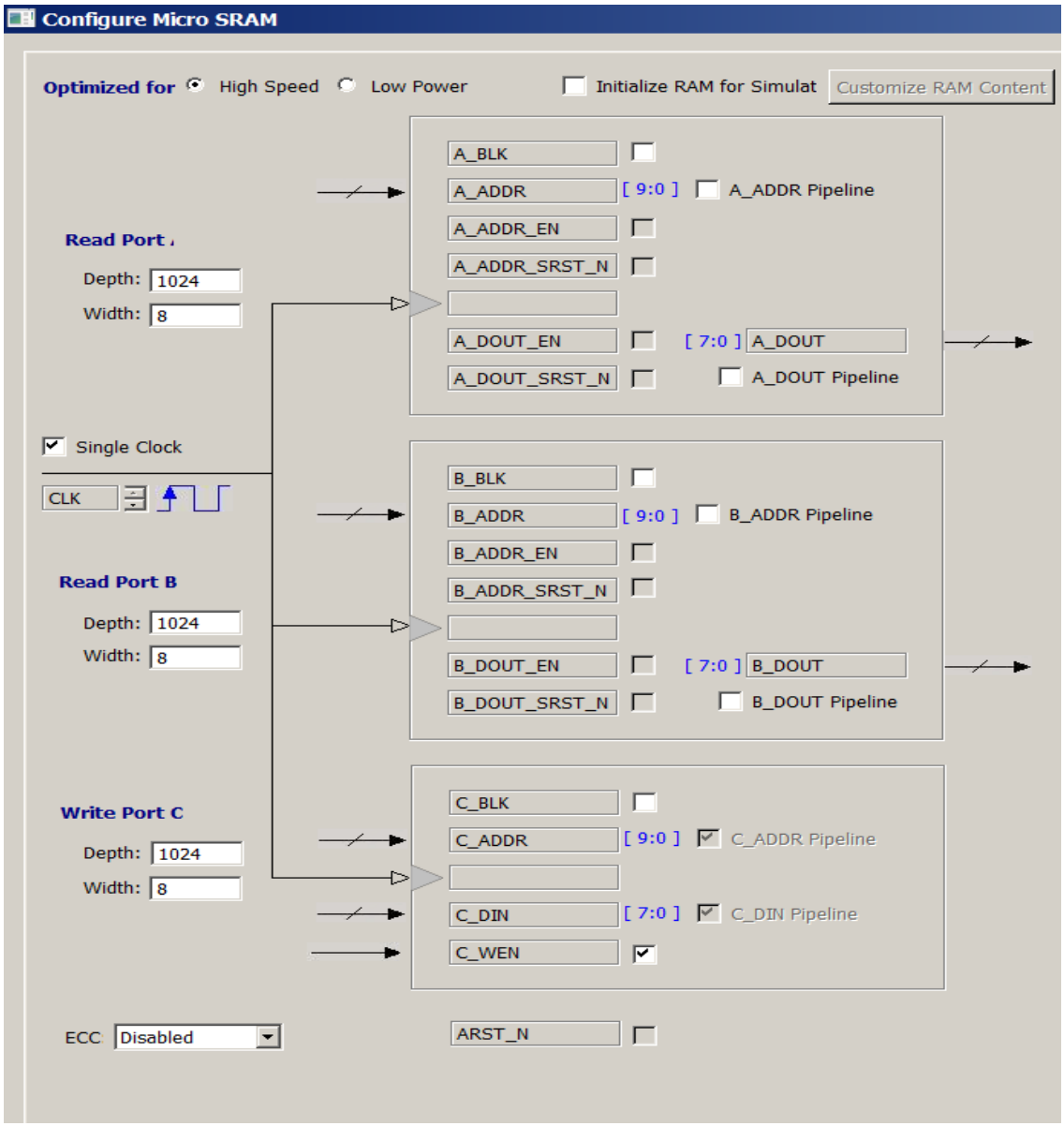


Figure 34: Microsemi Libero CAD uSRAM configuration panel. This is the configuration of the uSRAM without EDAC circuitry.

The DUA port names are listed in Table 12 and are illustrated in Figure 35.

Table 12: uSRAM with EDAC Port Names

Port Name	Operation	Direction	Bus Width
C_WEN	Write enable	Input	1
CLK	Clock	Input	1
C_DIN	Write Data	Input	8
A_ADDR	Write Address	Input	10
B_ADDR	Read Address	Input	10
C_ADDR	Read Address	Input	10
A_SB_CORRECT	Read Address	Input	1
B_SB_CORRECT	Read Address	Input	1
A_DB_DETECT	Read Address	Input	1
B_DB_DETECT	Read Address	Input	1
A_DOUT	Read Address	Input	8
B_DOUT	Read Address	Input	8

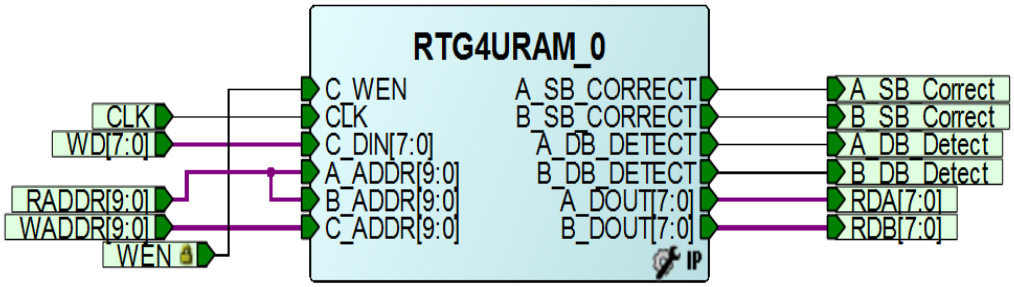


Figure 35: Top level representation of the uSRAM with EDAC circuitry. Inputs are on the left of the picture and outputs are on the right.

Figure 35 is a top-level representation of the uSRAM without EDAC circuitry. Inputs are on the left of the figure and outputs are on the right. Figure 36 is a picture of the Microsemi Libero CAD uSRAM configuration panel. This is the configuration of the uSRAM without EDAC circuitry. Notice the error correction code (ECC) box has the disabled option inside of it.

As previously mentioned, Figure 34 and Figure 36 are the configuration panels for the uSRAM blocks with and without EDAC. Notice that in both cases that no pipelines are used. Generally, pipelining is selected to speed up memory access. However, we chose not to implement pipelining in order to focus on memory-bit SEUs versus DFF SEUs.

Regarding Figure 34 and Figure 36, it can be seen that the uSRAM DUAs have dual read ports (A and B) and one write port (C). All ports use the same clock. Hence, the uSRAM dual port memory

structures are synchronous. Memory addresses are shared; hence the user must take care not to read and write the same address space simultaneously. If future testing allows us, we will test the internal SRAMs in asynchronous mode.

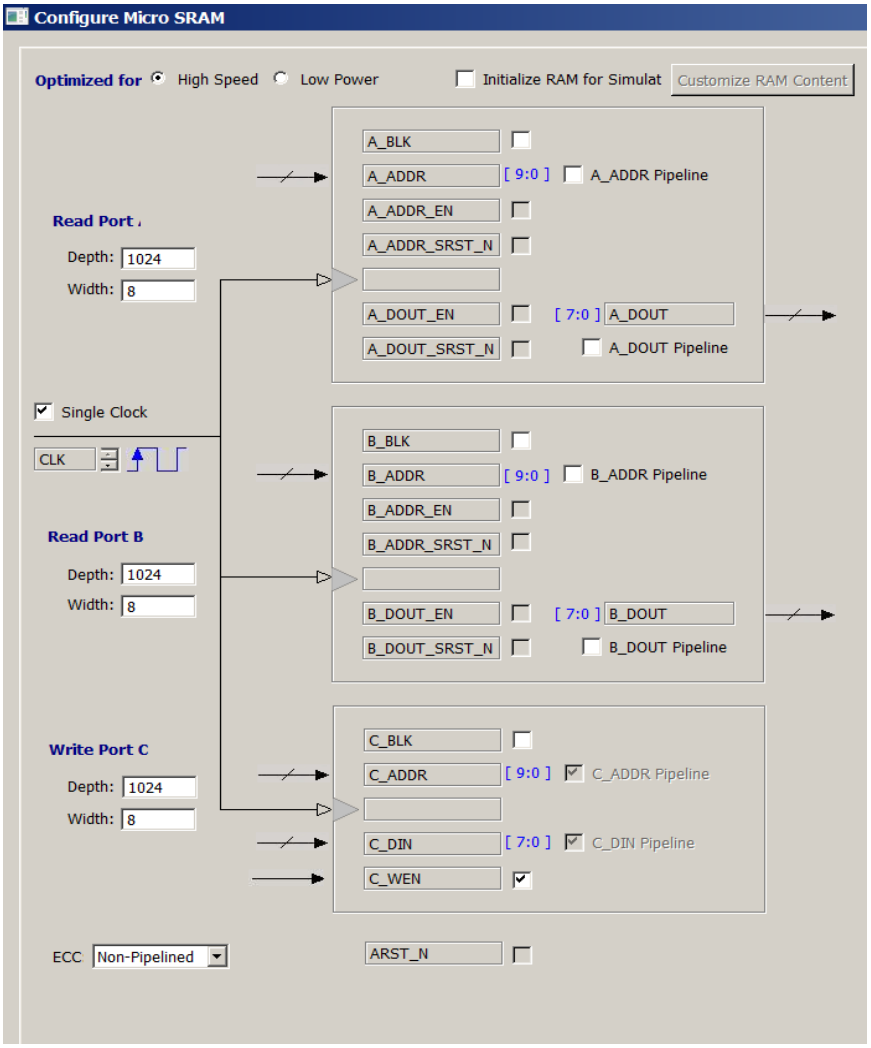


Figure 36: Microsemi Libero CAD uSRAM configuration panel. This is the configuration of the uSRAM with EDAC circuitry.

6.8.2 LSRAM DUA Schematic and Configuration Details

The Microsemi Libero tool was used to configure the different memories. Figure 37 is a top-level representation of the LSRAM without EDAC circuitry. Inputs are on the left of the figure and outputs are on the right. Figure 38 is a picture of the Microsemi Libero CAD LSRAM configuration panel. This is the configuration of the LSRAM without EDAC circuitry. Notice the error correction code (ECC) box has the disabled option inside of it.

The LSRAM is configured slightly different than the uSRAM. The LSRAM has a dual port (A and B) however the port A can only be written and port B can only be read. Although there is a write side and a read side of the memory, both ports share access to the same address space. If future testing allows us, we will test the memories in asynchronous mode.

An LSRAM design was created using DFF SET filters turned on and an LSRAM design was created with DFF SET filters turned off.

The LSRAM DUA has the following ports listed in Table 13 and are listed in Figure 37.

Table 13: LSRAM Port Names

Port Name	Operation	Direction	Bus Width
WEN	Write enable	Input	1
CLK	Clock	Input	1
WD	Write Data	Input	8
WADDR	Write Address	Input	16
RADDR	Read Address	Input	16
RD	Read Data	Output	8

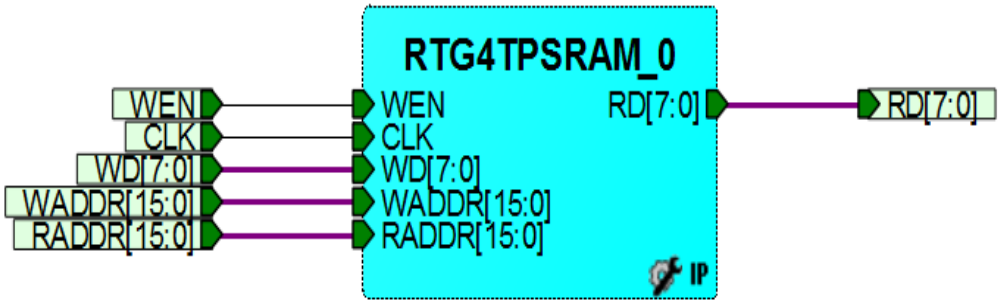


Figure 37: Top level representation of the LSRAM without EDAC circuitry. Inputs are on the left of the picture and outputs are on the right.

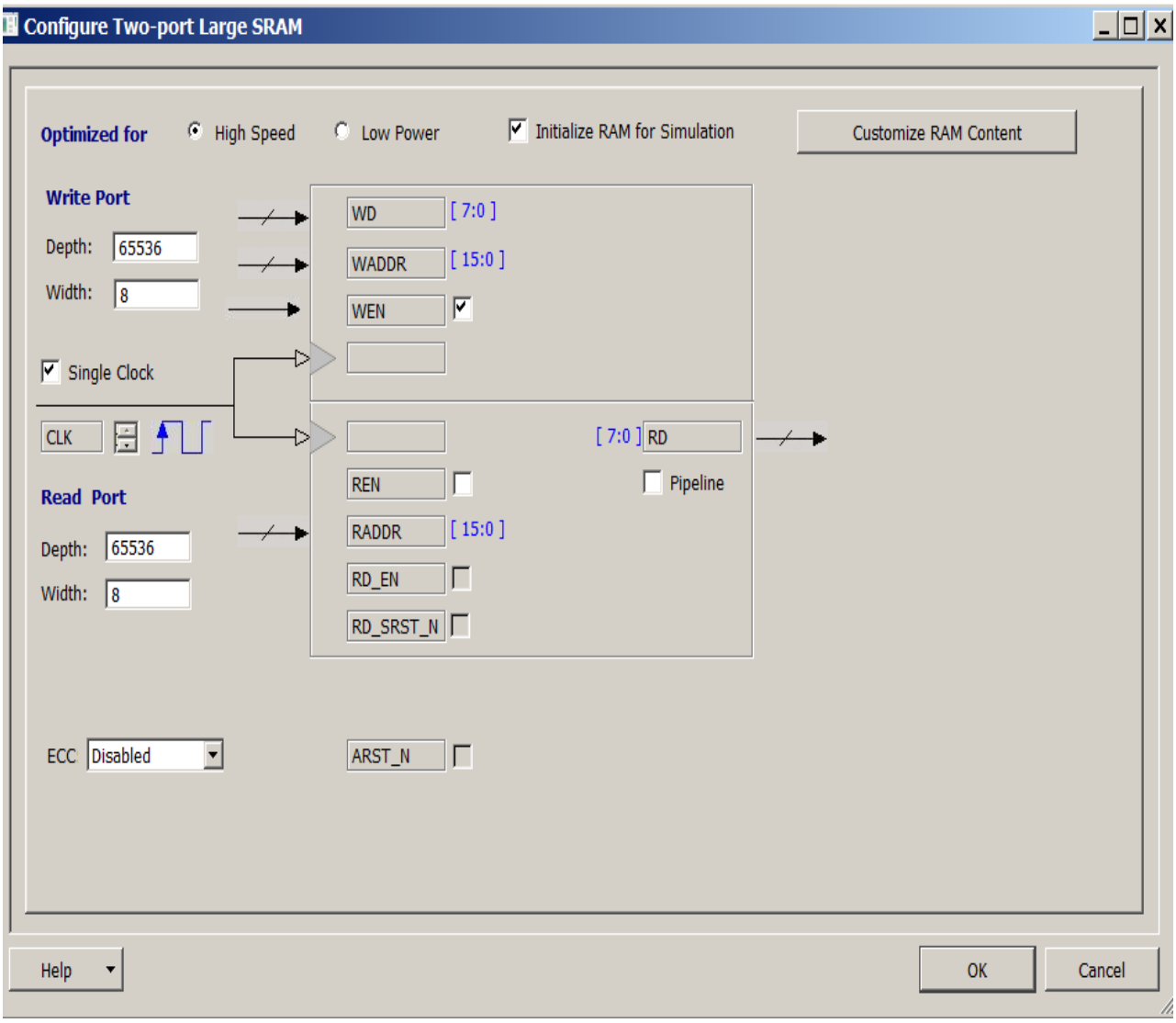


Figure 38: Microsemi Libero CAD LSRAM configuration panel. This is the configuration of the LSRAM without EDAC circuitry

6.8.3 Summary of RTG4 internal SRAM DUAs

A summary of RTG4 internal SRAM DUAs is listed in Table 14.

Table 14: List of SRAM DUAs

Design Name	Address Space	Port A Capability	Port B Capability	Port C	EDAC	SET Filter
uSRAM	1024	Read	Read	Write	Disabled	OFF
uSRAM_SET	1024	Read	Read	Write	Disabled	On
uSRAM_EDAC	1024	Read	Read	Write	Enabled	OFF
uSRAM_EDAC_SET	1024	Read	Read	Write	Enabled	On
LSRAM	65536	Write	Read	Not available	Disabled	OFF
LSRAM_SET	65536	Write	Read	Not available	Disabled	On

6.8.4 SRAM DUA Operation

The following is the algorithm for RTG4 SRAM DUA testing:

- Write the entire address space. Each address location is written with an 8-bit counter. The value of the counter is equivalent to the lower 8-bits of its address.
- Upon command, start the read-write process. Sequentially each address is read. The output is provided from the DUT to the tester. Following, the same address is re-written with its appropriate counter value.

6.8.5 SRAM DUT to LCDT Requirements

The LCDT is required to provide a clock, read address, and write address, write enable, and read enable to the DUT. The DUA performs the expected read or write function depending on the write enable and read enable state.

6.8.6 LSRAM and uSRAM Data Processing

Upon an active read enable (activated by the LCDT), the DUA will provide the address location contents on the read port. After a delay, the LCDT reads the DUT port. Once the data is read, the LCDT will compare the read data to the current lower 8-bits of the address. If they are not equal, the LCDT sends a message to the host PC.

6.8.7 Additional Data Processing for uSRAM EDAC DUAs

uSRAM EDAC DUAs have additional signals that reflect the state of the EDAC circuitry. These signals indicate single bit corrections and double bit detections for the A and B read ports. The LCDT monitors the state of the signals and places them in error record.

6.8.8 LSRAM and uSRAM Error Record

A significant amount of post processing was performed on this data. Subsequently, the error record should contain enough information to comprehend and differentiate between events.

Table 15: LSRAM Error Record Fields: Yellow indicates Fields generated from Tester capture of DUT Inputs. Other fields indicate values calculated internal to the tester

Field	Bits	Bit Position	Description
Read Data	8	7:0	DUA output of data after a read enable
Address A	16	55:40	Current Write Address
Address B	16	75:60	Current Read Address
Time Stamp	32	177:146	Time that error was observed. Time stamp is a cycle counter. It is later converted to seconds for post processing.
Status flags	3	183:181	

Table 16: uSRAM Error Record Fields for EDAC and no EDAC DUAs: Yellow indicates Fields generated from Tester capture of DUT Inputs. Other fields indicate values calculated internal to the tester

Field	Bits	Bit Position	Description
Read Data A	8	7:0	DUA output of data after a read enable port A
Read Data B	8	15:8	DUA output of data after a read enable port B
A_SB_Correct	1	16	DUA output indicating a single bit correction was performed on port A (field is set to 0 if the DUA doesn't contain EDAC)
B_SB_Correct	1	17	DUA output indicating a single bit correction was performed on port B (field is set to 0 if the DUA doesn't contain EDAC)
A_DB_Detect	1	18	DUA output indicating a double bit detection was performed on port A (field is set to 0 if the DUA doesn't contain EDAC)
B_DB_Detect	1	19	DUA output indicating a double bit detection was performed on port B(field is set to 0 if the DUA doesn't contain EDAC)
Address A	10	49:40	Current Write Address

Address B	10	69:60	Current Read Address
Time Stamp	32	177:146	Time that error was observed. Time stamp is a cycle counter. It is later converted to seconds for post processing.
Status flags	3	183:181	

6.8.9 LSRAM and uSRAM Data Post Processing

Each error record was post-processed. Error records (SEUs) were differentiated via the following: Single bit or multiple-bit upset. In addition, the efficacy of the EDAC circuitry was heavily analyzed.

•

$$\sigma_{LSRAM_Singlebit} = \frac{\#LSRAMSingleBit_{errors}}{fluence*65536*8} \quad (8)$$

$$\sigma_{LSRAM_Multiplebit} = \frac{\#LSRAMMultipleBit_{errors}}{fluence*65536*8} \quad (9)$$

$$\sigma_{uSRAM_Singlebit} = \frac{\#uSRAMSingleBit_{errors}}{fluence*1024*8} \quad (10)$$

$$\sigma_{uSRAM_Multiplebit} = \frac{\#uSRAMMultipleBit_{errors}}{fluence*1024*8} \quad (11)$$

6.9 DSP (HMACC) DUAs

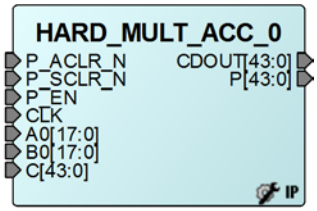


Figure 39: Microsemi top-level diagram of a hard multiplier accumulate (HMACC) block

The RTG4 math blocks (DSP or otherwise know as HMACC) were investigated. Figure 39 and Figure 40 illustrate Microsemi HMACC blocks. We created DUAs with DSP blocks chained together as a finite impulse response (FIR) filter. A typical FIR DUA is illustrated in Figure 41.

Each FIR chain has 50 DSP (HMACC) blocks cascaded together. Each block is configured as a 18x18 multiply accumulate block. Hence, the output of each block is 44-bits wide. Monitoring a high-speed FIR with a 44-bit output is a challenge. This is because of the signal integrity problems and difficulty of capturing 44 signals transferring from the DUT to the LCDT.

In order to deal with the signal integrity and capture challenges, built-in-self-test (BIST) is included in the DUA. Two FIR chains (each containing 50 DSP blocks) are implemented in the DUA. The following are the BIST attributes of the DUA:

- The last stages of the FIRs are compared:
  - If the 44-bit outputs of the two FIRs (last stage compare only) are not equivalent, then a signal (BADCOMPARE) gets set to a logic ‘1’. Else if the outputs are equivalent, BADCOMPARE is set to a signal ‘0’.
  - If the 44-bit outputs of the two FIRs (last stage compare only) are set to all ‘0’ (from an unexpected reset), then a signal (ALLZERO) gets set to a logic ‘1’. Else if the outputs are equivalent, ALLZERO is set to a signal ‘0’.
- BADCOMPARE and ALLZERO are sent to the LCDT.
- The lowest order 8-bits of the last stages of the two FIRs is sent to the LCDT.
- An important portion of the DUA is that both chains are in a dual redundant topology. In order to keep them synchronized and for us to focus on DSP susceptibility, they share multiple components; e.g., there is only one A coefficient register per FIR stage. The redundant HMACCs in the stage use the same coefficient registers. Hence if there is an SEU in one of the registers, it should not cause the DSP blocks to have a miscompare. In an “real-life” implantation of a FIR, you would want to have separate registers and detect miscompares all the wary from the FIR through their coefficients. However, because we are focusing on DSP susceptibility in these tests, sharing outside resources enhances DSP isolation. The topology is illustrated in Figure 41. We have used this same topology for DSP heavy ion testing in the RTAXs 4000D devices. The following resources are shared across the redundant FIR components:
- Clock
- Reset
- Coefficients

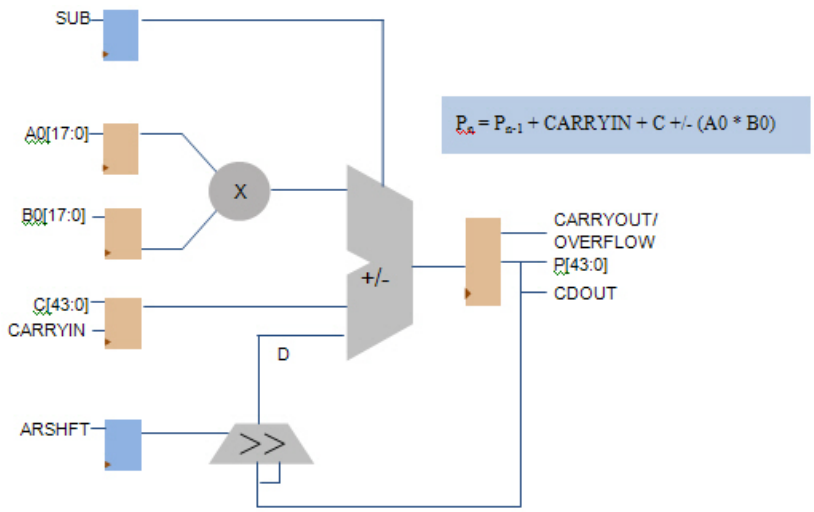


Figure 40: Logic schematic of a Microsemi RTG4 hard multiplier accumulate (HMACC) block

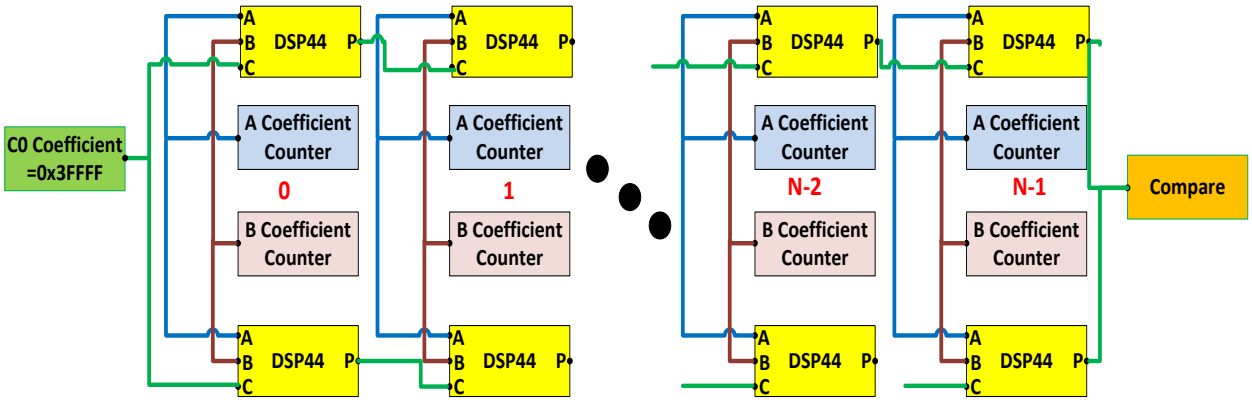


Figure 41: DUA finite response filter (FIR). The compare sends out two signals: BADCOMPARE and ALLZERO

6.9.1 DUA FIR to LCDT Requirements

The LCDT is required to provide a clock and a reset to the DUT. Once the clock and reset signals become active, the DUT will provide the LCDT outputs. The LCDT monitors the BADCOMPARE and ALLZERO signals.

6.9.2 DUA FIR Data Processing

Edge detector signal monitors were placed on the BADCOMPARE and ALLZERO signals. Any transitions from a logic ‘0’ to logic ‘1’ or logic ‘1’ to logic ‘0’ are sent to the Host PC.

6.9.3 DUA FIR Error Record

A significant amount of post processing was performed on this data. Subsequently, the error record should contain enough information to comprehend and differentiate between events.

Table 17: LSRAM Error Record Fields: Yellow indicates Fields generated from Tester capture of DUT Inputs. Other fields indicate values calculated internal to the tester

Field	Bits	Bit Position	Description
BADCOMPRE	1	0	DUA output of data after a read enable
ALLZERO	1	1	Current Write Address
Frequency	10	145:136	Frequency of FIR operation is controlled by the user via an LCDT command. Field reflects a divider of 100MHz. Top speed is 100MHz – yet field can be either a decimal 0 or a decimal 1 for a frequency of 100MHz
Time Stamp	32	177:146	Time that error was observed. Time stamp is a cycle counter. It is later converted to seconds for post processing.
Status flags	3	183:181	

6.9.4 DUA FIR Data Post Processing

Each error record was post-processed. Error records (SEUs) were differentiated via the following: Single bit or multiple-bit upset. In addition, the efficacy of the EDAC circuitry was heavily analyzed.

-

$$\sigma_{BADCOMPARE} = \frac{\#BADCOMPRE_{errors}}{fluence} \quad (12)$$

$$\sigma_{ALLZERO} = \frac{\#ALLZERO_{errors}}{fluence} \quad (13)$$

7. DUT ACCELERATED HEAVY ION TEST PROCEDURES

7.1 Summary of DUT-Tester operation.

Overview of performing an accelerated SEU test:

- Bias the device, turn on clocks, and toggle reset.
- For dynamic tests: DUA logic operates as tester captures DUA outputs and compare with expected counter pattern (verify no errors).
- Irradiate DUT.
- During irradiation: Tester reads DUT and compares to expected value:
    - If error during read, then the LCDT records that an error has occurred and sends the data value with timestamp to the PC.
    - If not done with test go to 4, else go to 5.
- Stop Beam
- Reset Tester and DUT to prepare for next test

7.2 Running a Full Test

7.2.1 Files required for running a test – 1st round of Rev C Testing

Table 18 lists the files and their time stamps used for running a test. Independent of the DUT design under analysis (DUA), each test requires a DUT file (configuration file with extension ".stp"), and a tester bit file (LCDT configuration file with extension ".bit").

In order to run a test, the tester-bit file is downloaded from the host PC, via Xilinx-impact (JTAG), to the LCDT3 configuration memory; the DUT-configuration file is downloaded from the host PC, via Microsemi-Libero Flash programmer, to the DUT configuration memory. After each test is finished, the DUT configuration is read-back, via Microsemi-Libero flash programmer. The read-back verify function will indicated a pass-fail.

Table 18: List of files used for each test

DUT	Time	Tester	Time
DUT_SHIFTREG_TOP_1clk_1async_reset.stp	12/15/15 16:01	RTG4_tester_top_200_1clk_1async_reset	12/15/15 15:31
DUT_SHIFTREG_TOP_w_Resets (4)	12/9/15 11:53	RTG4_tester_top_200_w_resets (4)	12/15/15 14:57
DUT_SHIFTREG_TOP_large_resetsandclocks.stp	12/15/15 17:03	RTG4_tester_top_200_w_resets (4)	12/15/15 14:57
RTG4_2Counters	12/13/15 15:51	RTG4_counter_tester_2Counters	12/13/15 10:38

7.2.2 Files required for running a test – second round of Rev C Testing

Table 19 through Table 22 lists the files and their time stamps used for running a test. Independent of the DUT design under analysis (DUA), each test requires a DUT file (configuration file with extension ".stp"), and a tester bit file (LCDT configuration file with extension ".bit").

In order to run a test, the tester-bit file is downloaded from the host PC, via Xilinx-impact (JTAG), to the LCDT3 configuration memory; the DUT-configuration file is downloaded from the host PC, via Microsemi-Libero Flash programmer, to the DUT configuration memory. After each test is finished, the DUT configuration is read-back, via Microsemi-Libero flash programmer. The read-back verify function will indicated a pass-fail.

Table 19: List of files used for each DUA PLL WSR test

DUT	Time	Tester	Time
DUT_SHIFTREG_TOP_w_Resets_PLL_1000	10/29/16 20:24	rtg4_pll_shift_reg	10/29/16 19:16
DUT_SHIFTREG_TOP_w_Resets_PLL_1000_SET	10/29/16 20:25	rtg4_pll_shift_reg	10/29/16 19:16
New Shift Reg PLL Delay Nov 1	11/1/16 13:56	rtg4_pll_shift_reg	11/1/16 23:55
DUT_SHIFTREG_TOP_w_Resets_	11/1/16	rtg4_pll_shift_reg	11/1/16

DELAY_SET	17:58		23:55

Table 20: List of files used for each DUA Counter test

DUT	Time	Tester	Time
V5_2CounterswPLL_FAST	10/30/16 12:07	RTG4_counter_tester_2Counters	12/13/15 10:38

Table 21: List of files used for each DUA SRAM test

DUT	Time	Tester	Time
Memory_top_DUALPort	10/12/16 23:28	lcdt_sls_ramb_tester_top	10/13/16 0:18
Memory_top_DUT_SET	10/13/16 19:05	lcdt_sls_ramb_tester_top	10/13/16 0:18
Memory_top_SET	10/13/16 17:44	lcdt_sls_ramb_tester_top_micro_1024_cen	10/12/16 21:01
Memory_topMemory_Top1024_EDAC	10/12/16 23:09	lcdt_sls_ramb_tester_top_micro_1024_edac_v2	10/12/16 23:42

Table 22: List of files used for each DUA FIR test

DUT	Time	Tester	Time
DSP_TOP_CLASSICAL_CLKINT_ASYNCRST	10/30/16 18:30	dsp_tester_top	10/30/16 16:02
DSP_TOP_CLASSICAL_CLKINT_ASYNCRST_SET	10/30/16 18:56	dsp_tester_top	10/30/16 16:02
DSP_TOP_CLASSICAL_CLKINT_SYNCRESET_SET_NOV1	11/2/16 2:47	dsp_tester_top	11/1/2016 8:40:00 PM
DSP_TOP_CLASSICAL_SET	10/29/16 20:44	dsp_tester_top	10/13/16 16:37
DSP_TOPSyncReset (3)	10/24/16 15:00	dsp_tester_top	10/13/16 16:37

7.2.3 Procedures for running a test

The following sections and tables list the procedures required for running a test.

7.2.3.1 WSR

WSR tests vary by the following:

- Frequency of operation: frequency can vary from 5 MHz to 160 MHz. Frequency of operation is controlled by command A0.
- Data Pattern: Input data pattern can be all 0's, all 1's, and checkerboard. Data pattern is controlled by command 91.
- Halt: WSR DFFs are loaded with a data pattern while beam is turned off. Beam is turned on while clocks are static (however, registers are still enabled). Beam is turned off and the tester reads out WSR DFFs.

Table 23: Running a WSR Test (1st round and 2nd round with PLLs)

Action	Explanation
Beam is off	
Program tester (download bit file to tester)	Via LCDT JTAG.
Program DUT (download bit file to DUT)	Via DUT JTAG.
Hardware reset	
Command 01 x x x	Via LabView: LDCT command Soft Reset.
Command A0 nn nn x	Via LabView: Frequency Control.
Command 02 x x x	Via LabView: Start the tester/DUT system
Turn Beam on	FPGA tester will collect DUT outputs and determine if an SEU has affected operation. FPGA tester will send the information to the host computer system. Upsets can be observed via LabView window and Logic Analyzer.
Turn Beam off	Reset system after turning beam off and log information

Table 24: Running a WSR Test with Halt (1st round and 2nd round with PLLs)

Action	Explanation
Turn beam off	
Program tester (download bit file to tester)	Via LCDT JTAG.
Program DUT (download bit file to DUT)	Via DUT JTAG.
Hardware reset	
Command 01 x x x	Via LabVIEW: LDCT command Soft Reset.
Command 99 x x x	Via LabVIEW: LDCT command Soft Reset.
Command A0 nn nn x	Via LabVIEW: Speed Control.
Command 02 x x x	Via LabVIEW: Start the tester/DUT system

Command 04 x x x	Via LabVIEW: Halt command (make DUT clock static = 0)
Turn Beam on	No output will be observed because WSR clocks are static.
Turn Beam off	
Command 06 x x x	Via LabVIEW: Start the tester/DUT system : FPGA tester will collect DUT outputs and determine if an SEU has affected operation. FPGA tester will send the information to the host computer system. Upsets can be observed via LabVIEWwindow and Logic Analyzer.
Reset system and log information	

7.2.3.2 Counter Arrays

Counter array tests only vary by frequency of operation.

Table 25: Running a Counter Array Test

Action	Explanation
Turn beam off	
Program tester (download bit file to tester)	Via LCDT JTAG.
Program DUT (download bit file to DUT)	Via DUT JTAG.
Hardware reset	
Command 01 x x x	Via LabVIEW: LDCT command Soft Reset.
Command 99 x x x	Via LabVIEW: LDCT command Soft Reset.
Command A0 nn nn x	Via LabVIEW: Speed Control.
Command 02 x x x	Via LabVIEW: Start the tester/DUT system
Turn Beam on	FPGA tester will collect DUT outputs and determine if an SEU has affected operation. FPGA tester will send the information to the host computer system. Upsets can be observed via LabVIEWwindow and Logic Analyzer.
Turn Beam off	Reset system after turning beam off and log information

7.2.3.3 SRAM DUAs

SRAM tests do not vary by frequency or pattern.

Table 26: Running a Dynamic SRAM Test

Action	Explanation
Turn beam off	
Program tester (download bit file to tester)	Via LCDT JTAG.
Program DUT (download bit file to DUT)	Via DUT JTAG.
Hardware reset	
Command 01 x x x	Via LabVIEW: LDCT command Soft Reset.
Command 99 x x x	Via LabVIEW: LDCT command Soft Reset.
Command 02 x x x	Via LabVIEW: Start the tester/DUT system
Turn Beam on	FPGA tester will collect DUT outputs and determine if an SEU has affected operation. FPGA tester will send the information to the host computer system. Upsets can be observed via LabVIEWwindow and Logic Analyzer.
Turn Beam off	Reset system after turning beam off and log information

Table 27: Running a Halt SRAM Test

Action	Explanation
Turn beam off	
Program tester (download bit file to tester)	Via LCDT JTAG.
Program DUT (download bit file to DUT)	Via DUT JTAG.
Hardware reset	
Command 01 x x x	Via LabVIEW: LDCT command Soft Reset.
Command 99 x x x	Via LabVIEW: LDCT command Soft Reset.
Command 02 x x x	Via LabVIEW: Start the tester/DUT system
Command 04 x x x	Halt operation
Turn Beam on	DUT is in a halt state so LCDT is not monitoring output. However, LCDT is monitoring power/current of the DUT
Turn Beam off	Reset system after turning beam off and log information

Command 06 x x x	Start read/write operation after halt

7.2.3.4 FIR DUAs

FIR tests vary by frequency only.

Table 28: Running a Dynamic FIR Test

Action	Explanation
Turn beam off	
Program tester (download bit file to tester)	Via LCDT JTAG.
Program DUT (download bit file to DUT)	Via DUT JTAG.
Hardware reset	
Command 01 x x x	Via LabVIEW: LDCT command Soft Reset.
Command 99 x x x	Via LabVIEW: LDCT command Soft Reset.
Command A0 nn nn x	Via LabVIEW: Speed Control.
Command 02 x x x	Via LabVIEW: Start the tester/DUT system
Turn Beam on	FPGA tester will collect DUT outputs and determine if an SEU has affected operation. FPGA tester will send the information to the host computer system. Upsets can be observed via LabVIEWwindow and Logic Analyzer.
Turn Beam off	Reset system after turning beam off and log information

8. HEAVY ION TEST FACILITY AND TEST CONDITIONS

We performed heavy ion testing at two different facilities: Texas A&M Cyclotron Single Event Effects Test Facility (TAMU) and Lawrence Berkeley National Laboratories 88inch Cyclotron (LBNL).

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, 25 MeV/amu tune.
Flux: $1.0x10^4$ to $1.0x10^5$ particles/cm^2/s
Fluence: All tests will be run to 1 x 10^7 particles/cm^2 or until destructive or functional events occurred.
Test Temperature: Room Temperature.

Facility: Lawrence Berkeley National Laboratories 88inch Cyclotron, 16 MeV/amu tune.
Flux: $1.0x10^4$ to $1.0x10^5$ particles/cm^2/s
Fluence: All tests will be run to 1 x 10^7 particles/cm^2 or until destructive or functional events occurred.
Test Temperature: Room Temperature.

Power Supply Voltage: V_{cc} = 1.2V; V_{IO} = 2.5V

Table 29: TAMU LET Table

Ion	Energy (MeV/Nucleon)	Energy (MeV/Nucleon)	LET (MeV*cm^2/mg) at angle
Ne	25	1.8	3.6 at 60°
Ar	25	5.7	8.1 at 45°
Kr	25	20.6	29.5 at 45°

Table 30: LBNL LET Table

Ion	Energy (MeV/Nucleon)	Energy (MeV/Nucleon)
N	16	1.16
Ne	16	2.39
Si	16	4.35
Ar	16	7.27
V	16	10.9
Cu	16	16.5
Kr	16	25
Xe	16	49.3

8.1.1 Overview of Heavy-ion Accelerated Tests Performed at LBNL March 2016 and TAMU May 2016

The following is a summary (list) describing test structures and set-up conditions for heavy-ion RTG4 testing at LBNL (March 2016) and TAMU (May 2016).

- Test structures:
  - Windowed shift registers (WSRs) each DUT containing four separate WSR chains (WSR_0, WSR_4, WSR_8, WSR_{16}):
    - WSR chains with ASSD global reset. 800 DFFs per chain.
    - WSR chains with Synchronous global reset. 800 DFFs per chain.
    - WSR chains with no reset. 20,000 DFFs per chain.
  - Counters arrays:
    - 200 8-bit counters per counter array including 200 8-bit snapshot registers.
    - 2 counter arrays in one DUT.
    - Synchronous global reset is used.

        - Both counter arrays share the same clock and same global reset.
- Frequency of operation and data patterns:
    - Shift registers will have data input patterns varied: all 0's, all 1's, and checkerboard. Shift register frequency of operation will be varied from 2KHz to 160MHz.
    - Counter arrays will have frequency varied ranging from 5MHz to 50MHz.
- Halt function:
    - WSRs are loaded with a data pattern while beam is turned off. Beam is turned on while clocks are static (however, registers are still enabled). Beam is turned off and the tester reads out registers.
    - Only performed on shift register test structures.

8.1.2 Overview of Heavy-ion Accelerated Tests Performed at LBNL October 2016

The following is a summary (list) describing test structures and set-up conditions for heavy-ion testing at LBNL (October 2016).

- Test structures: uSRAM and LSRAM
- Frequency of operation and data patterns:
    - Frequency was not varied. Read and write memory access was at 2MHz.
    - Data patterns were always counters. The counter that is stored in an address location is equal to the lower 8-bits of the address.
- Halt function:
    - Halt tests were performed (static memory testing). The memory is loaded with a counter pattern. Afterwards the beam is turned on. When the beam is turned off, the memory location contents are read by the LCDT and then processed.

8.1.3 Overview of Heavy-ion Accelerated Tests Performed at TAMU October-November 2016

The following is a summary (list) describing test structures and set-up conditions for heavy-ion RTG4 testing at TAMU (October-November 2016).

- WSR, Counter, and FIR DUA Test structures:
    - PLL Windowed shift registers (WSRs) each DUT containing four separate chains (Chain0-WSR_0, Chain1-WSR_0, Chain2-WSR_0, Chain3-WSR_0) topology.
        - There were DUAs that contained chains with resets and with 1000 DFFs per chain.
        - There were DUAs that contained chains with no reset and 20,000 DFFs per chain.
    - Counters array Topology:
        - 200 8-bit counters per counter array including 200 8-bit snapshot registers.

        - 2 counter arrays in one DUT.
        - Synchronous global reset is used.
        - Both counter arrays share the same clock and same global reset.
    - Dual Redundant FIR Topology:
        - 2 FIR chains. Each containing 100 18x18 HMACC blocks.
        - Both chains share the same clock (everything is synchronous).
        - Both chains share the same reset.
    - Frequency of operation and data patterns:
        - Shift registers will have data input patterns varied: all 0's, all 1's, and checkerboard. Shift register frequency of operation varied from 1MHz to 120MHz.
        - Counter arrays will have frequency varied ranging from 5MHz to 100MHz.
        - Dual redundant FIR chains varied from 1MHz to 100MHz.
    - Halt function:
        - WSRs are loaded with a data pattern while beam is turned off. Beam is turned on while clocks are static (however, registers are still enabled). Beam is turned off and the tester reads out registers.
        - Only performed on shift register test structures.
- SRAM DUA Test Structures:
    - uSRAM with one write port and two read ports. 1024 memory locations.
    - uSRAM with EDAC and one write port and two read ports. 1024 memory locations.
    - LSRAM with one read port and one write port. 65536 memory locations.

9. HEAVY-ION ACCELERATED TESTING DATA ANALYSIS

As previously mentioned, SEU cross-sections are measured by the number of errors normalized by the number of particle exposure (particle fluence). See Equation (1). This is an appropriate measurement, when testing flushable designs because a significant number of upsets will occur per particle event space.

From Equation (2), we categorize test structure data as follows: configuration upsets, functional data path, and global routes (or SEFIs).

9.1 RTG4 Flash Configuration Cells

9.1.1 Configuration Cell failures

In the Rev C version of the RTG4, no configuration failures were observed over all testing (>600 tests). Tests included LETs = 49.3MeVcm^2/mg.

9.1.2 Programmability failures

No programmability failures were observed during testing. Re-programmability failures were observed in the ProASIC3 at LETs >50MeVcm^2/mg. NEPP tests included up to LETs = 49.3MeVcm^2/mg. Higher LET values should be investigated to verify that the RTG4 does not experience similar behavior as the ProASIC3 at higher LETs.

It should be noted that programmability failures were observed once the DUT was dosed to greater values than the manufacturer indicates failure. This is because manufacturer TID is based off of Cobalt 60 sources or X-ray sources. Their dosage effects are more severe than heavy-ion dose effects.

9.2 Description of WSR Halt Tests (1st Round (no PLL) and 2nd round (with PLLs) of testing)

Designs are held in a static state because the clock is suspended. During a halt test, after the WSR string is loaded, the clock is held in a logic ‘0’ state. All DFFs are enabled but do not receive clock edges during halt state. Upsets can come from a global route or an internal DFF SEU (i.e. broken TMR). The halt test is used to test all of both.

It is important to note that clock tree SETs may not reach all DFFs. This could be caused by the following:

- An SET may not have been generated with enough strength to propagate to all DFFs.
- An SET may be generated on an internal clock tree leaf and only affect a subset of all DFFs.

Figure 42 illustrates the WSR string and timing diagrams for a WSR halt test with a checkerboard pattern. It is noted that if a test were performed with all ‘1’s or all ‘0’s then a clock SET would only cause the DFF to capture the same data and no system error would be occur upon the clock SET.

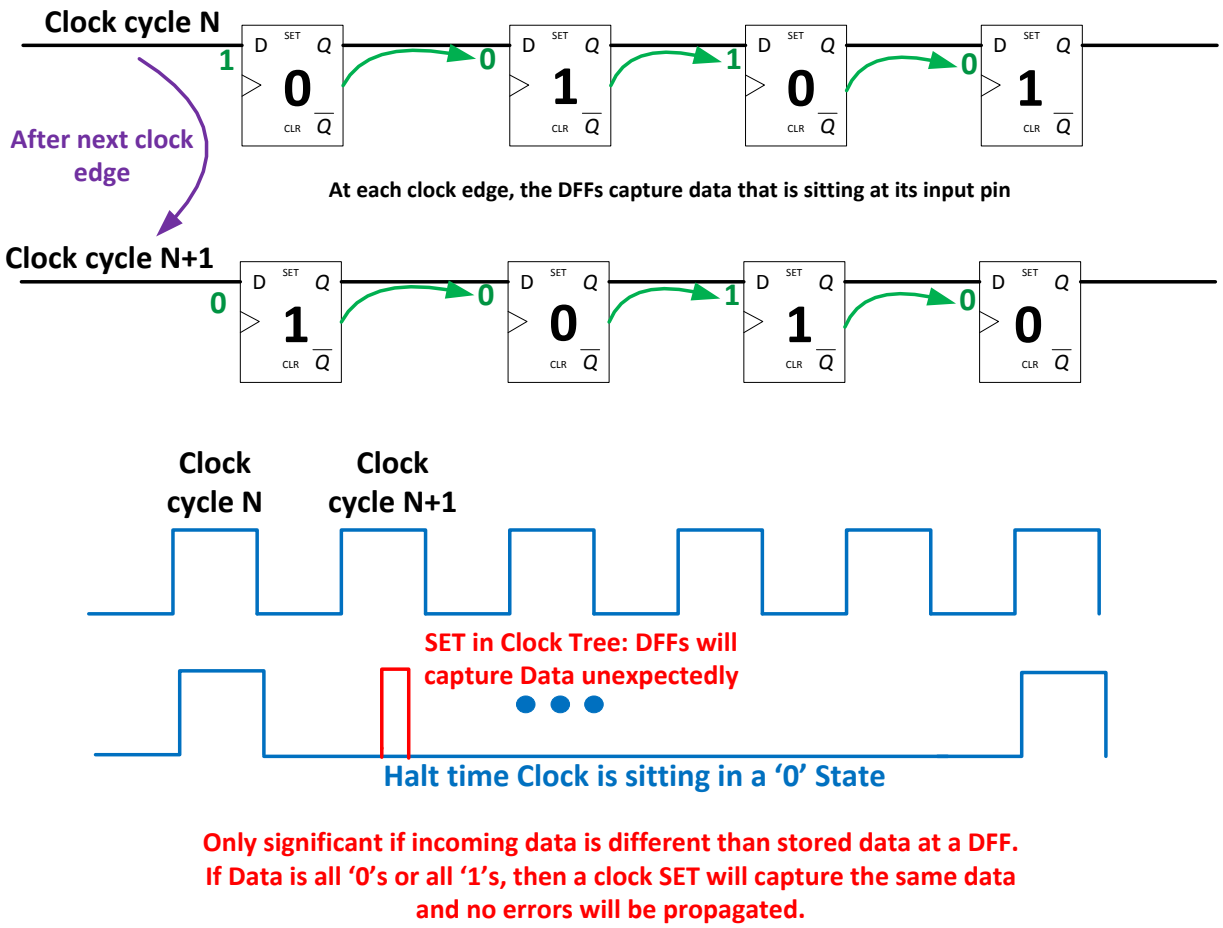


Figure 42: Halt Test timing diagram and DFF capture for a WSR checkerboard pattern. If an SET occurs during the halt state (while the clock is low), any DFFs that are affected by the clock SET can capture data incorrectly via the clock SET edge.

9.2.1 WSR Halt Test Results

- No SEUs were observed with All 1's and All 0's tests. This is as expected because, during a clock SET, the same data value is captured.
- SEUs were observed starting at LET = 5.1 MeV*cm^2/mg and a fluence of 10^7 particles/cm^2 with the following WSR configurations:
  - Normal I/O (acting as a clock) connected to a CLKINT.
  - OSC connected to PLL connected to a CLKINT.
- No SEUs were observed (up to 20 MeV*cm^2/mg) for the following:
  - DGBIO directly connected to a CLKBUF.
  - DGBIO connected to PLL connected to CLKINT.
- SET filters did not make a difference. This is as expected because data-path SETs cannot be captured (DFFs are not clocked during halt).

- No upsets were observed with fluences less than $5x10^6$.
- TMR of the DFFs does not break. All WSR string upsets come from the clock trees.

Cross sections were not calculated for this data because more testing needs to be performed to determine at which fluence the upsets start to occur.

9.3 WSR 1st round heavy ion tests

During WSR heavy ion tests, WSR input patterns and frequencies were varied. For data analysis, comparisons are made to investigate trends in adding combinatorial logic within data paths; and frequency effects to SEE susceptibility.

9.3.1 WSR 1st Results

Figure 43 shows the results for 4 clk 4 reset with SET filter. Results are across all patterns and LET values. Data results are from an input frequency = 100MHz only. It is important to note that the addition of combinatorial logic can make a difference during testing. As combinatorial logic is added to the data path, SEU cross sections will increase.

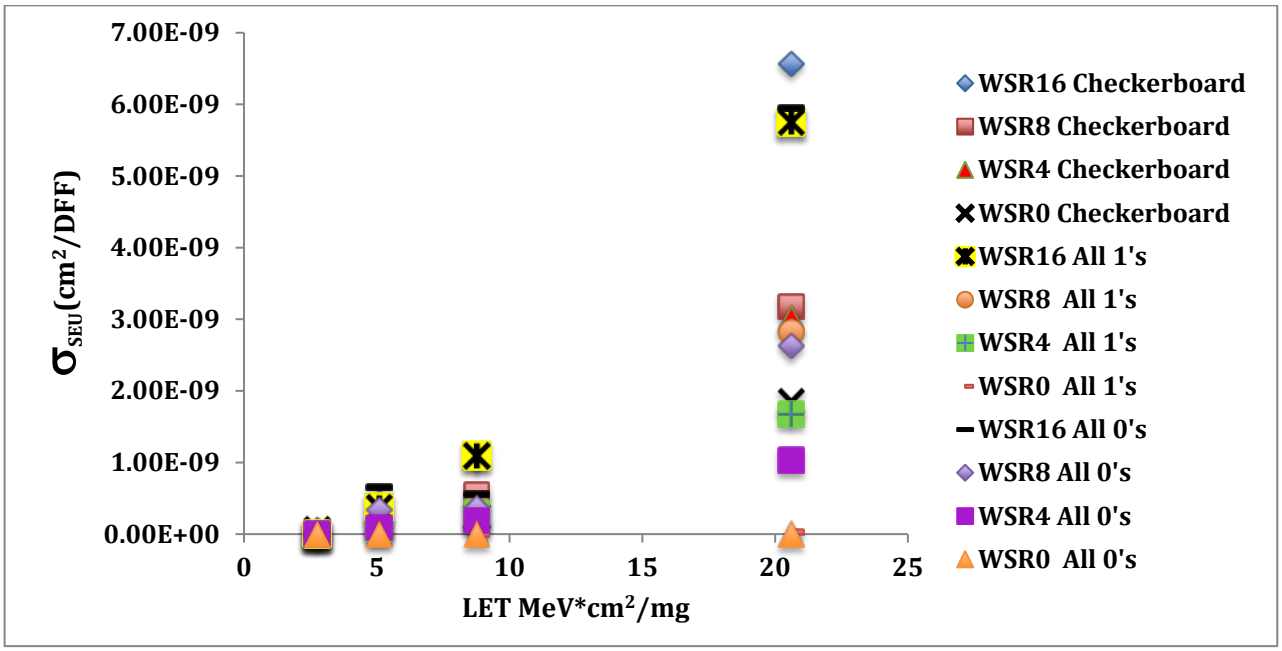


Figure 43: 4 CLK 4 RST FILTER versus LET at 100 MHz

Figure 44 shows the difference between turning the DFF SET filter on versus no DFF SET filter in the data path. All data patterns are shown. Data in Figure 44 are only at LET=20.6MeVcm^2/mg. There is a clear improvement with using an SET filter – about a decade of difference in SEU cross sections. As LET increases, the strength of the SET filters start to decrease. However, at LET=20.6MeVcm^2/mg the SET filters still provide benefits.

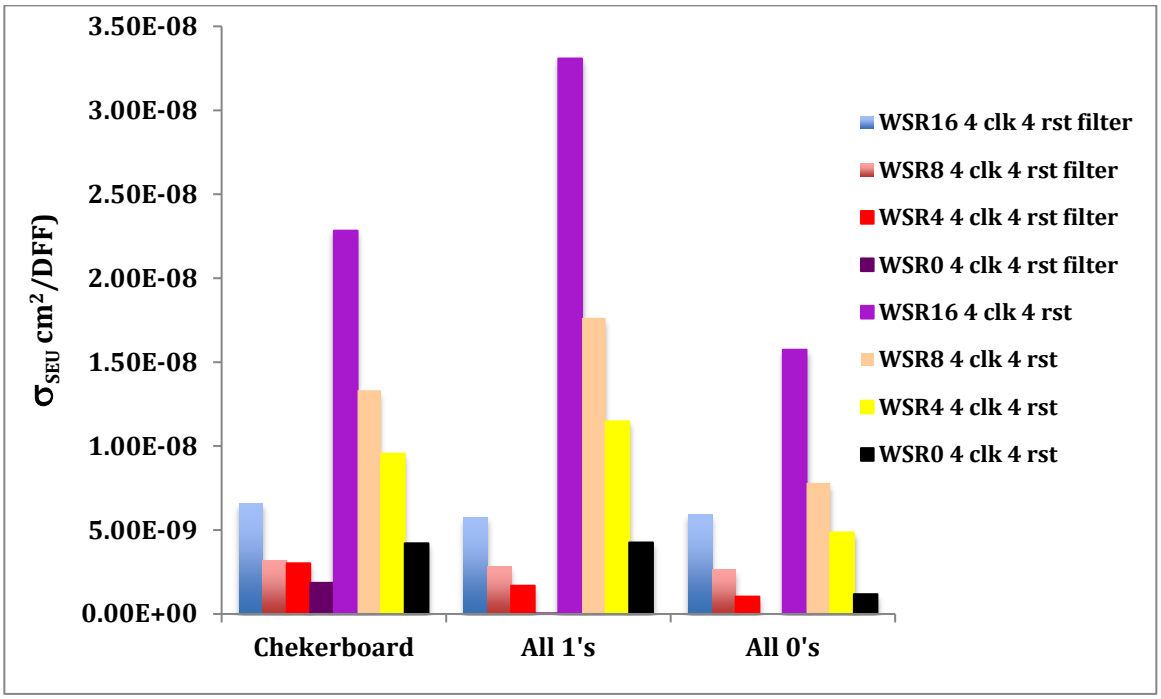
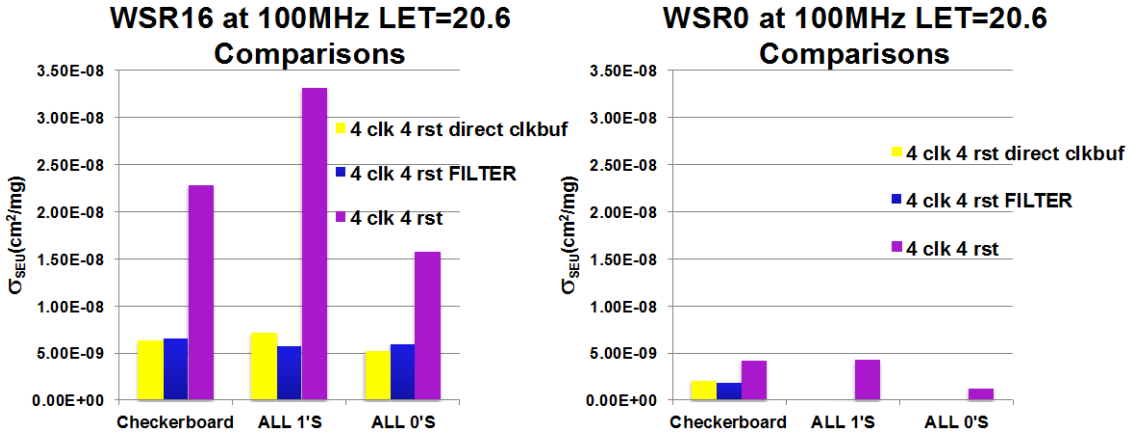


Figure 44: Comparing WSR Chains: 4 clk 4 rst with Filter and 4 clk 4 rst …100MHz with LET = 20.6MeVcm^2/mg



WSR_{16} has higher probability of data-path SET generation.

WSR_{16} Pattern	Direct/ filter	Direct/ no filter
Checker	0.96	0.28
All 1's	1.24	0.26
All 0's	0.88	0.33

Tables represent Ratios of SEU cross sections.

WSR_0 Pattern	Direct/ filter	Direct/ no filter
Checker	1.1	0.47
All 1's	1.0	0.007
All 0's	1.0	0.025

Figure 45: Comparing 4 clk 4 rst DUT Variations: How much Better Is A Direct Connection to CLKBUF and/or A SET Filter?

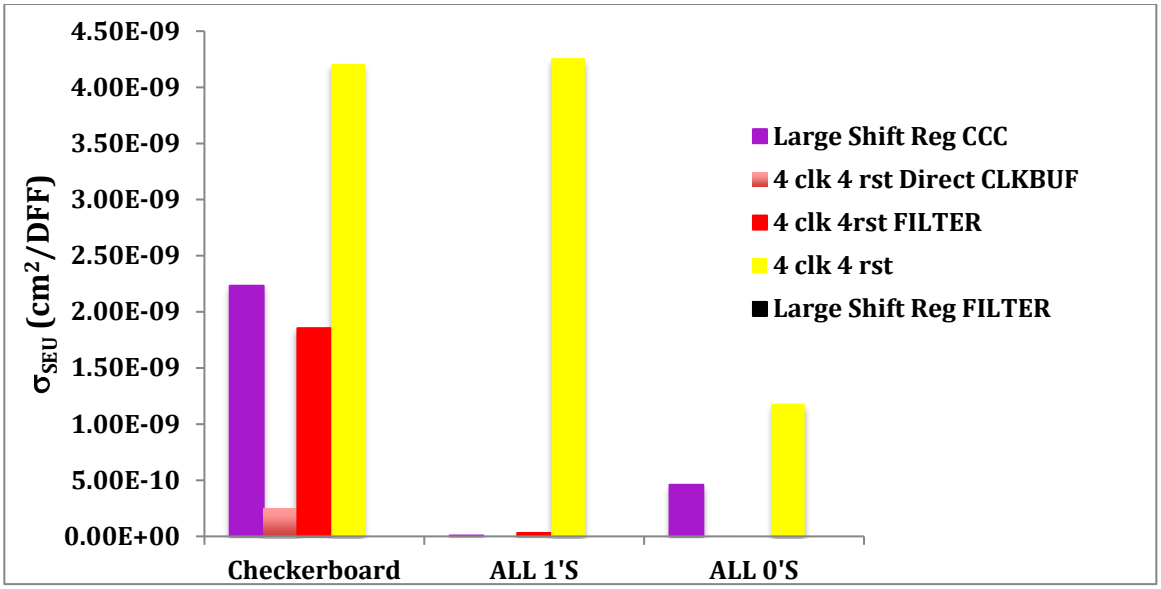


Figure 46: Large WSRs : Comparison of WSR_0 SEU Cross Sections at 100MHZ at LET = 20MeV*cm^2/mg

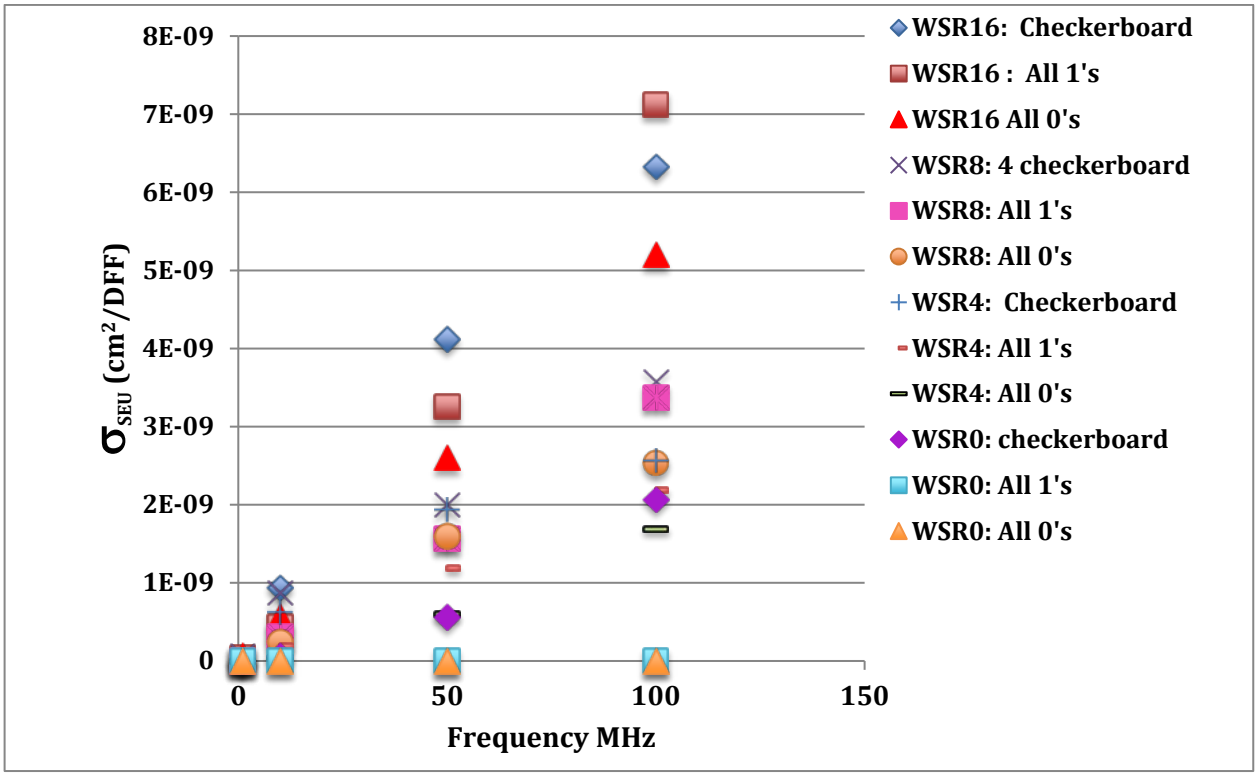


Figure 47: 4 Clk 4 rst Direct CLKBUF SEU Cross Sections versus Frequency at LET = 20.6 MeVcm^2/mg

Figure 47 shows data at LET=20.6MeVcm^2/mg across Frequency. This look at data shows how important it is to test across frequency for this device. Based off of the information in Berg M.," FPGA SEE Test Guidelines", NASA Radiation Effects and Analysis Group, the following are characteristics of WSR SEE susceptibility in configuration SEE hardened FPGA devices. The information is used to help analyze the data and verify component mitigation efficacy:

- If the DFFs are well mitigated, then the most susceptible paths will be the data path and the global clock paths. In this case, for a WSR:
    - The data path SET contribution to system error will be directly proportional to frequency (i.e., as frequency increases, SEU cross sections increase).
    - The data path SET contribution to system error will be directly proportional to number of combinatorial logic components in the data path (when they are not in a logic mask state); i.e., as combinatorial logic increase within data paths, SEU cross sections increase.
- If the DFFs are not well mitigated, then the most significant contribution to SEE susceptibility will be from the DFFs and the clock trees. The SET contribution would be negligible in comparison. In this case, due to the topology of a WSR and synchronous data capture, SEE system susceptibility is inversely proportional to frequency. It is important to note that although DFF SEU error rates will increase as frequency increases, the system error rate will not. This is because of how synchronous data capture is designed and the data path delay will mask DFF SEUs from their next stage as frequency increases.

Data in Figure 43 through Figure 46 show that for the RTG4 Rev C, as frequency increases and as combinatorial logic gates increase, the WSR (system) SEE susceptibility increases (SEU cross sections increase). This suggests that the DFFs are well mitigated and that system errors are mostly coming from data path SET capture and global routes.

9.4 Global Routes and PLL WSR Heavy Ion Tests (2nd Round) Results

9.4.1 DFF SEUs with respect to a variety of clock sources

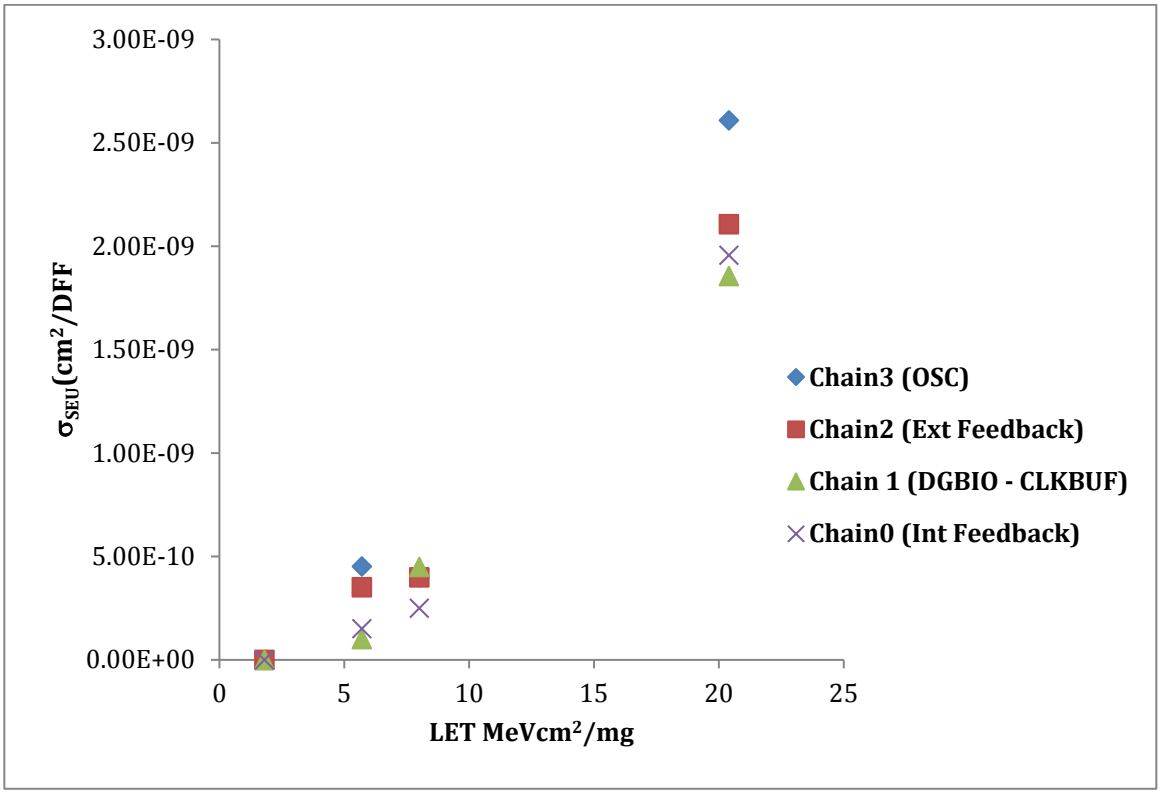


Figure 48: WSR_PLL_1000_SET SEU DFF cross sections across LET. All chains are WSR_0.

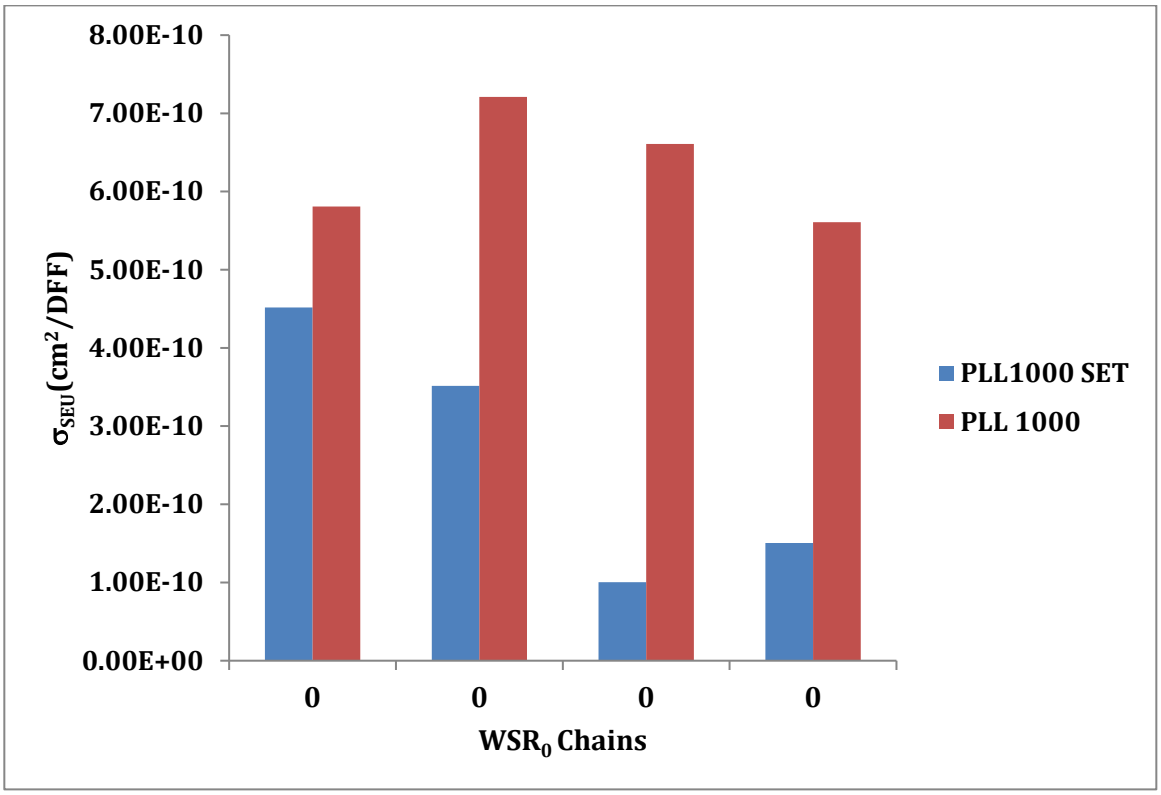


Figure 49: Comparison of WSR_PLL_1000_SET and WSR_PLL_1000 at an LET = 5.7MeVcm^2/mg

Figure 48 and Figure 49 show SEU data for WSR_PLL_1000_SET and WSR_PLL_1000. Because all chains are WSR_0, there is some improvement from the DFF SET filter; but not as much as if there were significant amount combinatorial logic between the DFF stages. As previously mentioned, although chains are WSR_0, there is still hidden combinatorial logic (buffers) between the DFF stages. Hence, there will be some data path SETs.

Data show that the most significant source of error for WSR_0 data paths with a DFF SET filter is the clock tree.

9.4.2 Global route overview

Summary of global route results starting from best performance:

- Direct clock I/O had the lowest SEU susceptibility (best performance.)
- Clock conditioning circuit had higher SEU susceptibility than direct clock I/O. However, performance can still be acceptable for critical missions.
- TMR clock conditioning circuit (TMR PLL) did not appear to reduce susceptibility and might have higher susceptibility at higher frequencies. Requires a power cycle with loss of lock.
- Internal oscillator clock is SEU soft and should not be used in critical circuits.

9.5 Counter Heavy Ion Tests

9.5.1 Description of Heavy Ion RTG4 Counter Tests

The counter tests were run across LET and Frequency.

9.6 Results

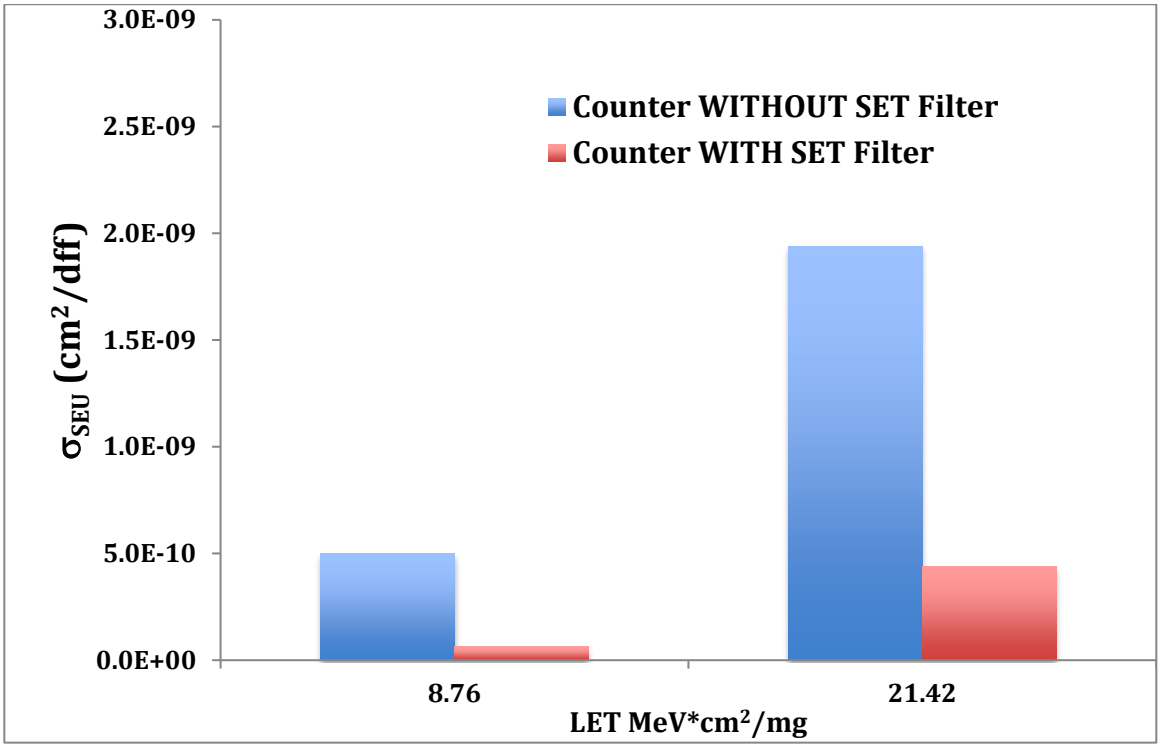


Figure 50: Rev C Counter Arrays Single Bit s_{SEU}s: without SET Filter versus with SET Filter at 50MHz .

Counter SEU cross-sections are lower than the corresponding (i.e., with filter or without) WSRs with checkerboard. Only counter-bits that change at the frequency of a checkerboard are bit-0 of each counter. As the bit-number of each counter increases, the bit frequency is decreased by a factor of 2.

Once again, the SET filter makes a significant difference. Counters were tested at 1MHz, 5MHz, 10MHz, 50MHz, and 100MHz. Upsets were not observed below 50MHz below an LET of 20MeV*cm^2/mg.

9.7 RTG4 Internal SRAM Heavy Ion Tests

9.7.1 Description of Internal SRAM Heavy Ion Tests

Tests were run in dynamic mode and static mode. In a dynamic memory test, the SRAM is continuously read and written during DUT beam exposure. In a static test, no reads or writes occur while during DUT beam exposure.

A distinction is made between single bit upsets and multiple bit upsets to help determine the efficacy of the SRAM EDAC circuitry.

9.7.2 LSRAM Results

Referencing Figure 51 and Figure 52, it is shown that there is no difference between DFF SET turned on versus DFF SET filter turned off. It can also be seen that the total bit upsets for dynamic tests versus static tests are statistically equivalent.

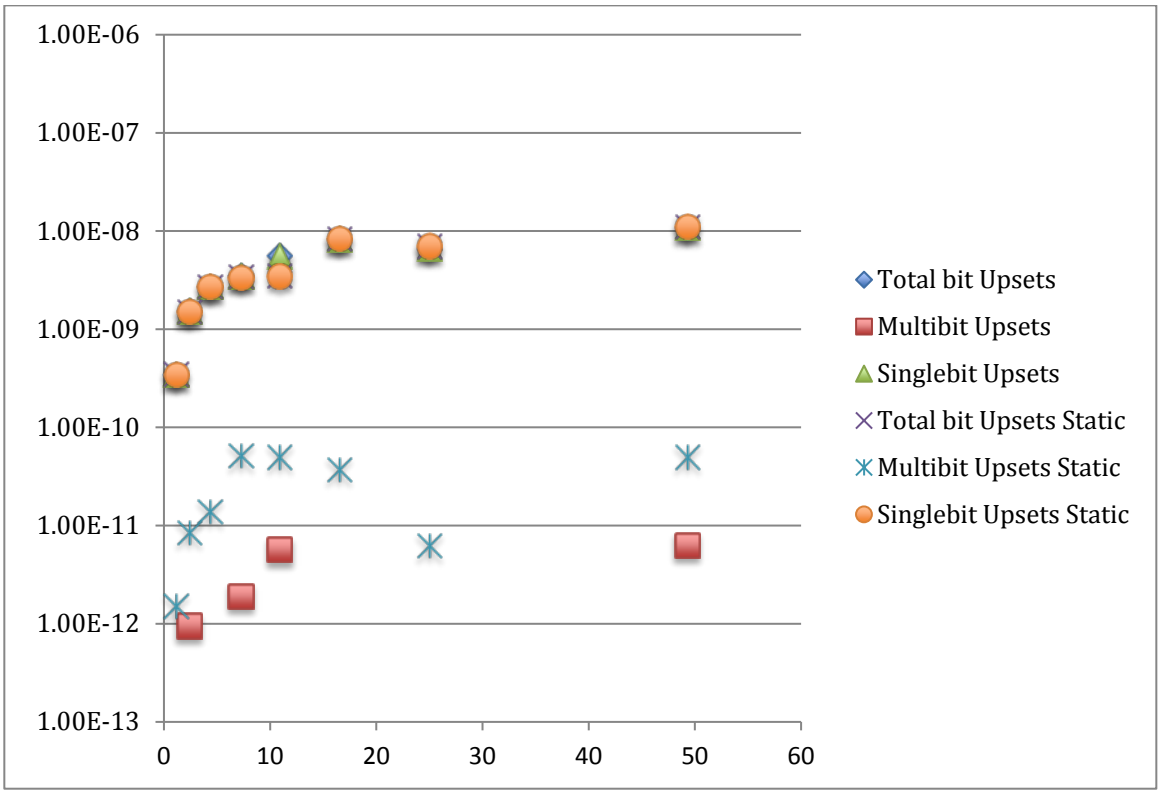


Figure 51: Large SRAM SEU Cross Sections across LET. All memory patterns are 8-bit counters. The stored 8-bit counter is equivalent to its address' lower 8-bits.

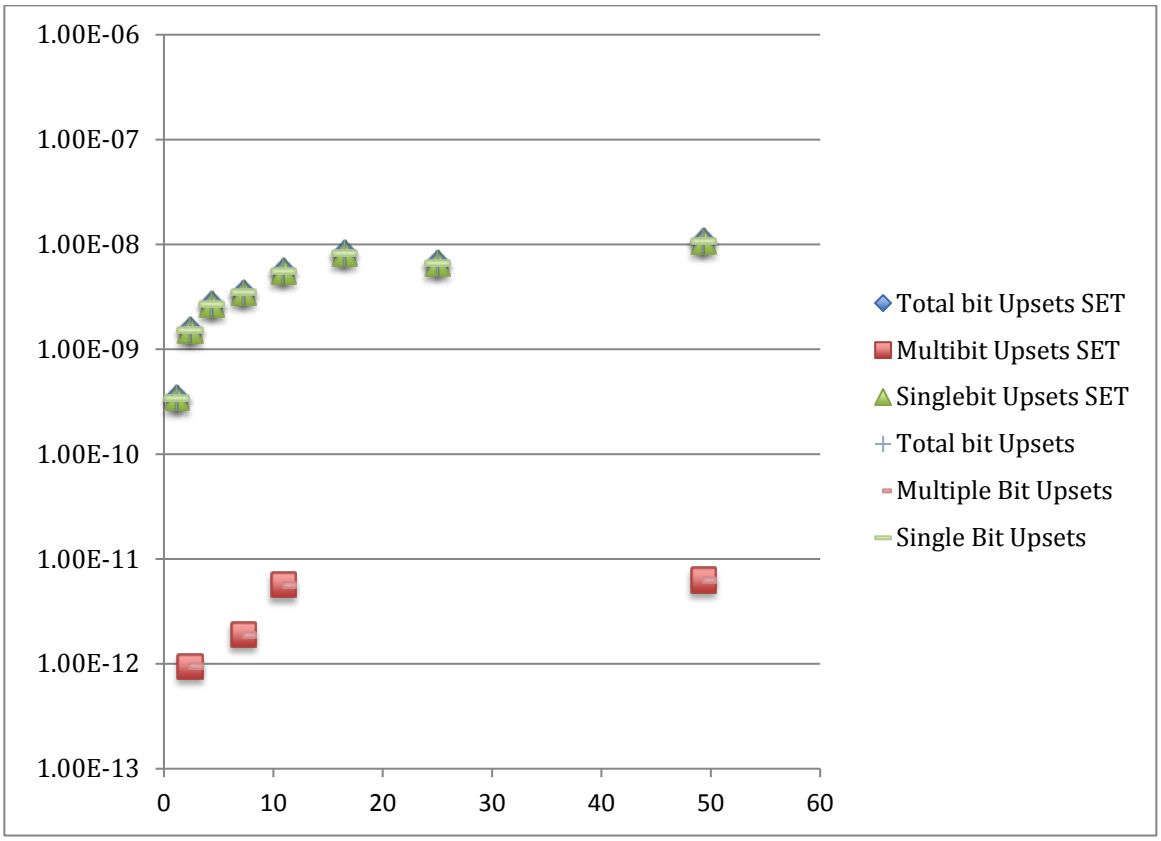


Figure 52: Large SRAM SEU Cross Sections across LET. A comparison of LSRAM with DFF SET filters turned on versus DFF SET filters turned off. All memory patterns are 8-bit counters. The stored 8-bit counter is equivalent to its address' lower 8-bits.

9.7.3 uSRAM Results

Figure 53 shows SEU data for the RTG4 internal uSRAM. Only one error was observed during dynamic testing of EDAC uSRAM. This is true across all LET.

Referencing Figure 53, there is a given number of single bit upsets and multiple bit upsets. No multiple bit upsets were observed during dynamic testing. Hence, dynamic EDAC performs as expected (practically no system errors). However, during static mode, there is a significant number of multiple bit upsets. This is most likely due to accumulation of SEUs over fluence. One would expect the total bit SEU cross section for uSRAM EDAC static mode to be statistically equivalent to the uSRAM multiple bit (no EDAC) SEU cross section. Alternatively, this is not true. The total bit EDAC static SEU cross is equivalent to the single bit EDAC upsets. This is a result of fluence. If testing to a fluence lower than $5x10^6$, in static mode, the EDAC circuitry is able to correct all data. However, at a fluence equal to 10^7, the EDAC breaks down. This will be further investigated.

As a summary, the EDAC circuitry works well if the memory will be occasionally written and is not sitting statically for a significant amount of time.

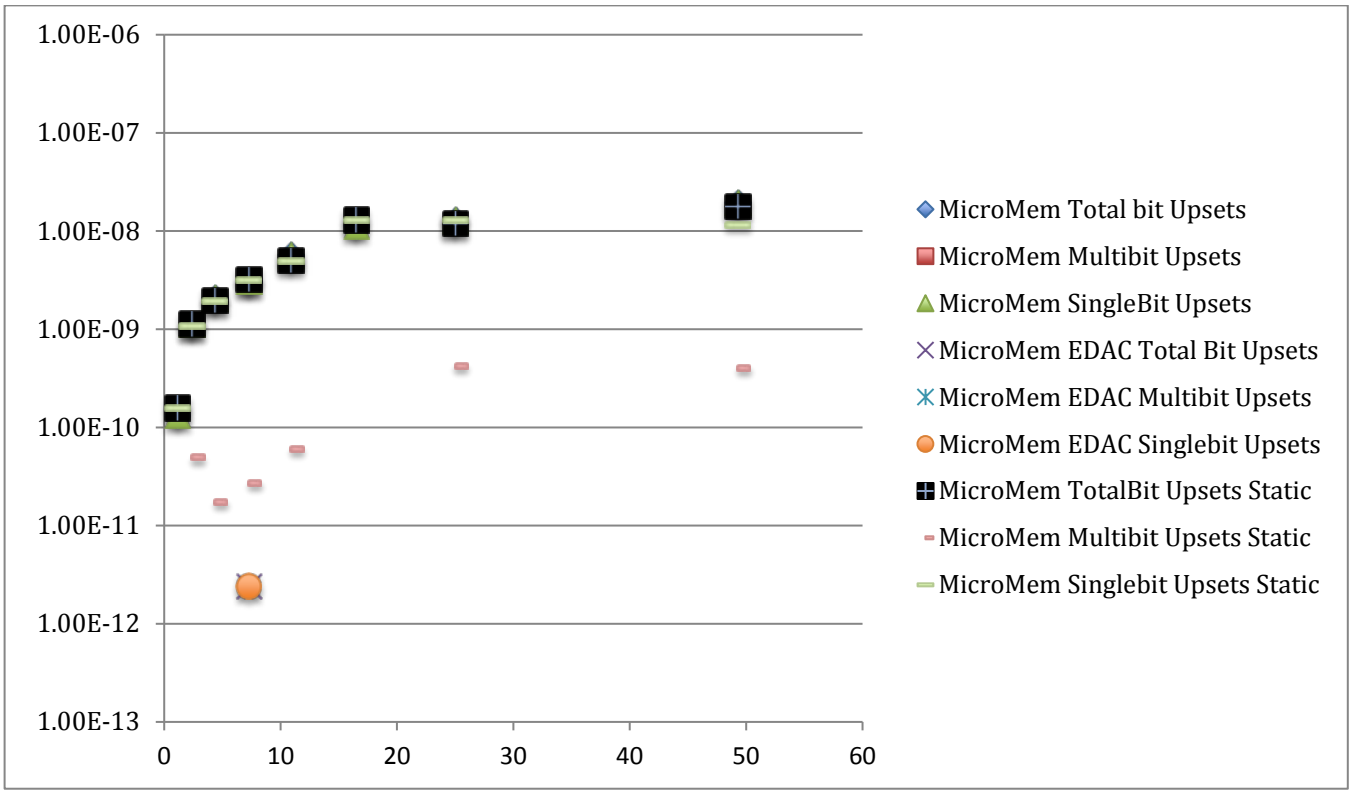


Figure 53: uSRAM SEU cross sections across LET.

9.8 DSP Heavy Ion Testing

Mathblocks (DSPs) were configured as: (a) 18x18 multiply adders (no feedback within the mathblock) or (b) 18x18 multiply accumulators (feedback within the mathblock). There was no significant difference in the SEU response between the DSP block configurations. However, SEUs in the accumulator version (with feedback) would cause the dual redundant structures to permanently lose track of each other during a run. Alternatively, with the adder version, SEUs would only cause the dual redundant chains to reflect a temporary error. This is because the adder configurations are flushable circuits.

Configuration (a) and configuration (b) were tested with SET filter on and SET filter off. The calculated SEU cross-sections are illustrated in Figure 54. At low LETs, there is a significant difference between SEU cross sections. As LET increases, the cross sections (SET filter on versus SET filter off) start to approach each other. This is as expected because as LET increases, the width of SETs increases and hence breaks the SET filter.

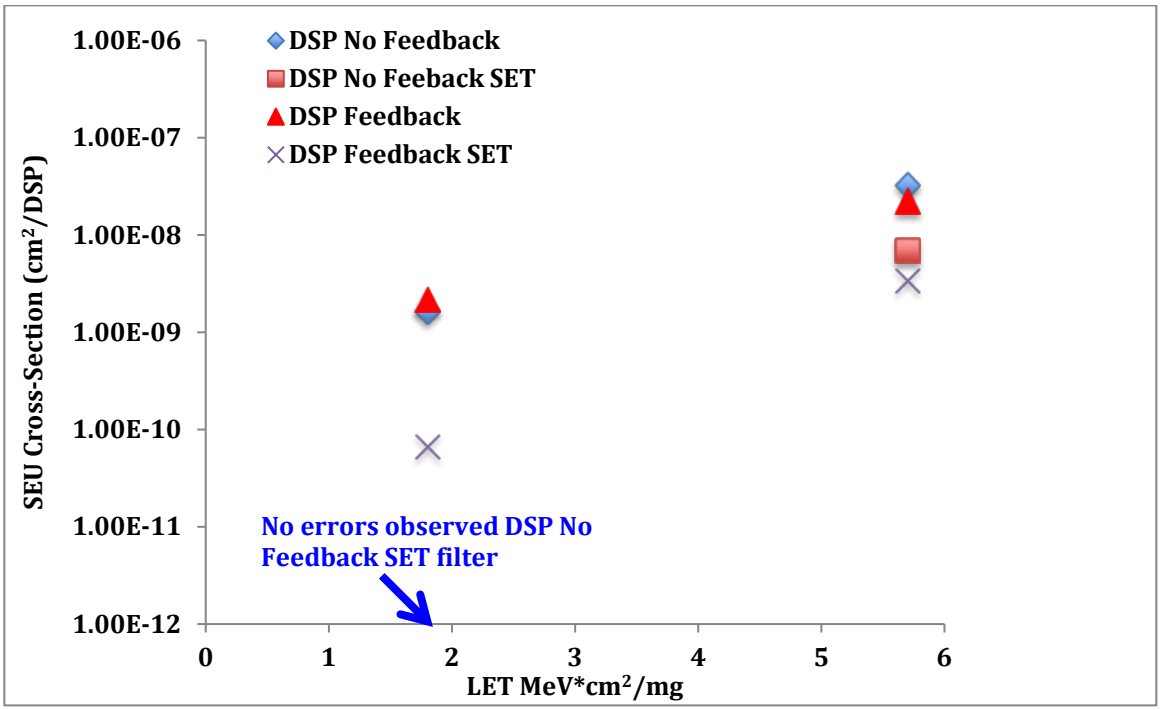


Figure 54: SEU Cross-sections for DSP Blocks in configured in a variety of topologies.

10. COMPARISON OF NEPP RTG4 TO NEPP PROASIC3 HEAVY-ION DATA

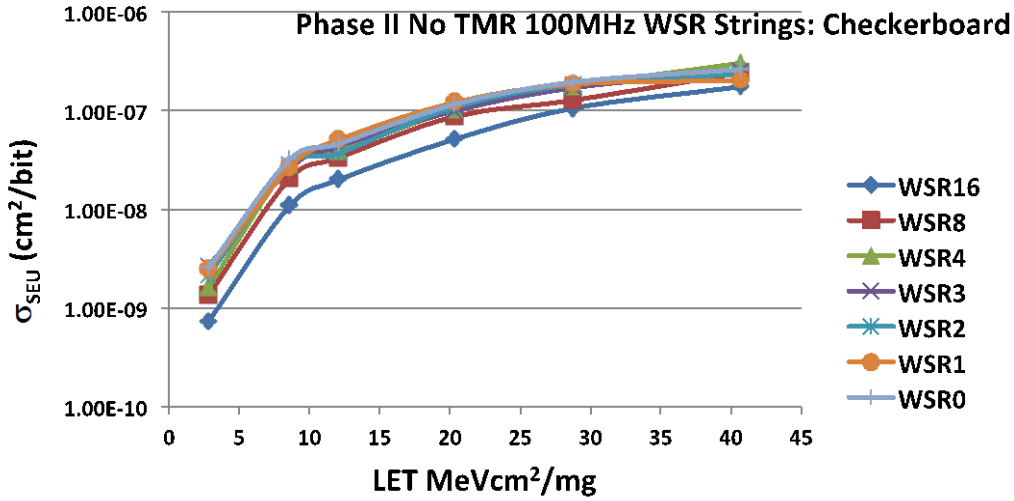


Figure 55: ProASIC3 Heavy-ion data. Data pattern is checkerboard taken at 100MHz

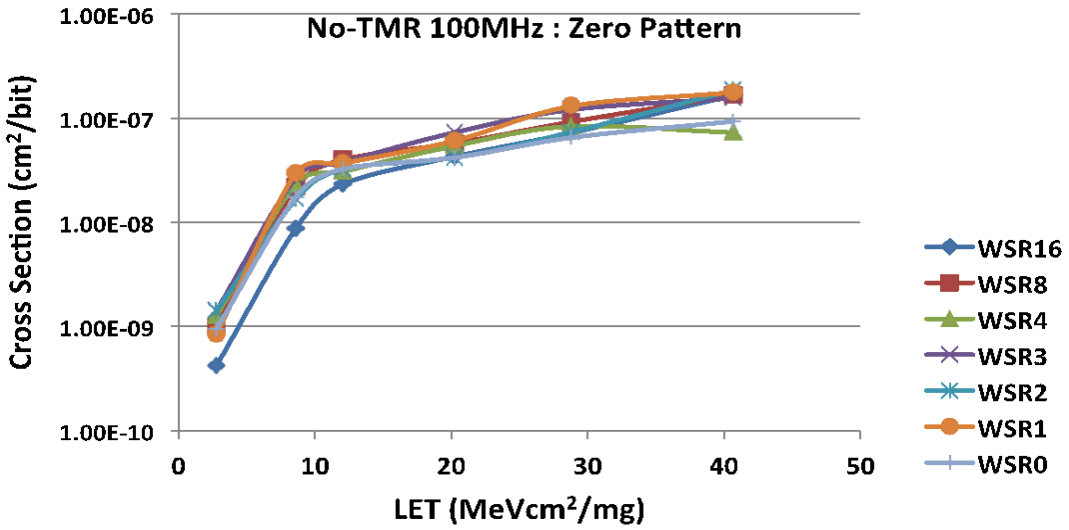


Figure 56: ProASIC3 Heavy-ion data. Data pattern is All 0's taken at 100MHz

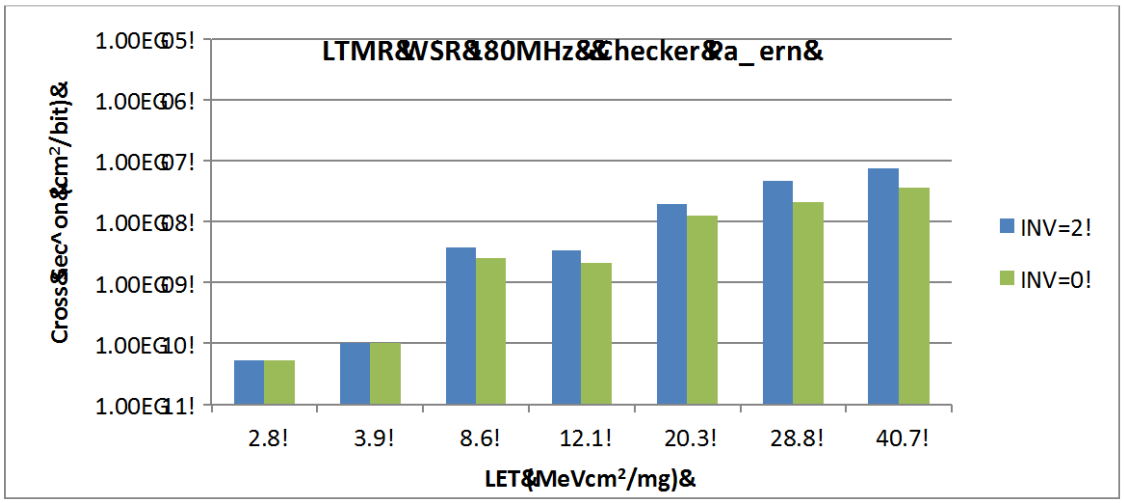


Figure 57: ProASIC3 WSR_0 and WSR_2 circuits. Data pattern is checkerboard taken at 180MHz. LTMR was manually inserted per DFF.

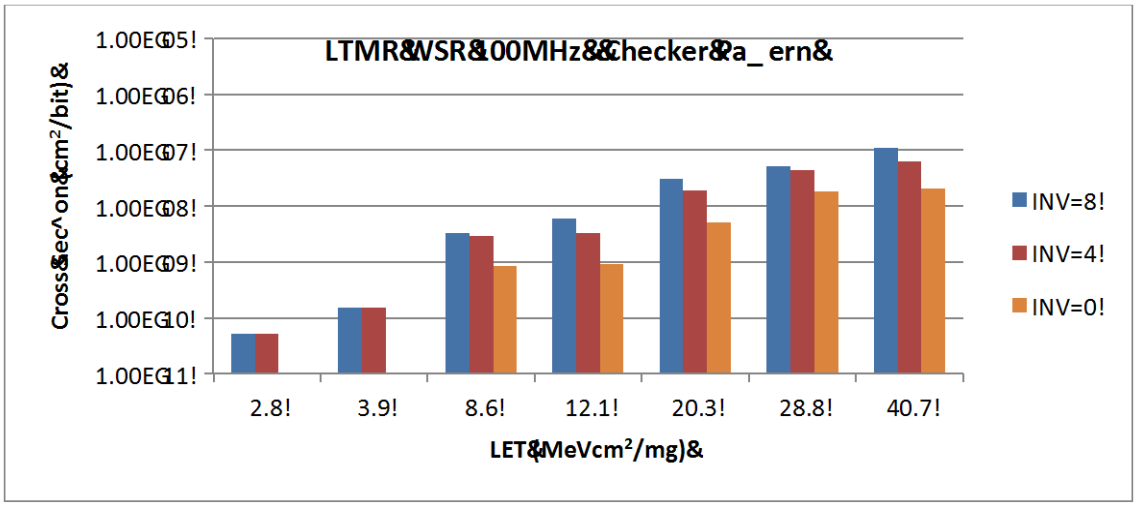


Figure 58: ProASIC3 WSR_0, WSR_4, and WSR_8 circuits. Data pattern is checkerboard taken at 100MHz. LTMR was manually inserted per DFF.

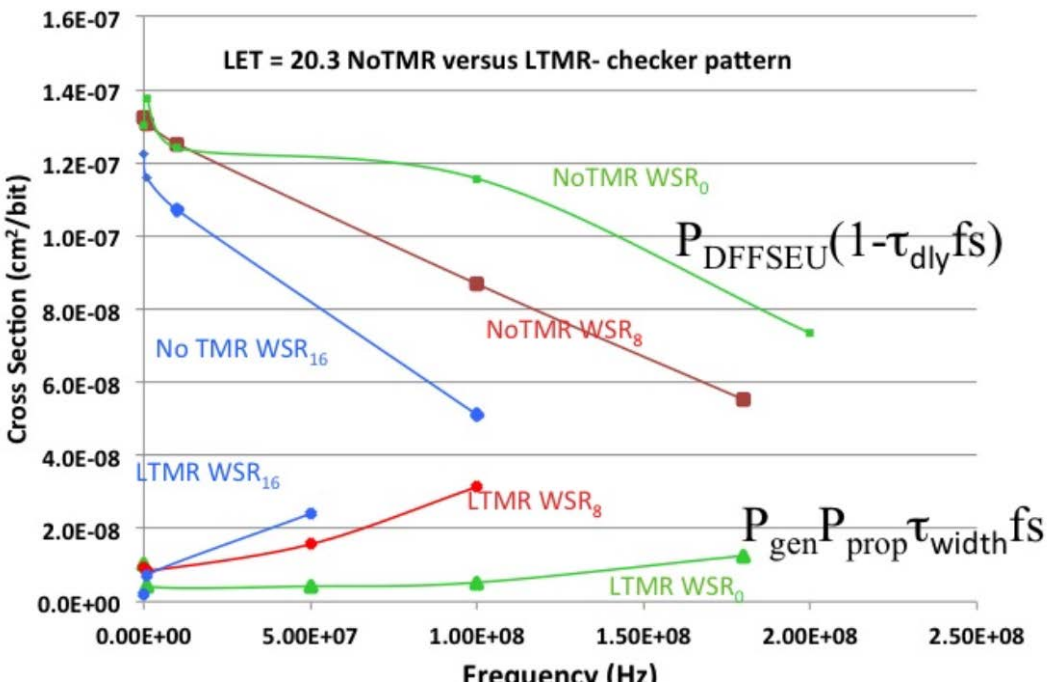


Figure 59: Comparison of ProASIC3 heavy-ion σ_{SEU} data: LTMR versus No-TMR.

The ProASIC3 devices were tested with No-TMR and LTMR. ProASIC3 data are illustrated in Figure 55 through Figure 59. When inserting the LTMR circuits in the ProASIC3 WSRs, σ_{SEU}s were reduced to the order of RTAX series devices at lower LETs. As LET increases, global upsets (from clocks) significantly increase ProASIC3 σ_{SEU}s.

ProASIC3 data is currently compatible to RTG4 Rev B. heavy-ion data.

11. CONCLUSION

No SEL or re-programmability problems observed. However, highest LET used during this test campaign was only 20.6 MeVcm^2/mg. More testing to come.

Selection of frequency and data pattern for WSR testing produced a wide range of SEU results. This shows the importance of reporting frequency and data pattern. In addition, frequency testing caused NEPP data to drastically differ from Microsemi data.

On-set for the RTG4 was lower than expected. This suggests that the device was more susceptible than expected during heavy-ion testing. This suggests that the SET filters are not being effective for the RTG4 Rev B device. In addition, there are potentially some additional unhardened buffers being inserted into the clock and data path.

Halt testing data uncovered a problem in the DFF clock circuitry susceptibility.

Comparisons to other Microsemi FPGA products used in space missions has been provided in this report:

- The full family of RTAXs has a higher on-set than RTG4.
- Theoretically unexpected because of the use of SET filters.
- However, the implementation of the filters is questionable.
- RTAX4000D has lowest susceptibility because Microsemi fixed the block buffer hardening.
- The ProASIC3 family with LTMR insertion had similar heavy-ion results as the RTG4.

12. APPENDIX 1:

[1] Actel Datasheet: “RTAX-S/SL RadTolerant FPGAs” http://www.actel.com/documents/RTAXS_DS.pdf, V5.2, October 2007.
[2] M. Berg “An Analysis of Single Event Upset Dependencies on High Frequency and Architectural Implementations within Actel RTAX-S Family Field Programmable Gate Arrays,” IEEE Trans. Nucl. Sci., vol. 53, n° 6, Dec. 2006.
[3] M. Berg “Trading Application Specific Integrated Circuit (ASIC) and Field Programmable Gate Array (FPGA) Considerations for System Insertion”, NSREC Short Course, Quebec City, CN, July 2009
[4] M. Berg et. al. RTAX-s/SL Test Report
[5] Microsemi white paper: “Mitigation of Radiation Effects in RTG4 Radiation- Tolerant Flash FPGAs,” WP0191 White Paper, April 2015.
[6] J. J. Wang, Nadia Rezzak, and Durwyn Dsilva, “RTG4 Radiation Test Results and Test Plans,” presented at Microsemi Space Forum 2015.