A New Approach to System-Level Single Event Survivability Prediction

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Acronyms

- Combinatorial logic (CL)
- Commercial off the shelf (COTS)
- Complementary metal-oxide semiconductor (CMOS)
- Device under test (DUT)
- Edge-triggered flip-flops (DFFs)
- Electronic design automation (EDA)
- Error rate (λ)
- Error rate per bit(λ_{bit})
- Error rate per system(λ_{system})
- Field programmable gate array (FPGA)
- Global triple modular redundancy (GTMR)
- Hardware description language (HDL)
- Input – output (I/O)
- Intellectual Property (IP)
- Linear energy transfer (LET)
- Mean fluence to failure (MFTF)
- Mean time to failure (MTTF)
- Number of used bits (#Usedbits)
- Operational frequency (fs)
- Personal Computer (PC)
- Probability of configuration upsets ($P_{configuration}$)
- Probability of Functional Logic upsets ($P_{functionalLogic}$)
- Probability of single event functional interrupt (P_{SEFI})
- Probability of system failure (P_{system})
- Processor (PC)
- Radiation Effects and Analysis Group (REAG)
- Reliability over time (R(t))
- Reliability over fluence ($R(\Phi)$)
- Single event effect (SEE)
- Single event functional interrupt (SEFI)
- Single event latch-up (SEL)
- Single event transient (SET)
- Single event upset (SEU)
- Single event upset cross-section (σ_{SEU})
- System on a chip (SoC)
- Windowed Shift Register (WSR)
- Xilinx Virtex 5 field programmable gate array (V5)
- Xilinx Virtex 5 field programmable gate array radiation hardened (V5QV)

Problem Statement and Abstract

- The process for application of single event upset (SEU) data used to characterize system performance in radiation environments needs improvement.
- We are investigating the application of classical reliability performance metrics combined with standard SEU analysis data to improve system survivability prediction.

This presentation is a simplified approach for SEU data extrapolation to complex systems. Future work will incorporate additional details.

Background (1) : FPGA SEU Susceptibility

SEU Cross Section (σ_{SEU})

- **σ_{SEU}s (per category) are calculated from SEU test and analysis.**
- **σ_{SEU}s are calculated per particle linear energy transfer (LET).**
- **Most believe the dominant σ_{SEU}s are per bit (configuration or flip-flops (DFFs)). However, global routes are significant (more than DFFs).**

σ_{SEU}s are measured by bit!

σ_{SEU}s are measured by bit???

$$P(fs)_{system} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

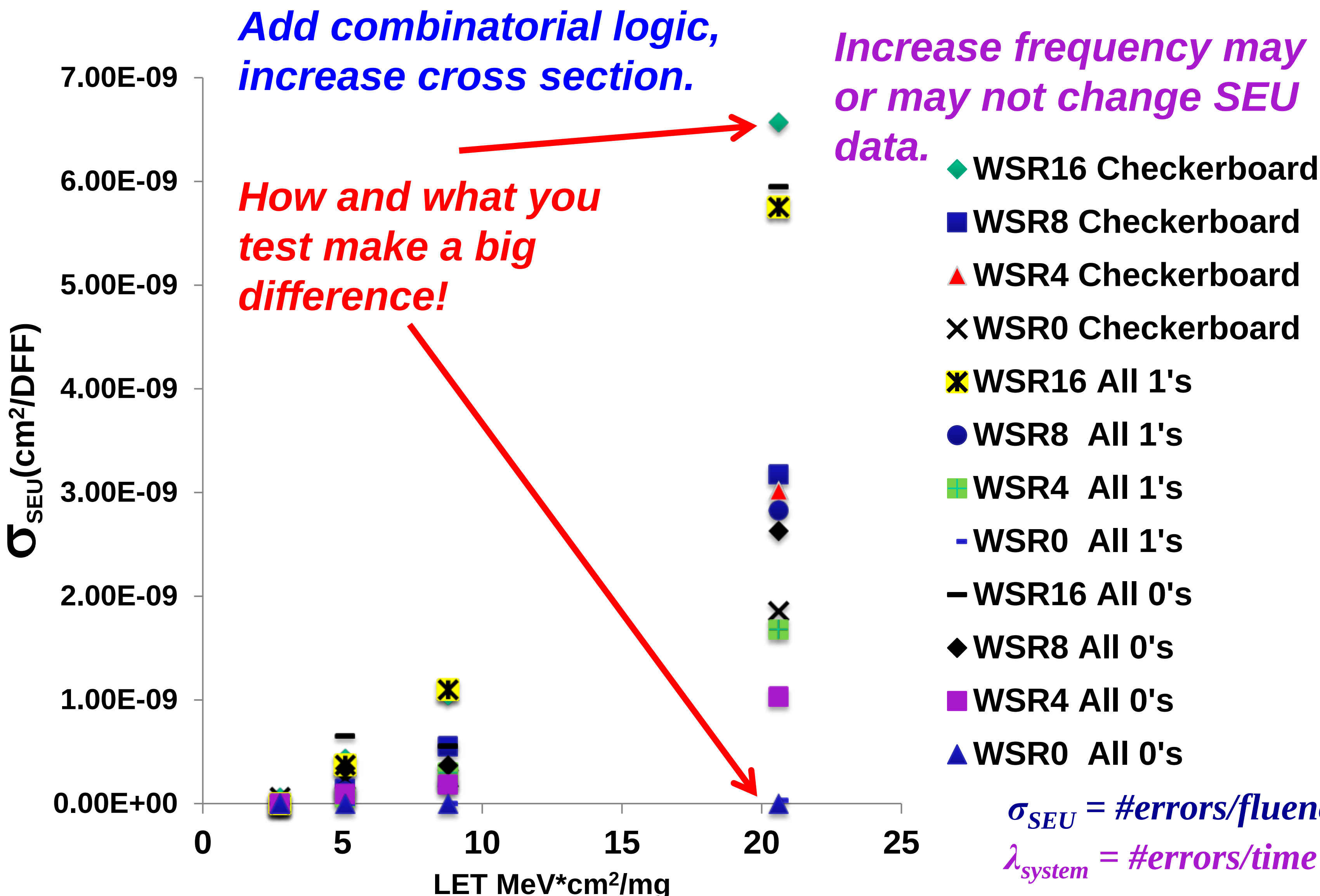
Design σ_{SEU} — *Configuration σ_{SEU}* — *Functional logic σ_{SEU}* — *SEFI σ_{SEU}*

For a system, should σ_{SEU}s be measured by bit????

Sequential and Combinatorial logic (CL) in data path

Global Routes and Hidden Logic

Window Shift Register (WSR) Microsemi σ_{SEU}s: Design and Stimulus Dependencies to SEUs



σ_{SEU} = #errors/fluence

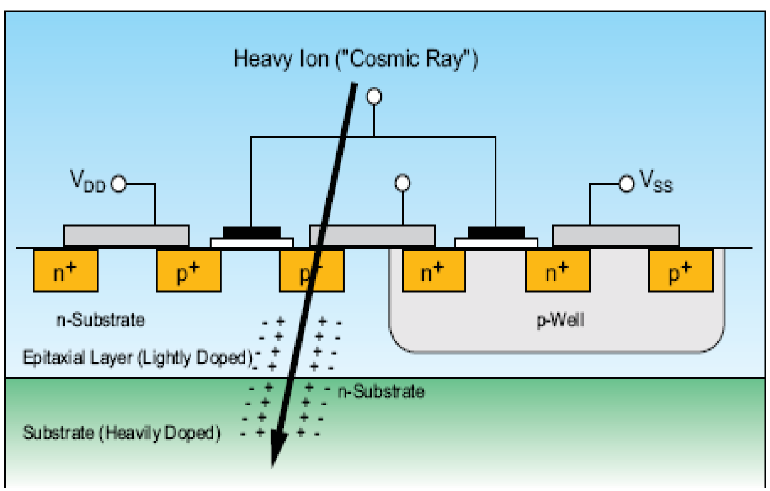
λ_{system} = #errors/time

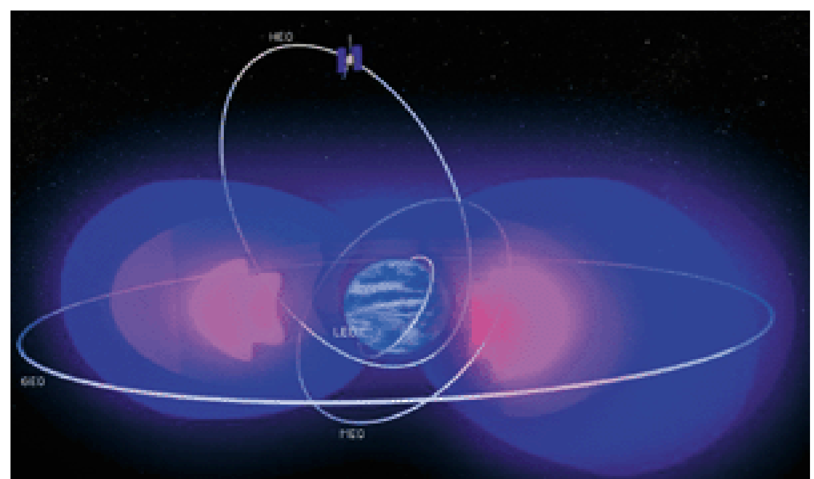
LET: Linear energy transfer

Background (2)

Conventional Conversion of SEU Cross-Sections To Error Rates for Complex Systems Next Step

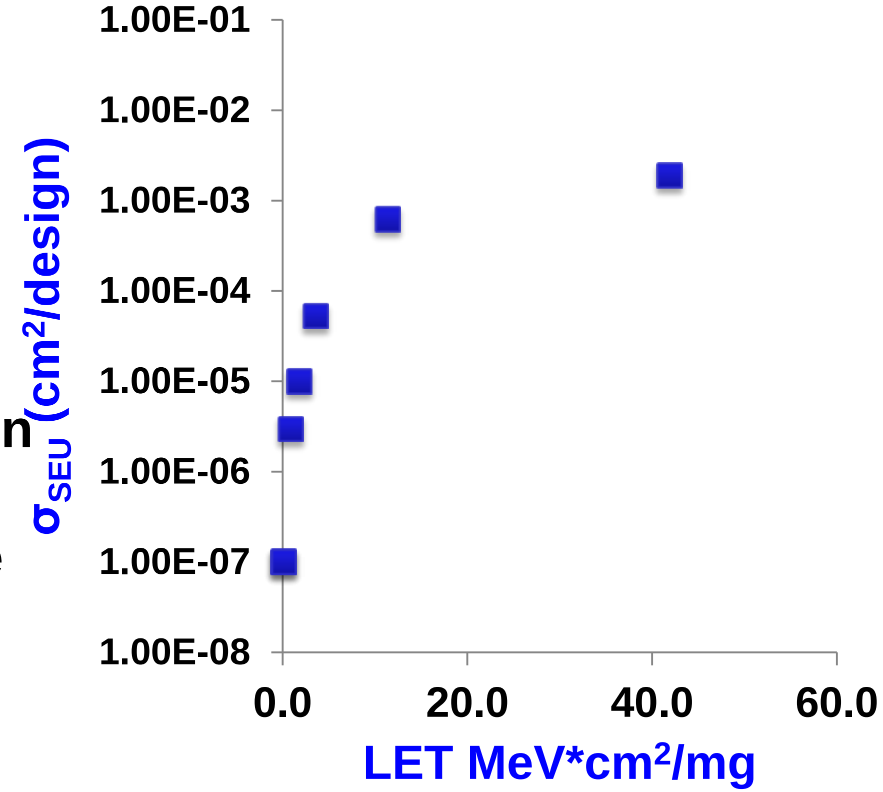
- **Bottom-Up approach (transistor level):**
  - Given σ_{SEU} (per bit) use an error rate calculator (such as CRÈME96) to obtain an error rate per bit (λ_{bit}).
  - Multiply λ_{bit} by the number of used memory bits (*#UsedBits*) in the target design to attain a system error rate (λ_{system}). Configuration and DFFs.
- **Top-Down approach (system level):**
  - Given σ_{SEU} (per system) use an error rate calculator (such as CRÈME96) to obtain an error rate per bit (λ_{system}).





Technical Problems with Current Methods of Error Rate Calculation

- For submission to CRÈME96, σ_{SEU} data (in Log-linear form) are fitted to a Weibull curve.
  - During the curve fitting process, a large amount of error can be introduced.
  - Consequently, it is possible for resultant error rates (for the same design) to vary by decades.
- Because of the error rate calculation process, σ_{SEU} data are blended together and it is nearly impossible to hone in on the problem spots. This can become important for mitigation insertion.



Technical Problems with Bottom-Up Analysis Method

- **Multiplying each bit within a design by λ_{bit} is not an efficient method of system error rate prediction.**
  - **Works well with memory structures… but…complex systems do not operate or respond like memories.**
  - **If an SEU affects a bit, and the bit is either inactive, disabled, or masked, a system malfunction might not occur.**
    - **Using the same multiplication factor across DFFs will produce extreme over-estimates.**

$$\lambda_{system} < \lambda_{bit} \times \#UsedBits$$

Let's Not Reinvent The Wheel… A Proven Solution Can Be Found in Classical Reliability System-Level Analysis

Mapping Classical Reliability Models from The Time Domain To The Fluence Domain

- The exponential model that relates reliability to MTTF assumes that during useful-lifetime:
  - Failures are independent.
  - Error rate is constant.
  - MTTF = 1/λ.

$R(t)=e^{-t/MTTF}$ or $R(t)=e^{-\lambda t}$

Weibull slope = 1… exponential.

Parallel between time and fluence.

- For a given LET (across fluence):
  - SEUs are independent.
  - σ_{SEU} is constant.
  - MFTF = $1/\sigma_{SEU}$.

σ_{SEU} = #errors/fluence

λ_{system} = #errors/time

- Hence, mapping from the time domain to the fluence domain (per LET) is straight forward:
  - $t \Leftrightarrow \Phi$
  - MTTF $\Leftrightarrow$ MFTF
  - $\lambda \Leftrightarrow \sigma_{SEU}$

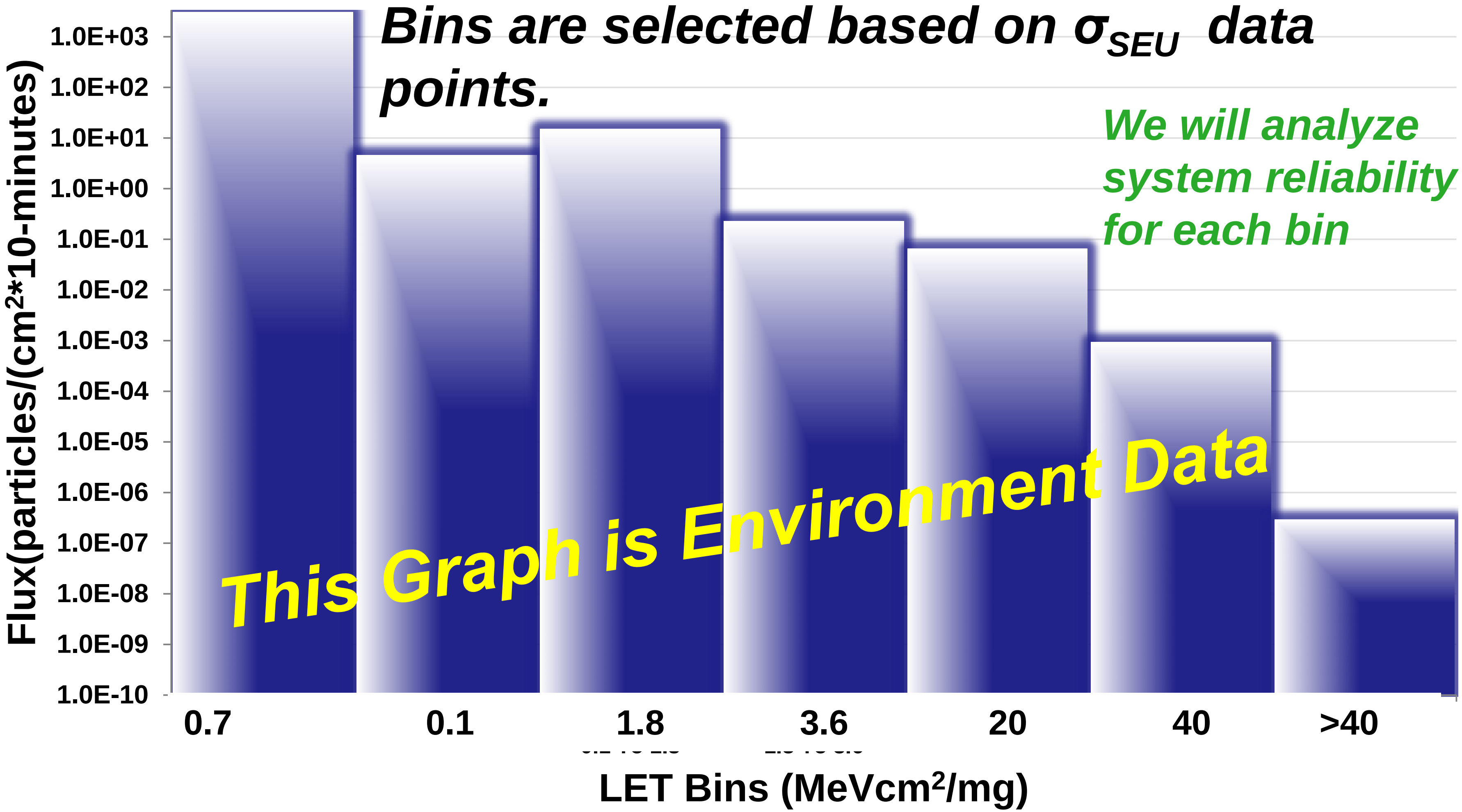
$$R(t)=e^{-t/MTTF} \Leftrightarrow R(\Phi)=e^{-\Phi/MFTF}$$

Example of Proposed Methodology Application

- **Mission requirements:**
  - **Selection shall be made between a Xilinx V5QV (relatively expensive device) or a Xilinx V5 with embedded PowerPC (relatively cheap device).**
  - **FPGA operation shall have reliability of 3-nines (99.9%) within a 10 minute window at Geosynchronous Equatorial Orbit (GEO).**
- **Proposed methodology:**
  - **Create a histogram of particle flux versus LET for a 10-minute window of time for your target environment.**
  - **Calculate MFTF per LET (obtain SEU data).**
  - **Graph R(Φ) for a variety of LET values and their associated MFTFs.** $R(\Phi)=e^{-\Phi/MFTF}$
  - **For selected ranges of LETs, use an upper bound of particle flux (number of particles/cm^2•10-minutes), to determine if the system will meet the mission's reliability requirements.**

Environment Data: Flux versus LET Histogram for A 10-minute Window

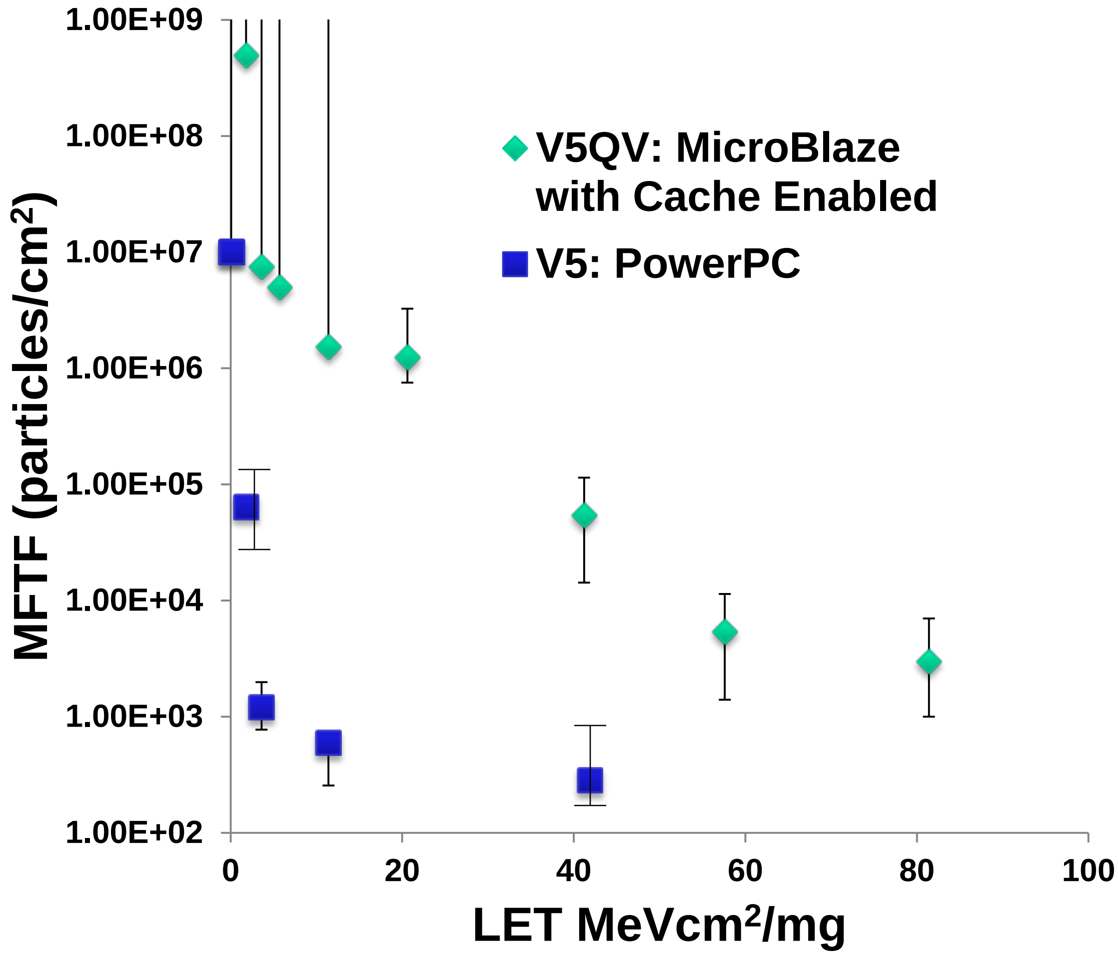
Geosynchronous Equatorial Orbit (GEO) 100-mils shielding



MFTF versus LET for the Xilinx V5 Embedded PowerPC Core and the Xilinx V5QV MicroBlaze Soft Processor Core

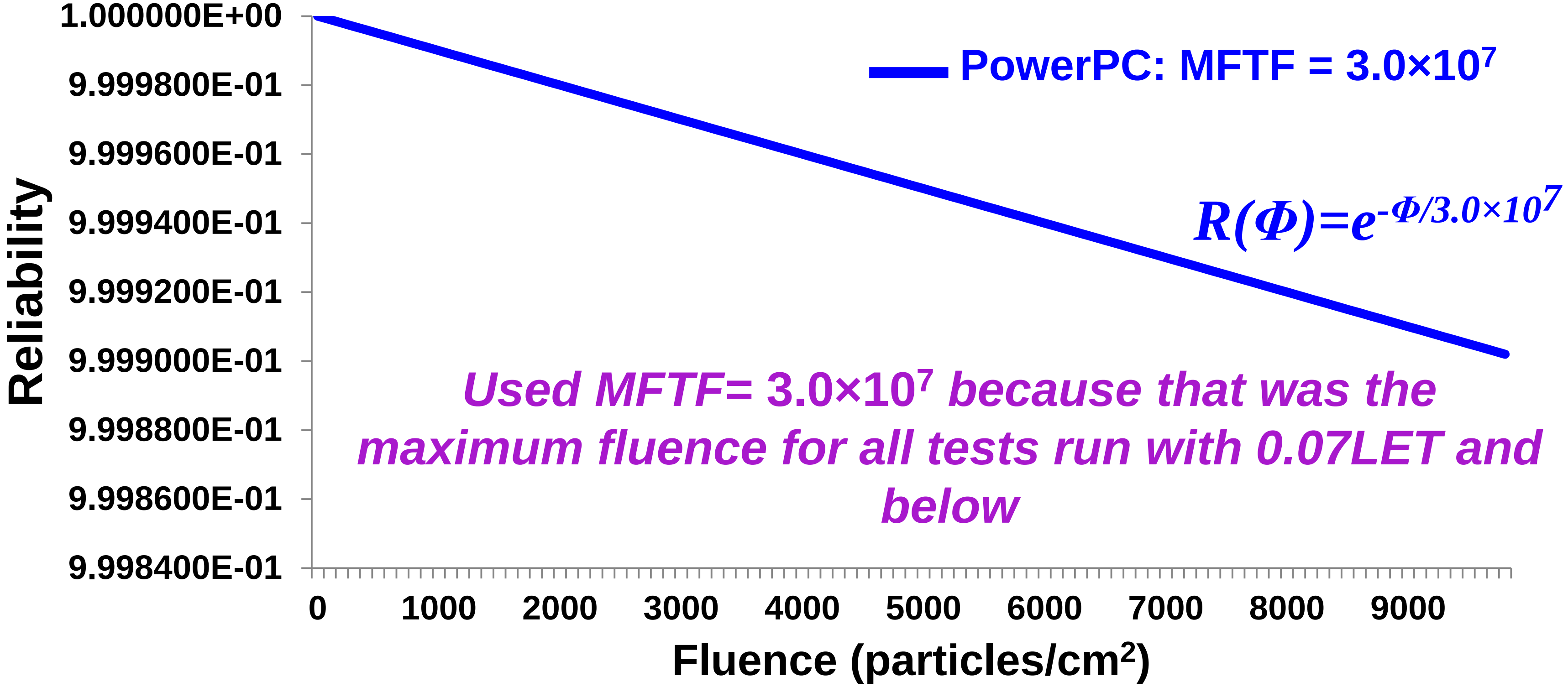
- **V5QV:** no system errors were observed below LET=1.8 MeV•cm²/mg. Total fluence > 5.0×10^8 particles/cm².
- **PowerPC:**
  - No system errors were observed below LET=0.07MeV•cm²/mg with total fluence = $3. \times 10^7$ particles/cm².
  - Hence, at 0.07, we will assume an upper-bound MFTF = 3.0×10^7 particles/cm².
  - More tests would increase the MFTF for this bin.

MFTF = $1/\sigma_{SEU}$



Reliability across Fluence up to LET=0.07MeV•cm^2/mg

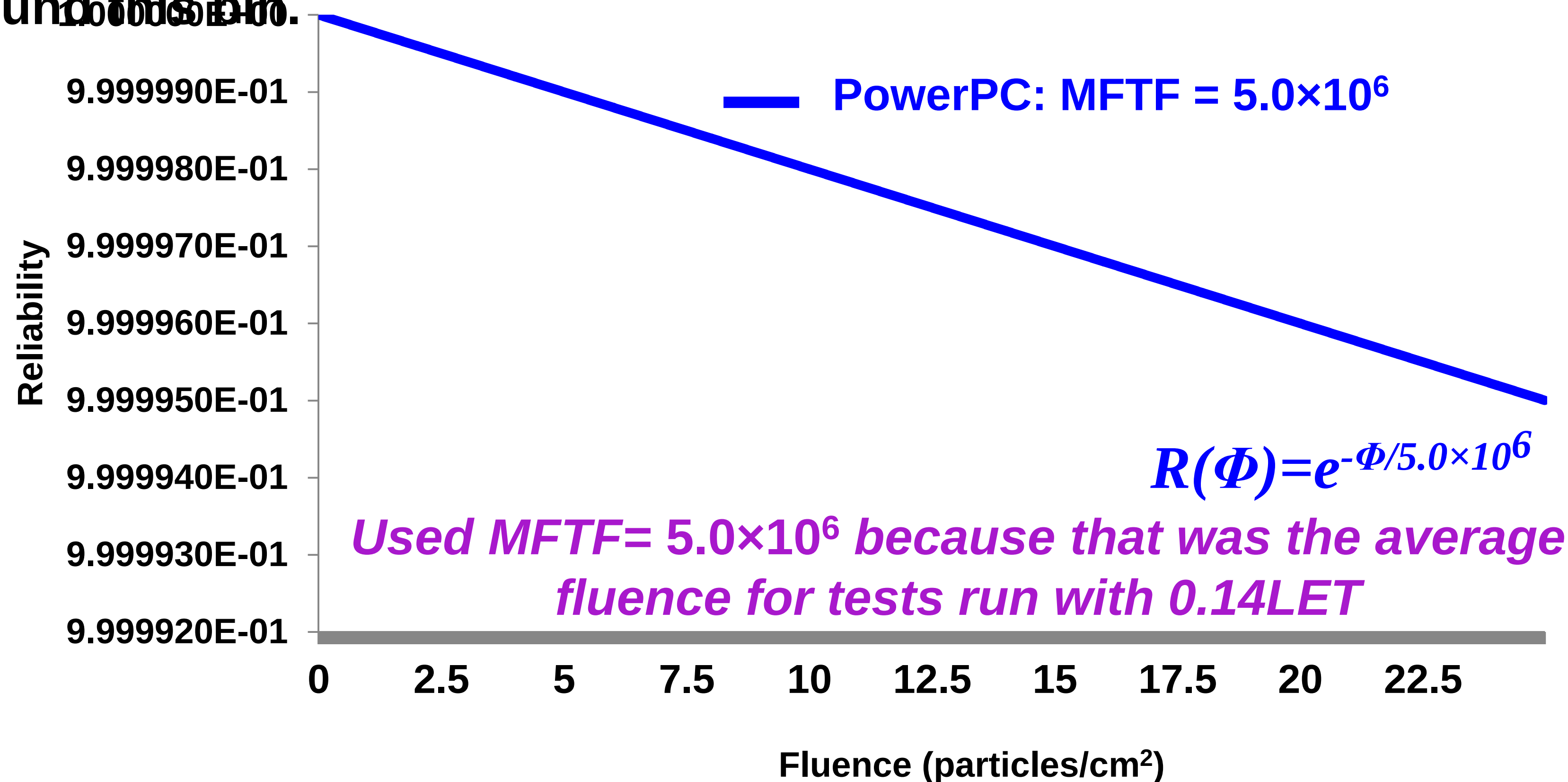
Binned GEO Environment data show approximately 3000 particles/(cm^2•10-minutes), in the range of 0.0MeV•cm^2/mg to 0.07MeV•cm^2/mg. We are using MFTF for 0.07MeV•cm^2/mg to upper bound this bin.



Reliability at 3000 particles/(cm^2•10-minutes) > 99.99% for the PowerPC design implementation. "9's" could be increased with more tests.

Reliability across Fluence up to LET=0.14MeV•cm²/mg

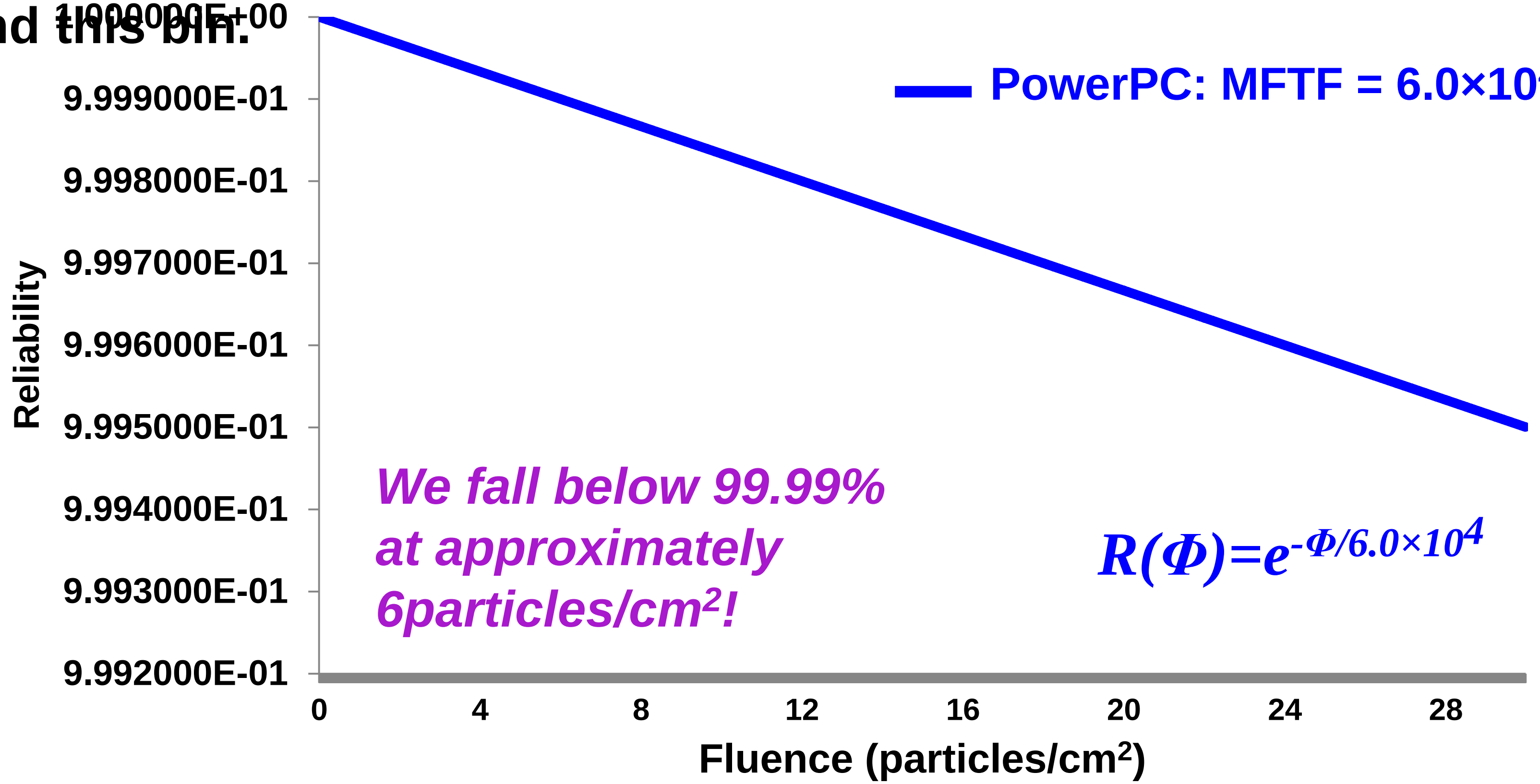
Binned GEO Environment data show approximately 11 particles/(cm²•10-minutes), in the range of 0.07MeV•cm²/mg to 0.14MeV•cm²/mg. We are using MFTF for 0.14MeV•cm²/mg to upper bound this bin.



Reliability at 5 particles/(cm²•10-minutes) > 99.999% for the V5QV PowerPC design implementation.

Reliability across Fluence up to LET=1.8 MeV•cm²/mg

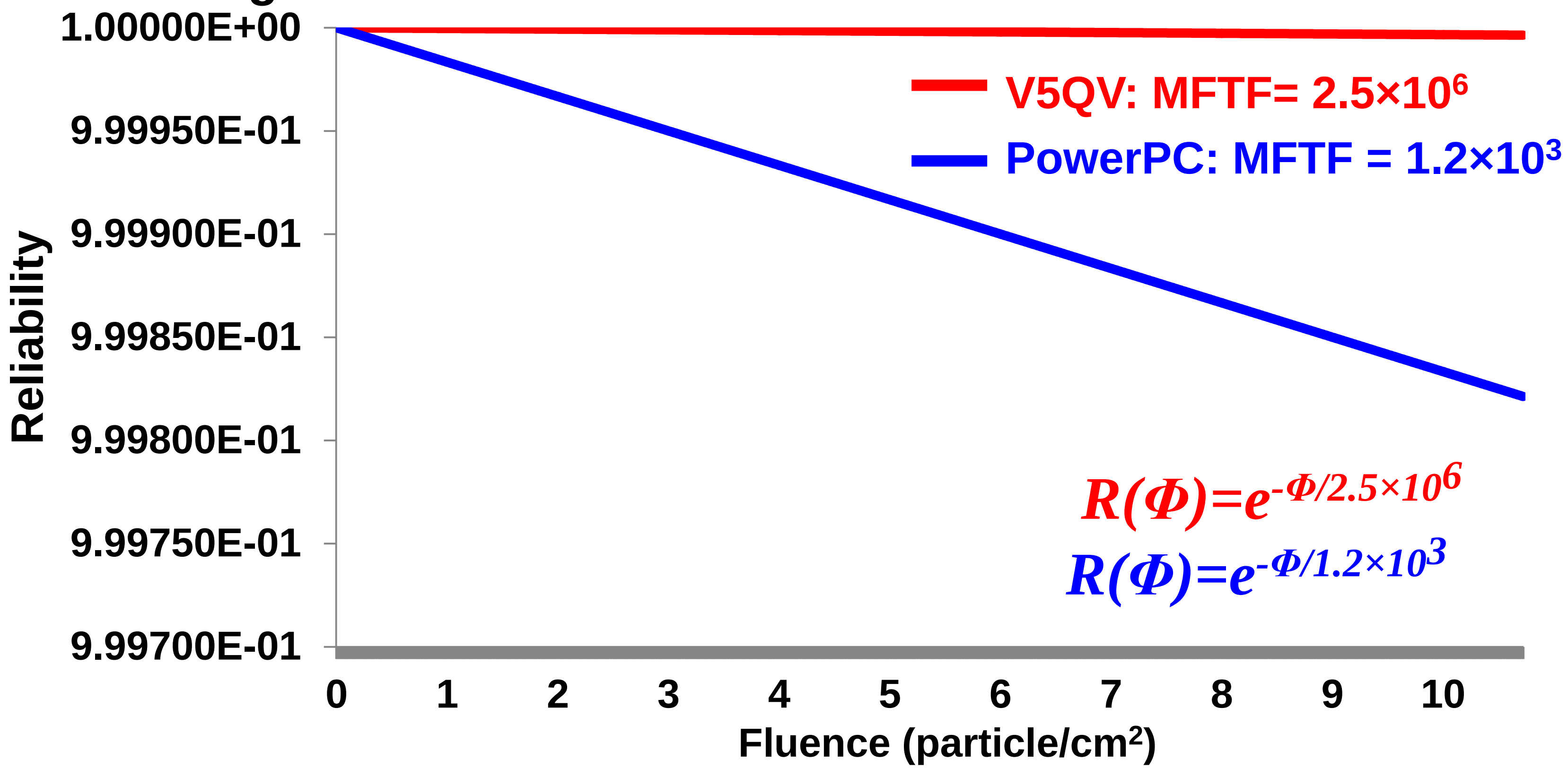
Binned GEO Environment data show approximately 9 particles/(cm²•10-minutes), in the range of 0.14MeV•cm²/mg to 1.8MeV•cm²/mg. We are using MFTF for 1.8MeV•cm²/mg to upper bound this bin.



Reliability at 9 particles/(cm²•10-minutes) > 99.9% for the PowerPC design implementation. This is the most susceptible bin for the system.

Reliability across Fluence up to LET=3.6MeV•cm²/mg

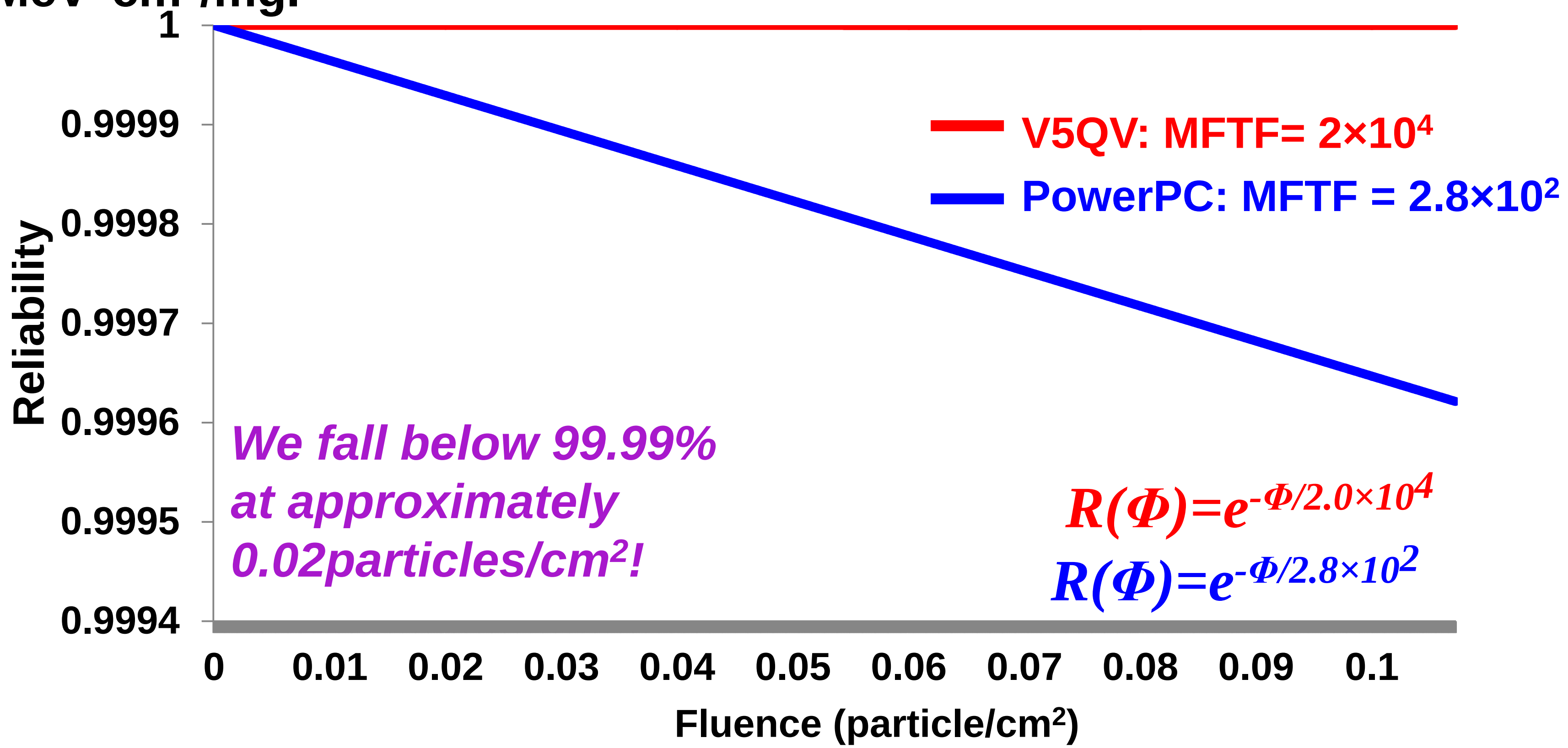
Binned GEO Environment data show approximately 0.23 particles/(cm²•10-minutes), in the range of 1.8MeV•cm²/mg to 3.6MeV•cm²/mg.



Within this LET range, reliability at 0.23 particles/(cm²•10-minutes) > 99.999% for both design implementations.

Reliability across Fluence at LET=40MeVcm²/mg

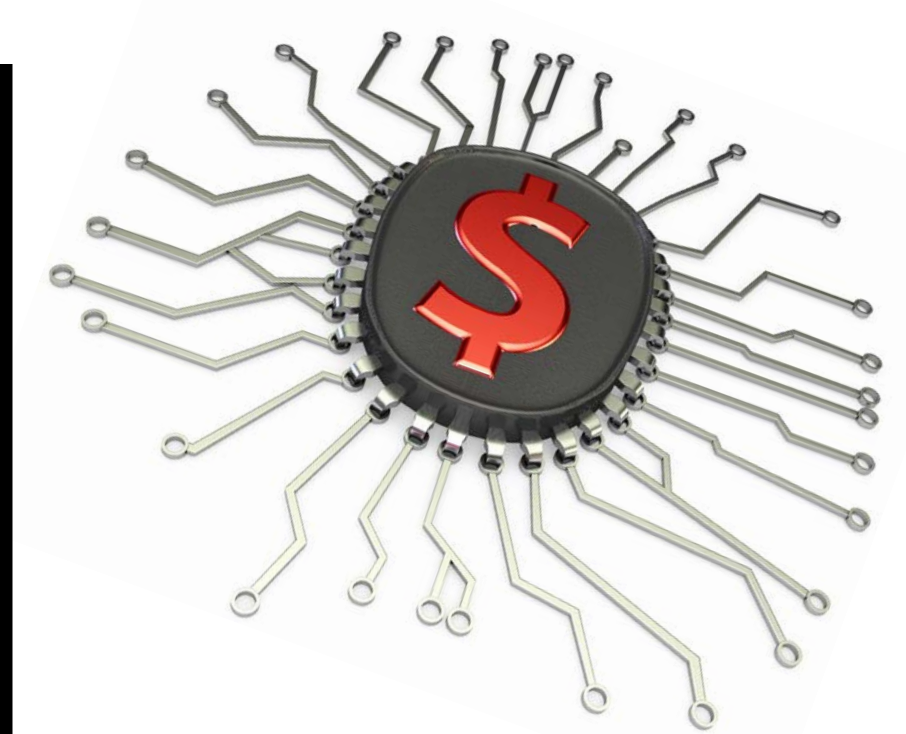
Binned GEO environment data show approximately 0.07 particles/(cm²•10-minutes), in the range of 3.6MeV•cm²/mg to 40.0MeV•cm²/mg.



Within this LET range, reliability at 0.07 particles/(cm²•10-minutes) > 99.9% for both design implementations. We can refine by analyzing smaller bins.

Example Conclusion

- **Using the proposed methodology, the commercial Xilinx V5 device will meet project requirements.**
- **In this case, the project is able to save money by selecting the significantly cheaper FPGA device and gain performance because of the embedded PowerPC.**



Conclusions

- This study transforms proven classical reliability models into the SEU particle fluence domain. The intent is to better characterize SEU responses for complex systems.
- The method for reliability-model application is as follows:
  - SEU data are obtained as MFTF.
  - Reliability curves (in the fluence domain) are calculated using MFTF; and are analyzed with a piecemeal approach.
  - Environment data are then used to determine particle flux exposure within required windows of mission operation.
- The proposed method does not rely on data-fitting and hence removes a significant source of error.
- The proposed method provides information for highly SEU-susceptible scenarios; hence enables a better choice of mitigation strategy.
- This is preliminary work. There is more to come regarding environment data transformation.

This methodology expresses SEU behavior and response in terms that missions understand via classical reliability metrics.

Acknowledgements

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