Radiation Hardened FPGA Technology for Space Applications

Leonard Rockett¹, Dinu Patel¹, Steven Danziger¹, J.J. Wang², and Brian Cronquist²

¹BAE Systems, 9300 Wellington Road, Manassas, VA 20110-4122
²Actel Corporation, 2061 Stierlin Court, Mountain View, CA 94043-4655

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RHAX250-S effort supported by the Defense Threat Reduction Agency
RH FPGA Programs at BAE SYSTEMS

- RH FPGA Roadmap
- RH FPGA Technologies
  - ONO
  - M2M
- RH FPGA Program Status Review
  - Restart RH1020/RH1280 FPGA Program
  - RHAX FPGA Demonstration and Qualification Program
- Summary and Outlook
Radiation Hardened FPGA Roadmap

Past

- Heritage: Actel ONO RH1280 and RH1020
- Anti-fuse technology, non-volatile
- 0.8µm RH CMOS, 5V Supply
- In production since 1996, over 25,000 shipped

Present

- M2M Anti-fuse Technology:
  - 250K-gate (RHAX250-S)
  - RH15 CMOS, 1.5V Core / 3.3V I/O
  - Flight Orders in 2008

Future

- ≥3M-gate, re-programmable, non-volatile
- Radiation Hardened, high speed
- RH15 CMOS, 1.5V Core / 3.3V I/O
- Projected qualification starts in 2009

BAE Supporting RHFPGA Needs for RHOC requirements

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ONO Antifuse Based FPGA’s

Antifuse integrated in FEOL

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ONO technology originally installed and qualified to support RH1020 and RH1280 FPGA’s and a 256K PROM [1994-96]

• Flight qualified production (with build-out inventory) [1996-2002]

• Production shutdown during foundry modernization [2002-2005]
  ➢ Process line re-tooled to support 250 and 150 nm technology nodes on 150mm wafers

• ONO technology now reinstalled in modernized foundry to restart FPGA & PROM product to supply continued demand [2007- ]
  ➢ Used same design data ⇒ same form, fit, and function as product built previously
Rad Hard FPGA RH1280B Technology Features

Features
- Guaranteed Total Dose Radiation Capability
- Low Single Event Upset Susceptibility
- High Dose Rate Survivability
-Latch-Up Immunity Guaranteed
- QML Qualified Devices
- Commercial Devices Available for Prototyping and Pre-Production Requirements
- Gate Capacities of 2,000 and 8,000 Gate Array Gates
- More Design Flexibility than Custom ASICs
- Significantly Greater Densities than Discrete Logic Devices
- Replaces up to 200 TTL Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to Two High-Speed, Low-Skew Clock Networks
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Non-Volatile, User Programmable Devices
- Fabricated in 0.8 μ Epitaxial Bulk CMOS Process
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer

Product Family Profile

<table>
<thead>
<tr>
<th>Device</th>
<th>RH1020</th>
<th>RH1280</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System Gates</td>
<td>3,000</td>
<td>12,000</td>
</tr>
<tr>
<td>Gate Array Equivalent Gates</td>
<td>7,000</td>
<td>8,000</td>
</tr>
<tr>
<td>PLD Equivalent Gates</td>
<td>6,000</td>
<td>20,000</td>
</tr>
<tr>
<td>TTL Equivalent Packages</td>
<td>50</td>
<td>200</td>
</tr>
<tr>
<td>20-Pin PAL Equivalent Packages</td>
<td>20</td>
<td>80</td>
</tr>
<tr>
<td>Logic Modules</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S-Modules</td>
<td>547</td>
<td>1,232</td>
</tr>
<tr>
<td>C-Modules</td>
<td>0</td>
<td>624</td>
</tr>
<tr>
<td></td>
<td>547</td>
<td>608</td>
</tr>
<tr>
<td>Flip-Flops (Maximum)</td>
<td>273</td>
<td>998</td>
</tr>
<tr>
<td>Routing Resources</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Horizontal Tracks/Channel</td>
<td>22</td>
<td>35</td>
</tr>
<tr>
<td>Vertical Tracks/Channel</td>
<td>13</td>
<td>15</td>
</tr>
<tr>
<td>PLICE Antifuse Elements</td>
<td>186,000</td>
<td>750,000</td>
</tr>
<tr>
<td>User I/Os (Maximum)</td>
<td>69</td>
<td>140</td>
</tr>
<tr>
<td>Packages (by Pin Count)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ceramic Quad Flat Pack (CQFP)</td>
<td>84</td>
<td>172</td>
</tr>
</tbody>
</table>
## Radiation Specifications

### Table 1-2 • Radiation Specifications\(^1,2\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristics</th>
<th>Conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTD</td>
<td>Total Dose</td>
<td></td>
<td>300 k</td>
<td></td>
<td>Rad (Si)</td>
</tr>
<tr>
<td>SEL</td>
<td>Single Event Latch-Up</td>
<td>(-55^\circ C \leq T_{case} \leq 125^\circ C)</td>
<td>0</td>
<td></td>
<td>Fails/Device-Day</td>
</tr>
<tr>
<td>SEU(^1)</td>
<td>Single Event Upset for S-modules</td>
<td>(-55^\circ C \leq T_{case} \leq 125^\circ C)</td>
<td>1E-6</td>
<td></td>
<td>Upsets/Bit-Day</td>
</tr>
<tr>
<td>SEU(^2)</td>
<td>Single Event Upset for C-modules</td>
<td>(-55^\circ C \leq T_{case} \leq 125^\circ C)</td>
<td>1E-7</td>
<td></td>
<td>Upsets/Bit-Day</td>
</tr>
<tr>
<td>SEU(^3)</td>
<td>Single Event Fuse Rupture</td>
<td>(-55^\circ C \leq T_{case} \leq 125^\circ C)</td>
<td>&lt;1</td>
<td></td>
<td>FIT (Fails/Device/1E9 Hrs)</td>
</tr>
<tr>
<td>RNF</td>
<td>Neutron Fluence</td>
<td></td>
<td>&gt;1E+12</td>
<td></td>
<td>N/cm(^2)</td>
</tr>
</tbody>
</table>

### Notes:
1. Measured at room temperature unless otherwise stated.
2. Device electrical characteristics are guaranteed for post-irradiation levels at worst-case conditions.
3. 10% worst-case particle environment, geosynchronous orbit, 0.025" of aluminum shielding. Specification set using the CREME code upset rate calculation method with a 2 μ epi thickness.
• Active current, VIL, VIH, Access time and chip enable time all remain stable through 600 Krd

RH ONO Technology Exceeds 400 Krad TID Requirements
ONO RH FPGA Program Status

- Successfully reinstalled ONO process technology
- Flight-qualified PROM production restarted
- RH1280B prototype hardware successfully built and tested, additional hardware being built in accordance with qualification plan.
  - BAE acquired license from Actel to produce, market and sell RH1280 FPGA’s
  - SEGR completed successfully, TID testing in progress this week
- RH1020 FPGA market assessment underway for potential product reinstallation.

RH1280B FPGA Flight Hardware Orders being taken
For shipments in 2008
Metal to Metal Antifuse Based FPGA’s

Antifuse integrated in BEOL

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Product Installation Approach

Low Risk: Port a proven RT design to a validated RH process.

RH15
Radiation Hardened 150nm CMOS Process Technology on Epi Wafers

FPGA
Unique features
- High Voltage Tx
- Anti-fuse

RH FPGA process derived from the integration of unique features into rad hard 150nm base technology (RH15)

Radiation Hardened 150nm CMOS Technology with features that support RH FPGA’s

Proven RTAX250-S Design

RTAX250-S is a 150nm product built at a commercial foundry on non-epi substrates.

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RHAX250-S Installation and Qualification Roadmap

**Approach**

**Process & Design Rule Development**
- assess RTAX design rules & process details
- define process flow
- create parametric targets
- build & evaluate short loops (Hi-V Tx; antifuse)

**Process Integration / Technology Validation**
- design technology characterization vehicle (TCV)
- build & evaluate full TCV lots

**QML Qualification**
- perform qualification testing on FPGA samples taken from $\geq 3$ lots

**Product Demonstration Prototypes Built & Tested**
- flight qualified product, same form/fit/function

**RHAX250-S**
- RT AX250-S design transferred to BAE

**Port Other RTAX Designs**

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Outline

Introduction

Technology Features

150nm Rad Hard CMOS

Antifuse Programming Element

RHAX250-S Product Description

Radiation Hardness

TID Test Results

SEU/SET Test Results

Summary and Plans

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## RH15 Technology Features

**Rad Hard 150nm CMOS Technology (RH15) Features**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Feature Size</td>
<td>150nm</td>
</tr>
<tr>
<td>Isolation</td>
<td>Shallow Trench Isolation</td>
</tr>
<tr>
<td>Device Options</td>
<td>26 Å / 70 Å</td>
</tr>
<tr>
<td>S/D Engineering</td>
<td>Halo with S/D Extensions</td>
</tr>
<tr>
<td>Supply Voltages</td>
<td>1.5V / 3.3V</td>
</tr>
<tr>
<td>Gate Electrodes</td>
<td>N+ Poly (NFET) / P+ Poly (PFET)</td>
</tr>
<tr>
<td>Metal Levels</td>
<td>7 Levels (Planarized BEOL)</td>
</tr>
<tr>
<td>Poly &amp; Diffusion Silicide</td>
<td>CoSi₂</td>
</tr>
</tbody>
</table>

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RH15 QML Qualification Test Summary

Qualification Test Vehicle:

- Chip Image: 17.6 mm x 17.1 mm
- 6T2R1C cell
- 31 Masking Levels
- Six Metal Levels
- Number of Transistors: 30M
- Number of Resistors: 8M
- Number of Capacitors: 4M
- Number of Contacts: 100 M
- Number of Vias: 70 M
- Wiring Length: ≈1Km

Qual Tests:

- Group A: All Electrical Tests PASSED
- Group C: 1000-Hr / 125°C Life Test PASSED
- Group E: All Radiation Testing PASSED

- Latchup Immune
- Single Event Upset << 1E-10 upsets/bit-day
- Total Ionizing Dose > 2 Mrad(Si)
- Prompt Dose Upset > 1E9 rad(Si)/s
- Prompt Dose Survivability > 1E12 rad(Si)/s

All Qualification Testing Completed Successfully

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RH15 Performance Assessment

High Speed Circuit Testing to measure on-chip gate delay.

Logic Representation of High Speed Signal Paths

Results confirm >1GHz performance both pre- and post-irradiation (2 Mrd(SiO₂))

No change in Iddq with dose.

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## RH15 Reliability Test
### Results Summary

<table>
<thead>
<tr>
<th>Category</th>
<th>Requirement</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>PFET Hot Carrier</td>
<td>10% shift in Vth @ 10-year life</td>
<td>Exceeds requirement</td>
</tr>
<tr>
<td>PFET NBTI</td>
<td>10% shift in Vth or 20% Ids change @10-year life</td>
<td>Exceeds requirement</td>
</tr>
<tr>
<td>NFET Hot Carrier</td>
<td>Less than 20% degradation in Ids @ 10-year life</td>
<td>Exceeds requirement</td>
</tr>
<tr>
<td>Gate Oxide Integrity</td>
<td>Less than 0.01% Cum. failure @ 10-year life</td>
<td>Exceeds requirement</td>
</tr>
<tr>
<td>Mobile Ions</td>
<td>Less than 5E11/cm2</td>
<td>No issue</td>
</tr>
<tr>
<td>Interconnect EM</td>
<td>Less than 0.01% Cum. failure @ 10-year life @ current density of 0.5 mega-A/cm2</td>
<td>Exceeds requirement</td>
</tr>
<tr>
<td>Interconnect Temp-Cycle</td>
<td>Less than 20% change in resistance</td>
<td>No change in resistance</td>
</tr>
<tr>
<td>Stress Migration</td>
<td>Less than 20% change in resistance after high Temp. stress for min stress time of 500 hours</td>
<td>Stress-migration is not an issue</td>
</tr>
<tr>
<td>BEOL Dielectric Integrity</td>
<td>Less than 5e-14uA/um2 leakage current after high Voltage/Temp. stress for 500 hours</td>
<td>No significant change in resistance</td>
</tr>
</tbody>
</table>

Reliability Assessments Exceed Requirements in All Categories
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- Antifuse Programming Element

RHAX250-S Product Description

Radiation Hardness

- TID Test Results
- SEU/SET Test Results

Summary and Plans

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Metal-to-Metal Antifuse

Antifuse Placement: Between to last two metal layers.

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Antifuse Cross-section

- Metal 7
- Top Electrode
- Dielectric
- Bottom Electrode
- W Stud

S4800 5.0kV 1.9mm x200k SE(U) 200nm

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Antifuse Integrity

Breakdown Voltage - 1K Antifuse Array

Breakdown Voltage Distribution Exceeds Requirement (>4.2V)

Leakage Distribution at 3 Volts - 1K Antifuse Array

Leakage Distribution Far Exceeds Requirement (<100µA)

Excellent Fuse Integrity Test Results

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Early Assessment of SEDR on RHAX antifuse arrays (1K)

SEDRA = Single Event Dielectric Rupture

Array Current vs. Fluence

FPGA Lot 2040702 P12W5 ET6 M6P7 [size=1000]

No Rupture Observed Up to Vdd = 4.2V
Demonstrating a large SEDR hardness margin for nominal 1.5V antifuse array

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RHAX250-S Description

chip size : W=9.6mm;  H=9.4mm

Total Transistors :  5.589   million
Total Anti-fuse Elements:  7.743   million
Total Contacts  59.480563   million
Total Via’s  132.824787   million

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## RHAX250-S Product Profile

### Performance

<table>
<thead>
<tr>
<th>Feature</th>
<th>RHAX250-S</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5V Core; 3.3V I/O</td>
<td></td>
</tr>
<tr>
<td>High-Performance Embedded FIFOs</td>
<td></td>
</tr>
<tr>
<td>350+ MHz System Performance</td>
<td></td>
</tr>
<tr>
<td>500+ MHz Internal Performance</td>
<td></td>
</tr>
<tr>
<td>700 Mb/s LVDS Capable I/Os</td>
<td></td>
</tr>
</tbody>
</table>

### Radiation Hardness Targets

<table>
<thead>
<tr>
<th>Target</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>TID</td>
<td>≥ 1Mrad(Si)</td>
</tr>
<tr>
<td>DR. Upset</td>
<td>&gt; 1E9 rad(Si)/sec</td>
</tr>
<tr>
<td>SEL</td>
<td>Immune</td>
</tr>
<tr>
<td>SEU&lt;sub&gt;REGS&lt;/sub&gt;</td>
<td>&lt; 1E-10 errors/bit-day (TMR-hardened)</td>
</tr>
<tr>
<td>SEU&lt;sub&gt;RAM&lt;/sub&gt;</td>
<td>&lt; 1E-10 errors/bit-day (EDAC)</td>
</tr>
</tbody>
</table>

### Modules

<table>
<thead>
<tr>
<th>Type</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register (R-Cells)</td>
<td>1,408</td>
</tr>
<tr>
<td>Combinatorial (C-Cells)</td>
<td>2,816</td>
</tr>
<tr>
<td>Flip-Flops (Maximum)</td>
<td>2,816</td>
</tr>
</tbody>
</table>

### Embedded RAM/FIFO (without EDAC)

<table>
<thead>
<tr>
<th>Type</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core RAM Blocks</td>
<td>12</td>
</tr>
<tr>
<td>Core RAM Bits (K = 1,024)</td>
<td>54 K</td>
</tr>
</tbody>
</table>

### Clocks Segmentable

<table>
<thead>
<tr>
<th>Type</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardwired</td>
<td>4</td>
</tr>
<tr>
<td>Routed</td>
<td>4</td>
</tr>
</tbody>
</table>

### I/O's

<table>
<thead>
<tr>
<th>Type</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O Banks</td>
<td>8</td>
</tr>
<tr>
<td>User I/O's (Maximum)</td>
<td>248</td>
</tr>
<tr>
<td>I/O Registers</td>
<td>744</td>
</tr>
</tbody>
</table>

### Package

<table>
<thead>
<tr>
<th>Type</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCGA/LGA</td>
<td>-</td>
</tr>
<tr>
<td>CQFP</td>
<td>208, 352</td>
</tr>
</tbody>
</table>

---

**RHAX FPGA will have the identical form, fit, and function of its RTAX counterpart.**

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Outline

Introduction

Technology Features

- 150nm Rad Hard CMOS
- Antifuse Programming Element

RHAX250-S Product Description

Radiation Hardness

- TID Test Results
- SEU/SET Test Results

Summary and Plans

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Recently built prototype RHAX250-S FPGA’s have yielded functional hardware, despite anomalous Hi-V Tx junction leakage.

Modules were programmed for total ionizing dose testing.

Circuit elements tested per module:
• 12 blocks of 4Kx1 SRAM (total: 48K)
• 1408-stage DFF register string
• Two 1408-stage logic chains
RHAX250-S TID Test Results

RHAX250-S modules remained fully functional throughout testing to 2Mrd(SiO₂)

TID test results on prototype FPGA’s demonstrate improved hardness. Hardening process adjustments are being implemented to further enhance hardness.
RHAX250-S modules remained fully functional throughout testing to 2Mrd(SiO₂)

These results demonstrate prototype capability

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Introduction
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Hardened Flip-Flop Design

Uses Triple Modular Redundancy (TMR) [hard-wired]

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200-stage DFF chains
Clock: 2 MHz

SEU Test Results on RTAX hardware

SEU Rate: $1.96 \times 10^{-11}$ upsets/bit-day*

* assumed radiation environment: GEO-min and 100 mil Al shielding

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SET Analysis Circuit

DFF chain with interwoven combinational logic

Signal Frequencies: 15MHz, 37.5MHz, 75MHz, and 150MHz

SET Test Results on RTAX hardware

Weibull fits to SET test data

SEU susceptibility increases for increasing signal frequencies and for increasing levels of logic.

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Predicted SEU Rates

vs. logic level & freq.

<table>
<thead>
<tr>
<th>Levels of Intervening Logic</th>
<th>Signal Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>15 MHz</td>
</tr>
<tr>
<td>8-Levels</td>
<td>5.31E-09</td>
</tr>
<tr>
<td>4-Levels</td>
<td>2.01E-09</td>
</tr>
<tr>
<td>0-Levels</td>
<td>6.08E-10</td>
</tr>
</tbody>
</table>

* assumed radiation environment: GEO-min and 100-mil Al shielding

Impact of SET on error rate depends on circuit design and signal frequency.

Further SEU Enhancements projected in Rad Hard Process

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Summary and Plans
Future Work - RHAX

• Build more hardware incorporating identified process enhancements for improved yield and hardness

• Subject functional hardware to full battery of reliability and radiation testing

• QML qualify the RHAX process technology

• Begin full RHAX250-S wafer production to supply Actel

• Port additional Actel RTAX FPGA designs onto rad hard process technology at BAE to extend rad hard offerings.

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Summary

• BAE and Actel are continuing their >12 year collaboration as rad hard FPGA suppliers.

• Next generation rad hard product is being built and tested.

• Total dose test results on RHAX250-S hardware demonstrates improved hardness over RTAX250-S.

• Single-event effects test results demonstrates product design’s high tolerance.

• Electrical, radiation, and reliability testing is on-going.

• Full flight-qualified production to begin by yearend.

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