Advanced ASICs For Obsolete FPGA Replacement

Honeywell

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Presentation Agenda

Honeywell

- Introduction
- Why Replace An FPGA?

- FPGA Replacement Capability
  - ASICs Platforms
  - ASIC Design Flow
  - SOI CMOS Trusted Foundry
  - Packaging

- Multi-Sourced Design IP
  - SERDES High Speed I/O
  - Logic
  - SRAMs
  - Processors

- Summary

Proven Source For FPGA Replacements

Introduction

- Honeywell Is An Experienced, Fully Qualified Supplier Of Microelectronics

  - High Complexity Obsolete IC Emulations
    - FPGA Replacements
    - SRAMs And Processors
    - Multiple Sources For Design IP

  - Leadership Digital Products For Space Market
    - First FPGA Replacement Completed In 1998
    - First To Market With Rad Hard FPGA In 2001
    - First 150nm Based 16M SRAM Products
    - First 150nm Based Digital ASICs
    - First 150nm Based SERDES I/O
    - First 150nm Based Structured ASIC

  - Charter Member, DoD Trusted Foundry Certification Program

  - QML And ISO90001 Quality Management Systems
  - Experienced Management Team

Proven Source For FPGA Replacements

Capability For High Complexity Emulations Today

Honeywell

DoD Capability Today	DoD Future Requirement	Honeywell Capability Today
1. Advanced Digital Devices <2500 gates, <48 Pin, 1um Technology	**VLSI Devices including complex standard functions, 500K density near term, 30M gate density in future.**	500K to 12M gate density ASICs with embedded complex functions like SERDES, roadmap to 30M density.
2. Microprocessors MIL-STD-1750A	**Common 4-32 bit processors and associated chipsets.**	1750A, RHPPC And custom 32 bit processors.
3. Memory 5V memory up to 4K in size	**Programmable, EP, EEP, static, dynamic, flash – 256K very near term, 16M out years.**	Standard and embedded SRAM up to 16M density.
4. Programmable Logic	**Various types of both programmable and field programmable devices.**	Meet future requirements with mask and field programmable devices.
5. Hybrid Microelectronics	**Integrate components from SSI complexity to as complex as defined in 1-4 above.**	Meet future requirements.
6. Linear/Analog Electronics Simple amplifiers, comparators and 20V drivers.	Integrate low end op amps thru high performance A/D and D/A.	Meet future requirements.
7. Circuit Card Assemblies	FFF emulation of CCA's and sub assemblies.	Meet future requirements.

Source: June 2007 BAA From DLA

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Why Replace Your FPGAs?

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- Original Source of Supply Discontinues Product
  - Process Migration
  - Not Enough Volume
  - Or Both

- You Have To Redesign Your Electronics To
  - Reduce Power
  - Reduce Cost
  - Reduce Weight
  - Improve Performance
  - Achieve Flight Level Radiation Hardness

- Meet Emerging DoD Requirement That System Critical ASICs Be Made By Trusted Foundry To Keep IP Within USA

Proven Source For FPGA Replacements

ASICS For FPGA Replacement

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Platform	HX2000	HX3000	HX5000	Structured ASIC
Process	0.8 um	0.35 um	150 nm	150 nm
# Base Arrays	5	4	6	1
Max # I/O	372	388	1330	956
Useable Gates	40-390K	235-1,200K	2-14M**	1M+**
Design IP	Honeywell, Customer	Honeywell, Customer	Honeywell SERDES, Synopsys	Honeywell, Synopsys
Self Test	JTAG	JTAG	JTAG, MBIST	JTAG, MBIST
Design Flow	Cadence	Cadence	Synopsys	Synopsys
Qualification	QML	QML	QML	QML
Foundry	Trusted	Trusted	Trusted	Trusted

* (nW/gate/MHz) ** maximum number depends on mix of logic and memory

Proven Source For FPGA Replacements

Synopsys Based ASIC Design Process

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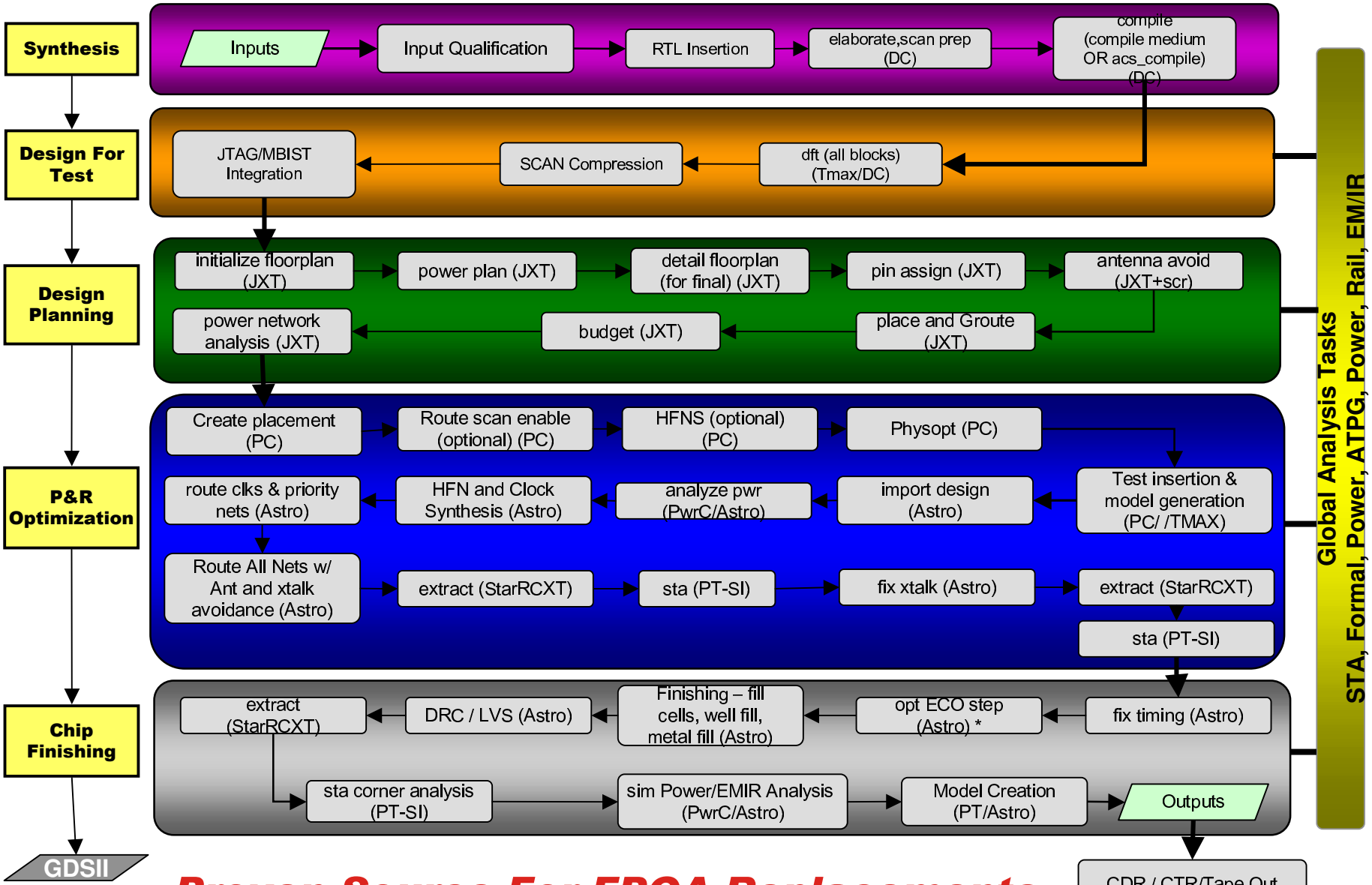

Proven Source For FPGA Replacements

SOI CMOS Wafer Processes

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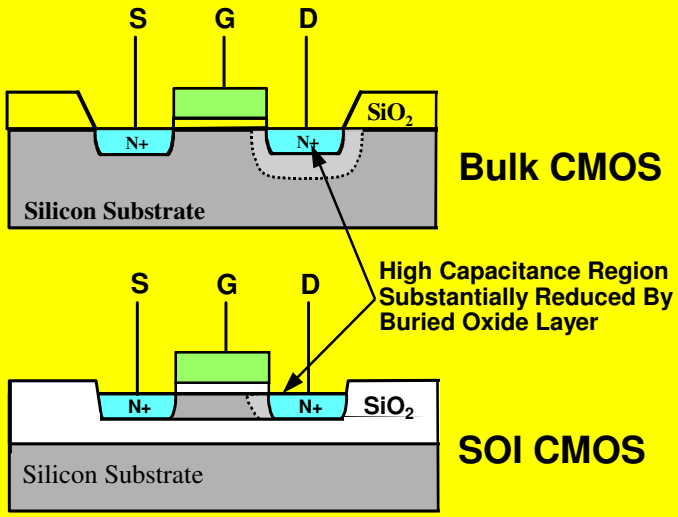
	SOI-4	SOI-5	S150
Production*	Now Thru 2015+	Now Thru 2015+	Now Thru 2015+
Interconnect	4 Level CuAl	4 Level CuAl	6 Level CuAl
Gate Length	.7 um	.35 um	150 nm
Wafer Size	150 mm	150 mm	200 mm
Devices	NCh, PCh, DMOS	NCh, PCh	NCh, PCh
Vdd (V)	3.3-20	3.3	3.3/25/1.8
Hardened By	Process	Process	Process
Process Options	CrSi, RF Discrete	CrSi, EEPROM	MIMCAP, Bump/FC

Transistor Cross Sections



Buried SiO_2 Layer Provides

- Radiation Hardness
- Ultra High Reliability
- 30% To 40% Faster Circuits At Same Node
- 30% To 40% Lower Power At Same Node
- Excellent Isolation For Mixed Signal ASICs
- Continuous High Temp Operation At 225°C

* Assured Source Of Supply To Major DoD Programs

Proven Source For FPGA Replacements

Advanced ASIC Packaging Options

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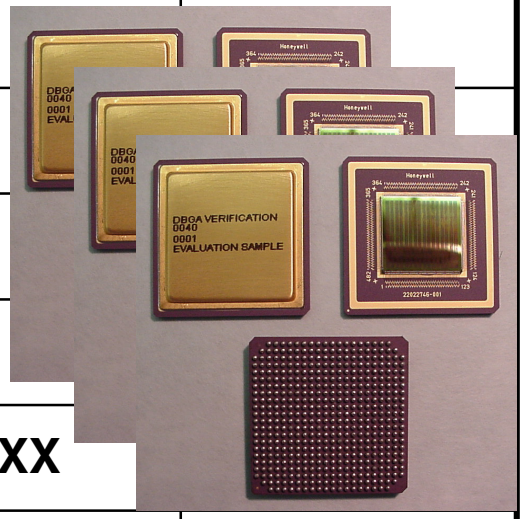
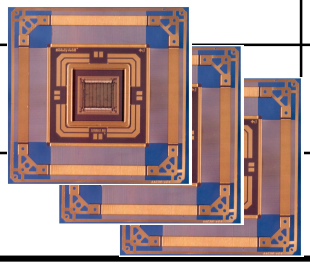
ASIC	HX2000	HX3000	HX5000	Structured ASIC
Package				
DIP	XXX			
CQFP	XXX			
PGA	XXX			
BGA	XXX	XXX	XXX	
LGA	XXX	XXX	XXX	XXX
DBGA		XXX	XXX	XXX
CGA			XXX	XXX
Flip Chip				XXX





Proven Source For FPGA Replacements

Structured ASIC Created For FPGA Replacements

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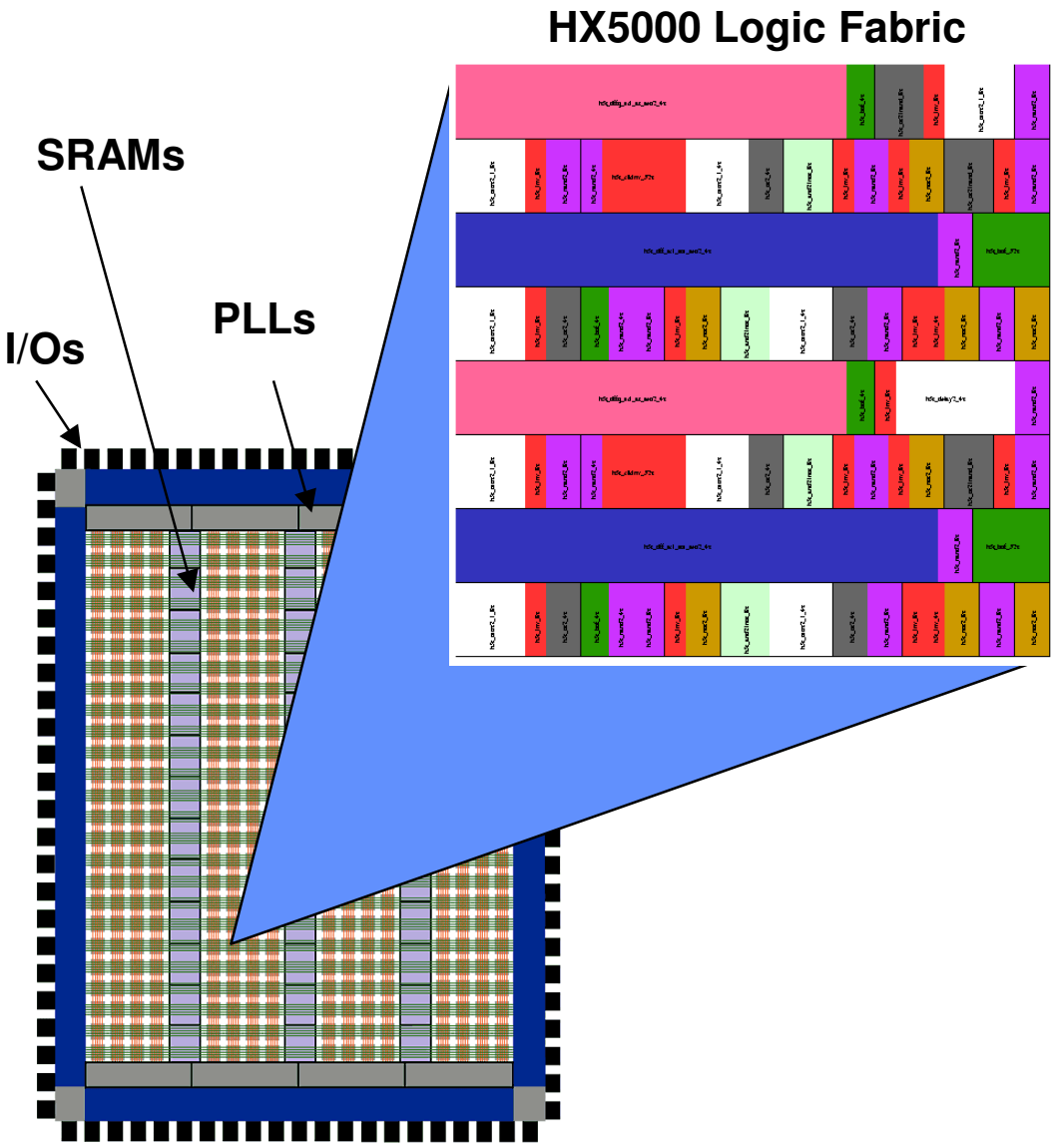

- **Benefits**
  - Lower Power
  - Rad Hard By Process
  - Automated Design Migration
  - ~25% Of HX5 NRE Cost
  - ~30% Of HX5 NRE Cycle Time
- **Built On Proven Capability**
  - 150nm SOI CMOS
  - HX5000 Standard Cells
  - HX5000 SRAM and PLLs
  - User Selectable And FPGA Compatible I/O Types
  - FFF Packaging
- **Design Flow Uses**
  - Synopsys Front End
  - Lightspeed Back End

Working Silicon In Hand!

Structured ASIC Product Comparison

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	FPGAs		Honeywell S-ASIC	HX5000	
	Actel AX2000	Xilinx 2V8000	Structured ASIC	Honeywell HX511	Honeywell HX514
System Gates	2,000,000	8,000,000			
Typical Gates	1,060,000	500,000-2M	1,044,000	11,000,000	14,000,000
Total RAM Bits	294,912	3,000,000	2,520,000		
RAM Blocks	64	160	140		
PLLs	8	12	8		
Max User I/Os	684	1,108	956	872	1000

- **S-ASIC Typical Gates**
  - SRAM Area Equivalent To ~8 Million Gates (By Nand2_4x Standard)
  - 1 Million Usable Gates Are As Seen By FPGA Designer
  - ASIC Designer Would Consider Gate Count Much Higher Than 1million Gates Shown
  - 90% Place And Route Utilization Demonstrated
- **S-ASIC Available For Early Adopters In 2008**

Replaces Actel And Xilinx FPGAs

Advanced ASICs Can Replace These FPGAs

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FPGA	Migrates To	Available	K Gates	Cycle Time
Actel 1020	HX2000	Now	1	12 Weeks
Actel 1280	HX2000	Now	1	12 Weeks
Actel RTX2000	Structured ASIC	2008	1000	12-16 Weeks
Actel MX Series	HX2000	Now	1	Call For Quote
Actel eX Series	HX2000/3000	Now	12	Call For Quote
Actel SX Series	HX3000	Now	108	Call For Quote
Altera Apex 20k	HX3000	Now	500	Call For Quote
Altera Flex Series	HX2000	Now	250	Call For Quote
Altera Stratix	HX5000	Now	3000	Call For Quote
Atmel AT6002	HXFPGA6010*	Now	6	12 Weeks
Atmel AT6003	HXFPGA6010*	Now	9	12 Weeks
Atmel AT6005	HXFPGA6010*	Now	15	12 Weeks
Atmel AT6010	HXFPGA6010*	Now	30	12 Weeks
AT40 Series	HX2000	Now	50	Call For Quote
Xilinx Spartan II	HX2000	Now	250	Call For Quote
Xilinx Vertex 2	Structured ASIC	2008	1000	12-16 Weeks
Xilinx Vertex 4	HX5000	Now	3000	24-32 Weeks

Can Replace 13 FPGA Families Today

* FPGA Available Today

Proven Capability For FPGA And CCA Replacements

Honeywell

Clearwater, Florida Capability

For Circuit Card Replacements

- Leverage Program Success As Supplier To TRIDENT, MMIII & Space Shuttle
- Complete In-House Design, Test And Integration Capability
- NASA NHB5300/IPCJ-STD-001 Compliant
- DoD Supplier For Over 50 Years

Plymouth, Minnesota Capability

For FPGA Replacements

- Leverage $300M Of DoD Investment In Microelectronics Technology For DoD
- Complete On Shore, In-House Design, Wafer Fab, Assembly & Test Capability
- QML And ISO9001 Certified
- Processes Maintained Thru 2015
- DoD Supplier For Over 25 Years

Accreditation of Trust

Microelectronics Trusted Source
CATEGORY I

By these presents the undersigned expresses the confidence of the Department of Defense Trusted Access Program Office in the ability of the organization known as

Honeywell International
Plymouth, Minnesota

to deliver trusted foundry microelectronic goods and services to end users within the United States Government that correspond to Trusted Category I which meets Mission Assurance Category I as defined by Instruction 8500.2 of the Department of Defense Directives, effective this date by the authorities granted by USD/AT&L memo of 27 January 2004.

0005	13 November 2006	13 November 2007	Gerald W. Etzold, Chief
Site Accreditation Number	Effective Date	Renewal Date	Director, DoD Trusted Access Program Office

Complete On-Shore And In-House Capability To Design And Manufacture Both FPGA And CCA Replacements

www.honeywell.com/microelectronics

A History Of Success Stories

Honeywell

Customer	Product	Success
Restricted	Convert Actel 1080 And 1280 FPGAs	100% First Pass Success On 40+ Designs
Backpack Radio OEM	4K X 1 SRAM	Shipping Production
Satellite OEM	Convert Actel 1080 And 1280 FPGAs	100% First Pass And 1280 FPGAs
Engine Control OEM	MIL-STD-1750A Micro-processor	Shipping Production To Multiple Customers
Oilfield Services OEM	80C51 Emulation	Shipping Production
Radar System OEM	ECL ASIC Emulation	First Pass Success On First Two Designs
Satellite OEM	Atmel AT6010 Emulation	Shipping Production

750,000 Units Shipped Since 2003

Multi-Sourced Design IP

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Type Of IP	Sources	Type	Available
High Speed I/O	Honeywell	SERDES Fiber Channel	Now
		SERDES GB Ethernet	Now
		SERDES PCI Express	Now
	Synopsys*	PCI Express	Now
Digital Logic	Honeywell	In ASIC Library	Now
	Synopsys	DesignWare Library	Now
Memory	Honeywell	Embedded SRAM	Now
		Embedded NVSRAM	Ask
		Embedded EEPROM	Ask
		Custom SRAM	Now
Processor	Honeywell	HX1750A	Now
		RHPPC	Now
	IPeXtreme	68000 Series	Now
	Synopsys*	80C51, 6811	Now

Multi-Sourced Design IP Supports FPGA Replacements

* Part Of Synopsys DesignWare Library

SERDES Applications

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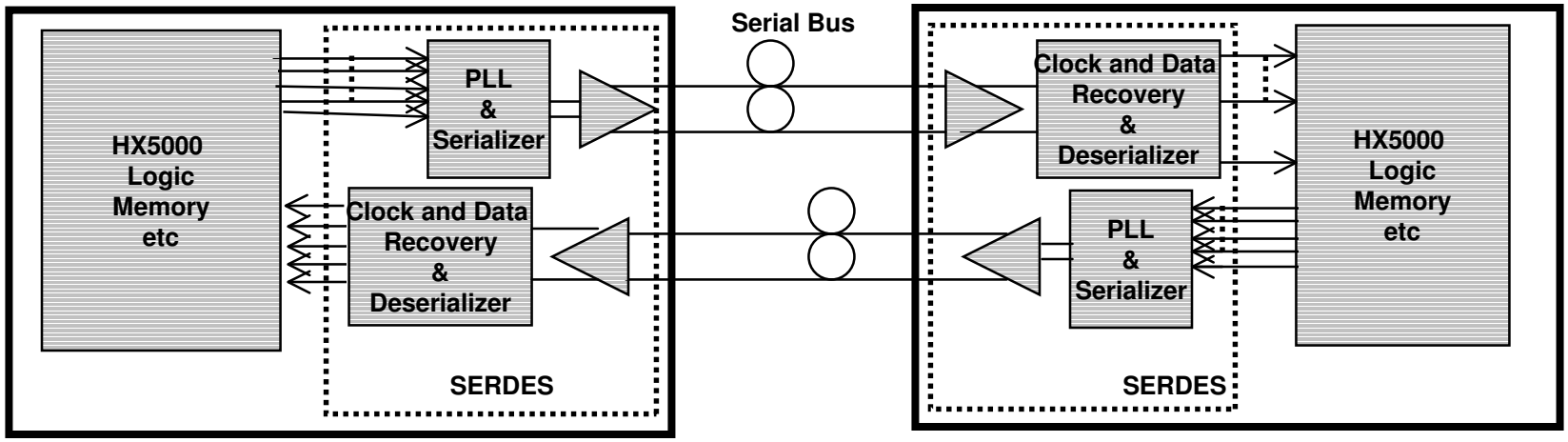

What Is A SERDES?

- A SERDES Coverts High-speed Serial Data To Lower-speed Parallel Clock & Data To Enable Designers To Use Integration Of Deep Submicron ASICs
- A SERDES Increases The Amount Of Data That Can Be Reliably Sent Between Two Chips
- A SERDES Offers Significantly Lower Power And Pin Counts Than Traditional Parallel Interfaces

When Is It Used?

- Systems With High Bandwidth Requirements
- Systems That Need To Send Information Over Long Distances
- To Ease The Timing Constraints Associated With Large I/O Interfaces

Proven Design IP For FPGA Replacements

SERDES Communication I/O

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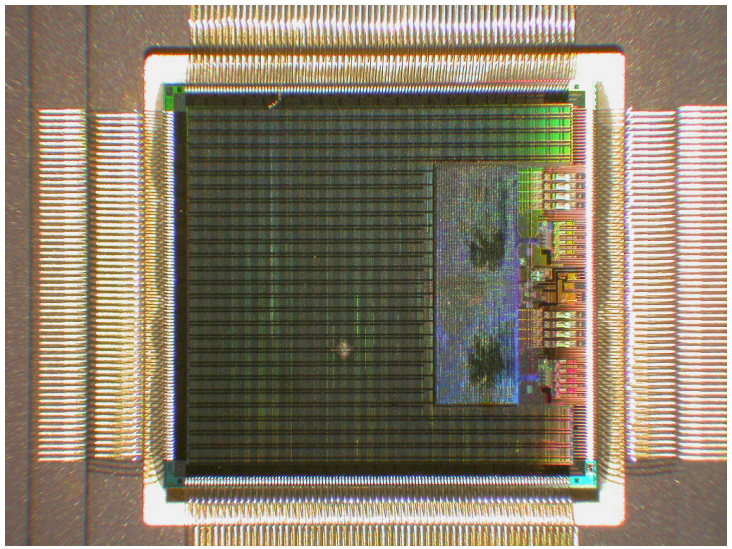

- **RADHARD/Tolerant SERDES Integrated Into HX5000 ASIC And Validated In Silicon**

- **Supports Multiple Standards**
  - **10GE (4x3.125 Gbps XAUI)**
  - **10G Fibre Channel (4x3.1875 Gbps XAUI)**
  - **1G FC / 2G FC / 4G FC**

- **Low Power**
  - **125 mW Per Channel @ 1.8V**
  - **4–20 Channels With A Single VCO**

- **High Signal Integrity**
  - **Superior Distance**
    - FR4 backplane > 1m @ 4.25 Gbps
    - Infiniband cable > 15m @ 4.25 Gbps
  - **Margin Increases At Lower Data Rates**
  - **Low jitter**
    - TX DJ = 0.20 UI, TX TJ = 0.33 UI
    - RX DJ = 0.33 UI, RX TJ = 0.62 UI
  - **BER Of 1e-14**

- **Individual Channel Programmability**
  - **Selectable Data Rate**
  - **Selectable Signal Shaping For Optimization Of Individual Channels**

- **Built In Self Test**
  - **At Speed Testing Of High-speed Circuitry For Diagnostics And At-Speed Verification On An ATE Platform**

Proven Design IP For FPGA Replacements

High Speed SERDES Macrocell

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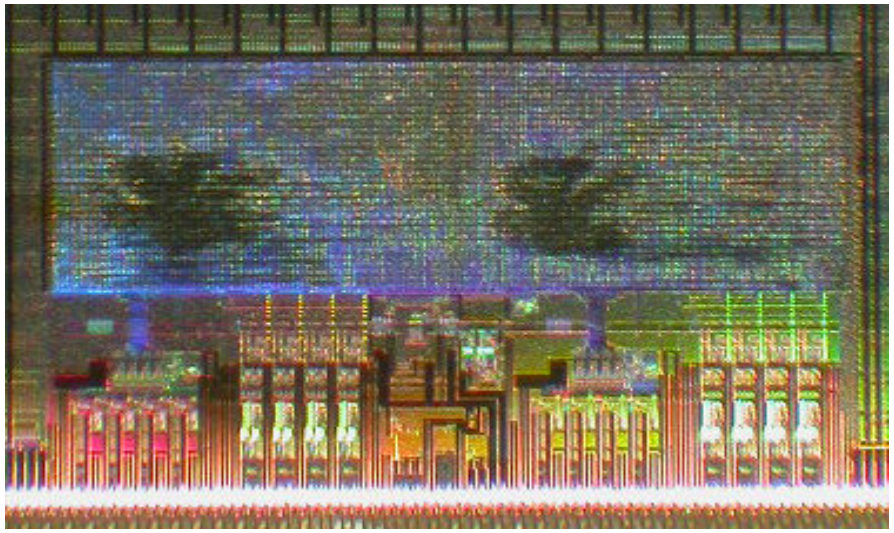


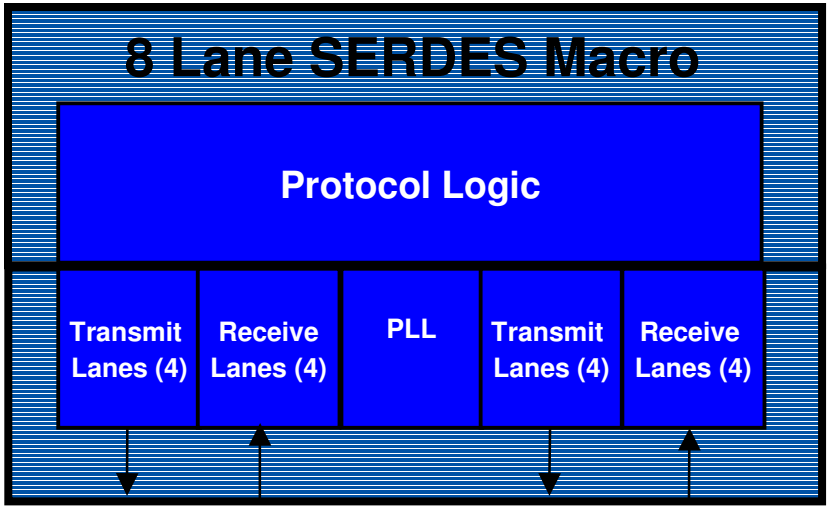
High Speed SERDES Macrocell On HX5000 ASIC

Protocol Support

- 1 to 4.25Gbps
- Fibre Channel
  - 1G/2G/4G and 10G (XAUI)
- Gigabit Ethernet
  - 1G and 10G (XAUI)
- PCI-Express & Rapid IO
  - Bypass mode

HX5000 Library Offerings

- 8 Lane Macro (Q2, 2008)
- 4 Lane Macro (Q3, 2008)
- Customized Upon Request



High Speed SERDES Macrocell Block Diagram

Directly Applicable To FPGA Replacements

SERDES Works!

Honeywell

- **Product Meets All Published Datasheet Specifications**
  - Datasheet Available NOW
  - TID And SEE Radiation Reports Available Under NDA
- **Demonstrated Bit Error Ratio That Exceeds Specs**
  - Lower Than 10^{-17} At 2.125Gbps
  - Lower Than 10^{-14} At 4.25Gbps
- **Demonstrated Ability To Drive 100 Feet Of Cable At 3.125 Gbps**
- **Less Than 200mw Power Per Lane At 3.125 Gbps**
- **Multiple BIST Loopback Modes Available**
- **Multiple Configuration Interfaces Available**

Ready For Integration Into FPGA Replacements

SERDES Is User Programmable

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- Transmitter
  - On-chip 100-ohm Resistor Termination
  - Supports User Programmable 4-level Pre-emphasis
  - Supports User Programmable Output Amplitude
  - Can Be Powered Down On A lane-by-lane Basis
- Receiver
  - Supports Individual User Programmable 4-level Equalization
  - Supports Programmable Loss Of Signal Detection
  - Can Be Powered Down On A lane-by-lane Basis
- Integrated PLL
  - Only Needs A Single External Resistor
  - Internal Bandgap Voltage Reference
  - Supports Up To 16 Lanes With A Single PLL

Flexible Enough To Emulate SERDES From Popular FPGAs

Quad Redundant SERDES Standard Product

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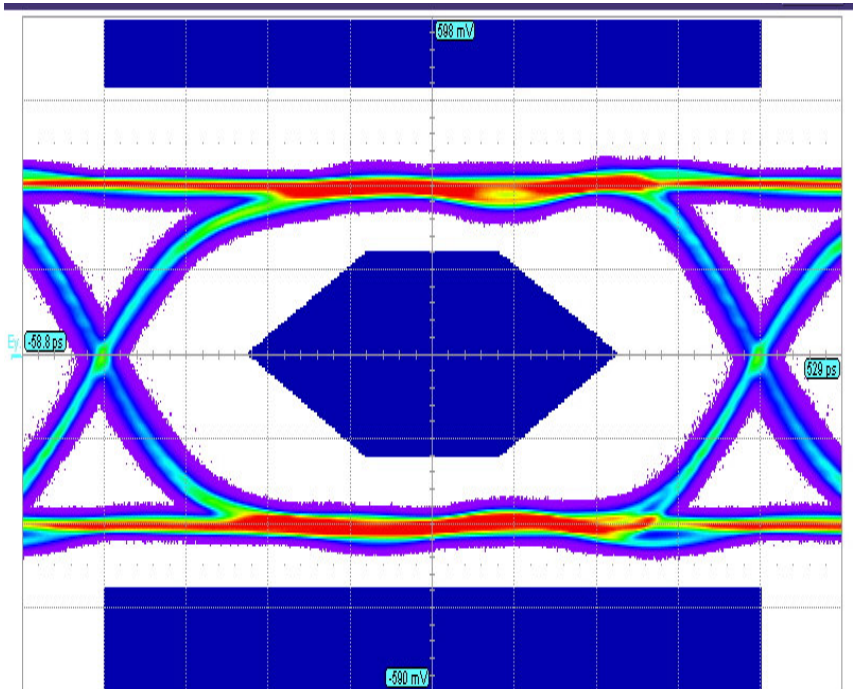


Product Information

- Sampling NOW, Production Q3 2008
- Quad SERDES With Redundant Serial IO
- Parallel Interface Using SSTL2 IO
- Programmable Input & Output Buffers
- 448-ball BGA Package

Protocol Support

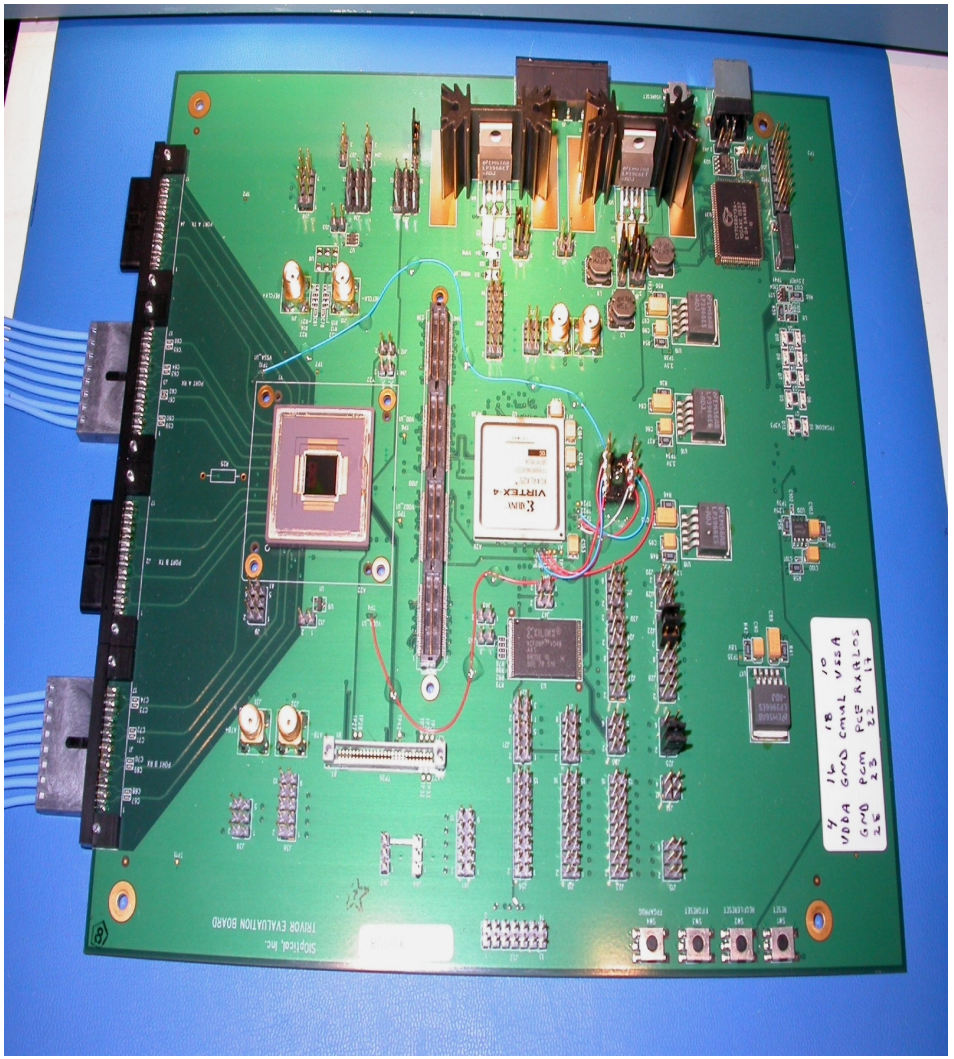
- 1Gbps To 4.25Gbps For General Backplane Applications
- 1G/2G/4G & 10G (XAUI) Fibre Channel
- 1G And 10G (XAUI) Ethernet
- Multiple Bypass Modes

Works With Existing FPGAs Or Replacements

SERDES Evaluation Kit

Honeywell

- **Accepting Orders NOW For January 2008 Delivery!**
- **Enables Evaluating Both The SERDES Macro And The Quad Redundant Standard Product**
- **The Evaluation Kit Contains**
  - SERDES Evaluation Board
  - Cables And Software
  - Documentation
  - Video Of Honeywell Demo
- **Mates To Your Existing Backplane For At-speed Characterization**



Enables Easy SERDES Evaluation

HX5000 Logic Design IP Summary

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- Starting Point For Cell List Is HX3000
  - 233 Combinational, 4 Clock, 94 Sequential, And 1 PLL (332 Total)
  - Most Cell Names Stay The Same
  - Most Functions And Pin Names Stay The Same
- New Cells Based On Review Of Foundry Benchmarks
  - Added 98 Sequential
  - Added 94 Combinational
  - Added 30 Clock
  - Added 57 SET Hardened Combinational
  - Added 2 'Other'
- New LSSD And Dlatchnq
  - Dlatchnq_seu4_4x,16x, Dlatchnq_ar_seu4_4x,16x
  - Lssd_seu4_4x,16x
  - Lssd_ar_seu4_4x,16x
- Cell Count (613 Total)
  - Combinational = 327
  - Sequential = 184
  - Clock = 34
  - SET Hard Combinational = 57
  - Other = 3

Over 600 Unique Cells* And Growing

* Not Counting Synopsys DesignWare

HX5000 SRAM Design IP Summary

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- **Single Port (63 Options)**

h5s256	x8	12	16	20	24	28	32	36	40
h5s512	x8	12	16	20	24	28	32	36	40
h5s1024	x8	12	16	20	24	28	32	36	40
h5s2048	x8	12	16	20	24	28	32	36	40
h5s4096	x8	12	16	20	24	28	32	36	40
h5s8192	x8	12	16	20	24	28	32	36	40
h5s16384	x8	12	16	20	24	28	32	36	40

- **Dual Port (63 Options)**

h5d256	x8	12	16	20	24	28	32	36	40
h5d512	x8	12	16	20	24	28	32	36	40
h5d1024	x8	12	16	20	24	28	32	36	40
h5d2048	x8	12	16	20	24	28	32	36	40
h5d4096	x8	12	16	20	24	28	32	36	40
h5d8192	x8	12	16	20	24	28	32	36	40
h5d16384	x8	12	16	20	24	28	32	36	40

Over 120 Unique Drop-In SRAMs* And Growing

*** Not Counting Synopsys DesignWare**

HX5000 IO Design IP Summary

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Description	Voltage	Max Frequency	Features
CMOS	1.8, 2.5, 3.3	200 MHz	Cold Sparing
PCI	3.3	33MHz/66MHz	
LVDS	2.5, 3.3	600 Mb/s	Cold Sparing
SERDES	1.8	4.25 Gb/s/lane 10gb/s XAUI	8 Channel Macro
SSTL	2.5	250 MHz	C-I, C-II, I, O And Bi-pad
LVPECL	1.8	1.2 GHz Clock 1.2 GB/s Data	AC Coupled Input Only

Supports All I/O Types From Popular FPGAs

RHPPC Processor Product

Honeywell

Processor Replacement

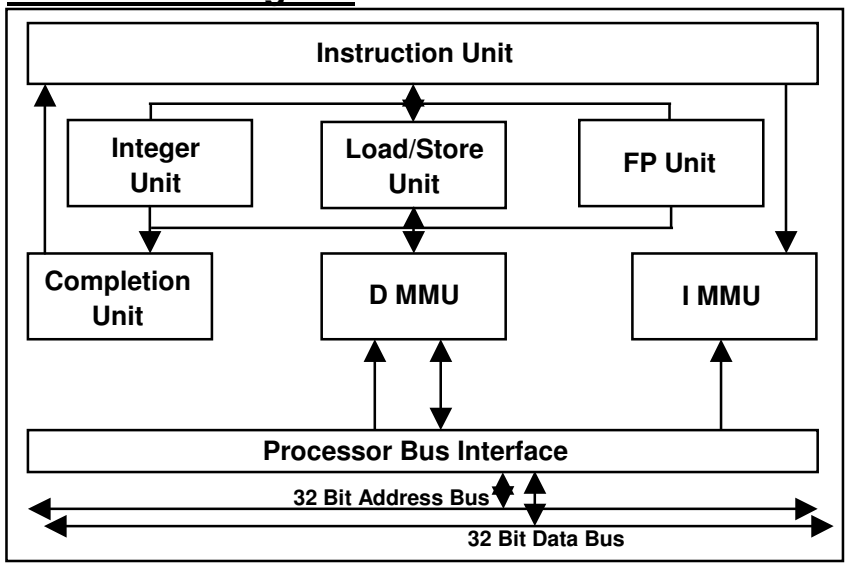
Features

- Proven Rad Hard, High Performance Super Scalar Processor
  - 3.3V Supply
  - SMD Drawing 5962-07A01
  - Core frequency up to 100 MHz
  - Five Independent Execution Units And Two Register Files
- Programmable Integrated PLL
- QFP, BGA And CGA Packaging

Radiation Performance

- Total Dose	300K Rad (Si)
- Dose Rate Upset	4X10e11 rad (Si)/sec
- Dose Rate Survive	1e12 rad (Si)/sec
- SEU	< 8.5X10e-6 Upsets Per Device-Day, GEO AP8 Min
- Neutron Fluence	1e14 N/cm squared

Functional Diagram



Design Support

- Honeywell Provides System Design Support
  - Basic Level Included In Unit Pricing
  - Advanced Level Quoted Upon Request
- 100% Code Compatible With Freescale Semiconductor Version
- Available COTS PowerPC Development Tools Can Be Used

Available For New Designs Today

www.honeywell.com/microelectronics

HXRFP6010 FPGA Product

FPGA Replacement

Honeywell

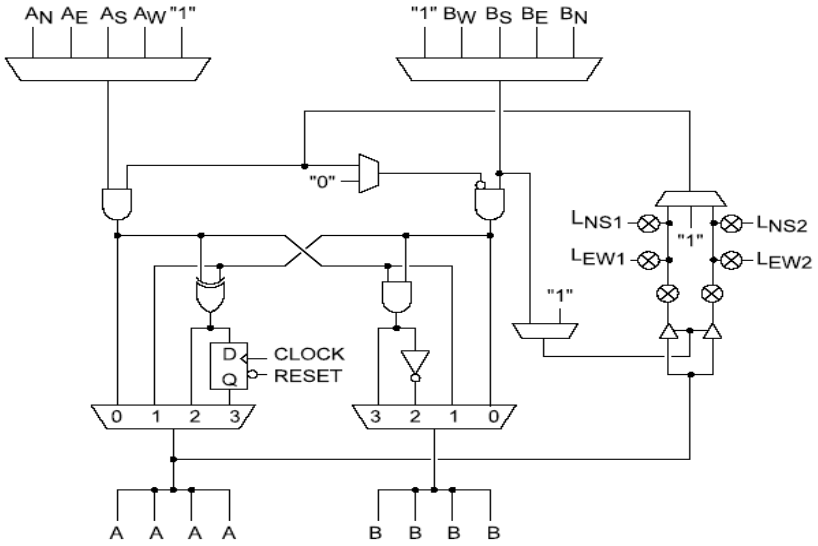
Features

- SRAM Based FPGA Enables Flying The Devices Your Design Is Prototyped In
- Integrates Up To 30,000 Gates
- 0.35um SOI CMOS Process
- CMOS Compatible I/O
- 3.3V Supply
- 240 Pin CQFP Package
- Production Level Product

Radiation Performance

- Total Dose	> 300K Rad (Si)
- SEU	< 5X10e-15 Upsets/Bit-Day
- Dose Rate Upset	> 1X10e11 Rad (Si)/sec
- Dose Rate Surv.	> 1X10e12 Rad (Si)/sec
- Latch Up	None

Functional Diagram – Each Of 640 Core Cells



Design Support

- Honeywell Provides Design Support
  - Chip Level Free Of Charge
  - Systems Level Quoted Upon Request
- 100% Compatible With Atmel FPGA Integrated Development System. Users Can Download These Tools From

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2747

Production Product Today

www.honeywell.com/microelectronics

Summary

Honeywell

- Honeywell Is An Experienced, Fully Qualified Supplier Of Microelectronics

  - High Complexity Obsolete IC Emulations
    - FPGA Replacements
    - SRAMs And Processors
    - Multiple Sources For Design IP

  - Leadership Digital Products For Space Market
    - First FPGA Replacement Completed In 1998
    - First To Market With Rad Hard FPGA In 2001
    - First 150nm Based 16M SRAM Products
    - First 150nm Based Digital ASICs
    - First 150nm Based SERDES I/O
    - First 150nm Based Structured ASIC

  - Charter Member, DoD Trusted Foundry Certification Program

  - QML And ISO90001 Quality Management Systems
  - Experienced Management Team

Proven Source For FPGA Replacements