Actel Space-Flight FPGA Product Update and Roadmap

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Actel Company Overview

Established FPGA Supplier

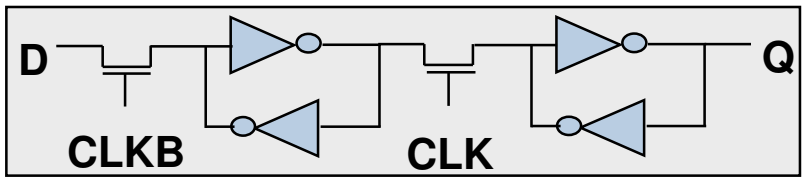
- First FPGA shipped – 1988
- First space FPGA shipped – 1992
- $191M in sales in 2006
- More than 580 employees
- Fabless company
- #1 flash FPGA supplier
- #1 antifuse FPGA supplier
- ~35% of revenue from mil / aero FPGAs

ONE CHIP is all you need

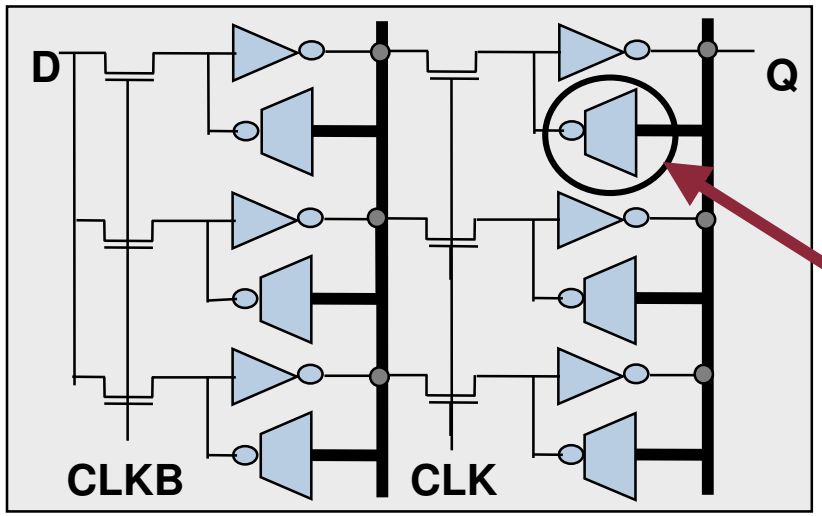
SEU-Enhanced Flip-Flops

Foundation for Actel RTSX-SU and RTAX-S FPGAs

Standard Flip-flop



SEU-Enhanced Flip-flop

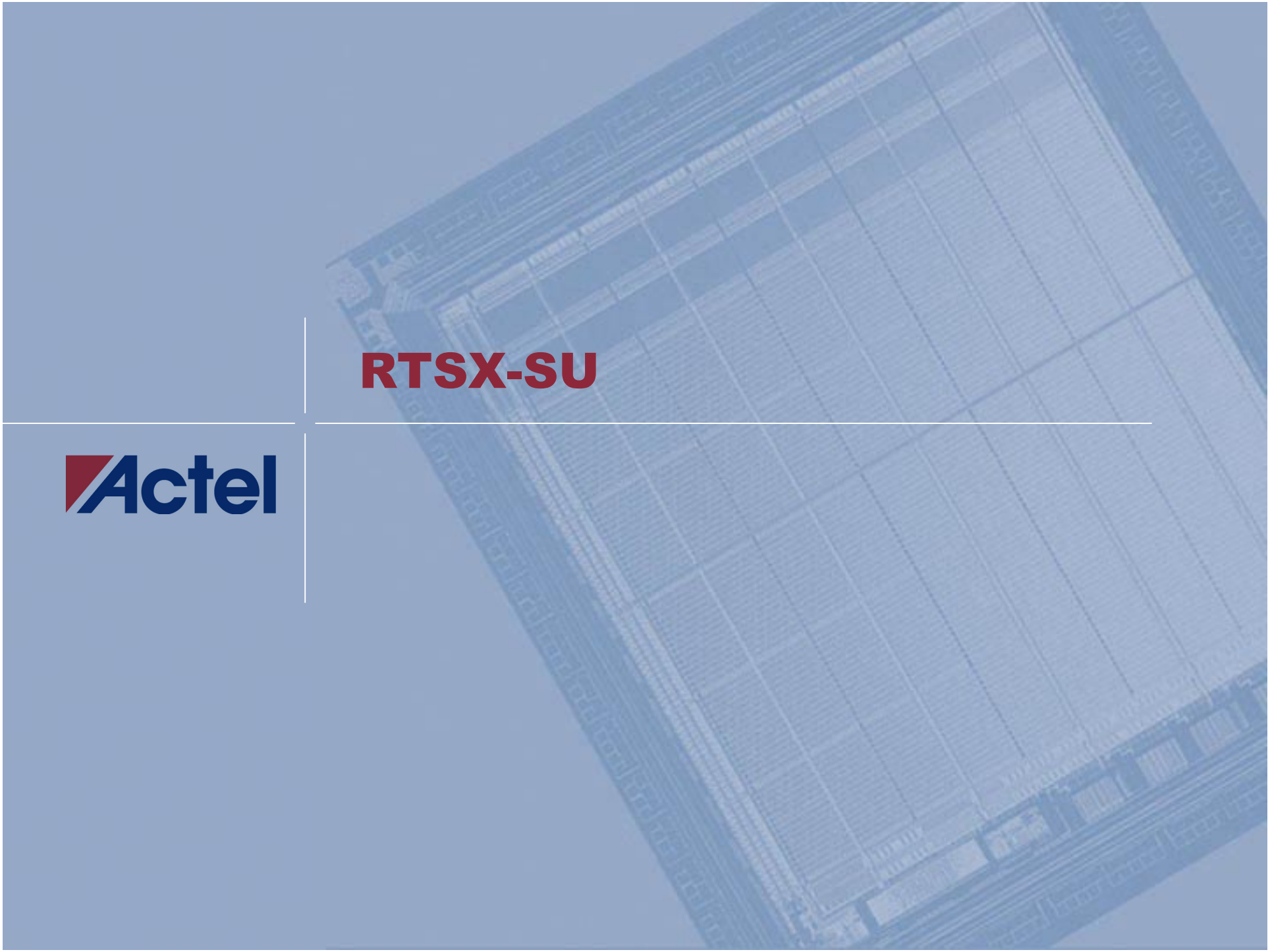


Voter Gate

Actel Advantage

- 100% gate availability - no gate loss to TMR implementation
- Upsets due to single ion strike voted out by the unaffected latches
- Voting the feedback paths prevents the flip flop from changing state
- Transparent to user, no special skill or knowledge needed

RTSX-SU



RTSX-SU Family

RTSX-SU Features

- Designed specifically for Space Applications
- Up to 2,012 SEU Hardened Flip-Flops eliminate user-designed TMR
- Single Event Latch-up Immune
- Supports Hot-Swapping and Cold Sparing
- Configurable I/O support CMOS, TTL, LVTTL, and 3.3V/5.0V PCI
- Secure programming technology prevents reverse engineering
- Pin Compatible with commercial SX-A devices for easy prototyping
- QML Certified Devices

High frequency SET testing

- Tested to 100 MHz at TAMU with NASA GSFC, Oct 2005
- Report available from Actel

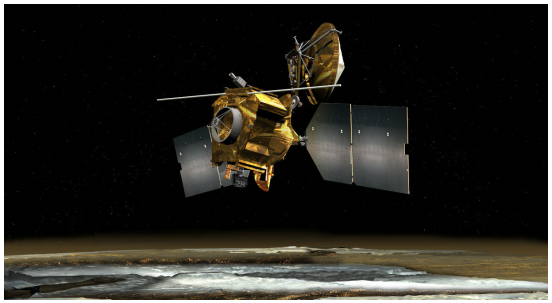
Antifuse Reliability

- Aerospace FIT calculator projects 40 FIT for RTSX72SU, typical design

	RTSX32SU	RTSX72SU
System Gates	48K	108K
Logic Modules	2,880	6,048
Registers	1,080	2,016
Max User I/O	224	353
Packages	84-CQFP 208-CQFP 256-CQFP 256-CCLG	208-CQFP 256-CQFP 624-CCGA 624-LGA

Success in Space – RTSX-SU

Mars Reconnaissance Orbiter
Launched August 2005



Actel RTSX-SU On Board

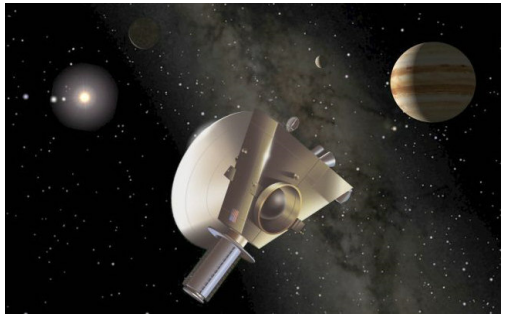
GPS 2R-M Program
First Launch Sept 2005

Actel RTSX-SU On Board

Galileo GIOVE-A
Launched Dec 2005

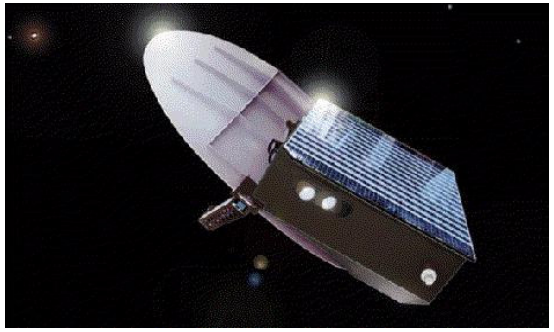
Actel RTSX-SU On Board

New Horizons
Launched Jan 2006



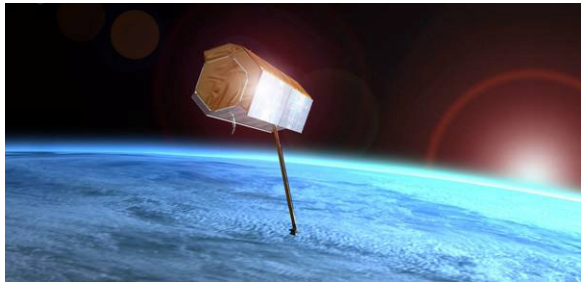
Actel RTSX-SU On Board

SAR-Lupe 1 and 2
First Launch Dec 2006



Actel RTSX-SU On Board

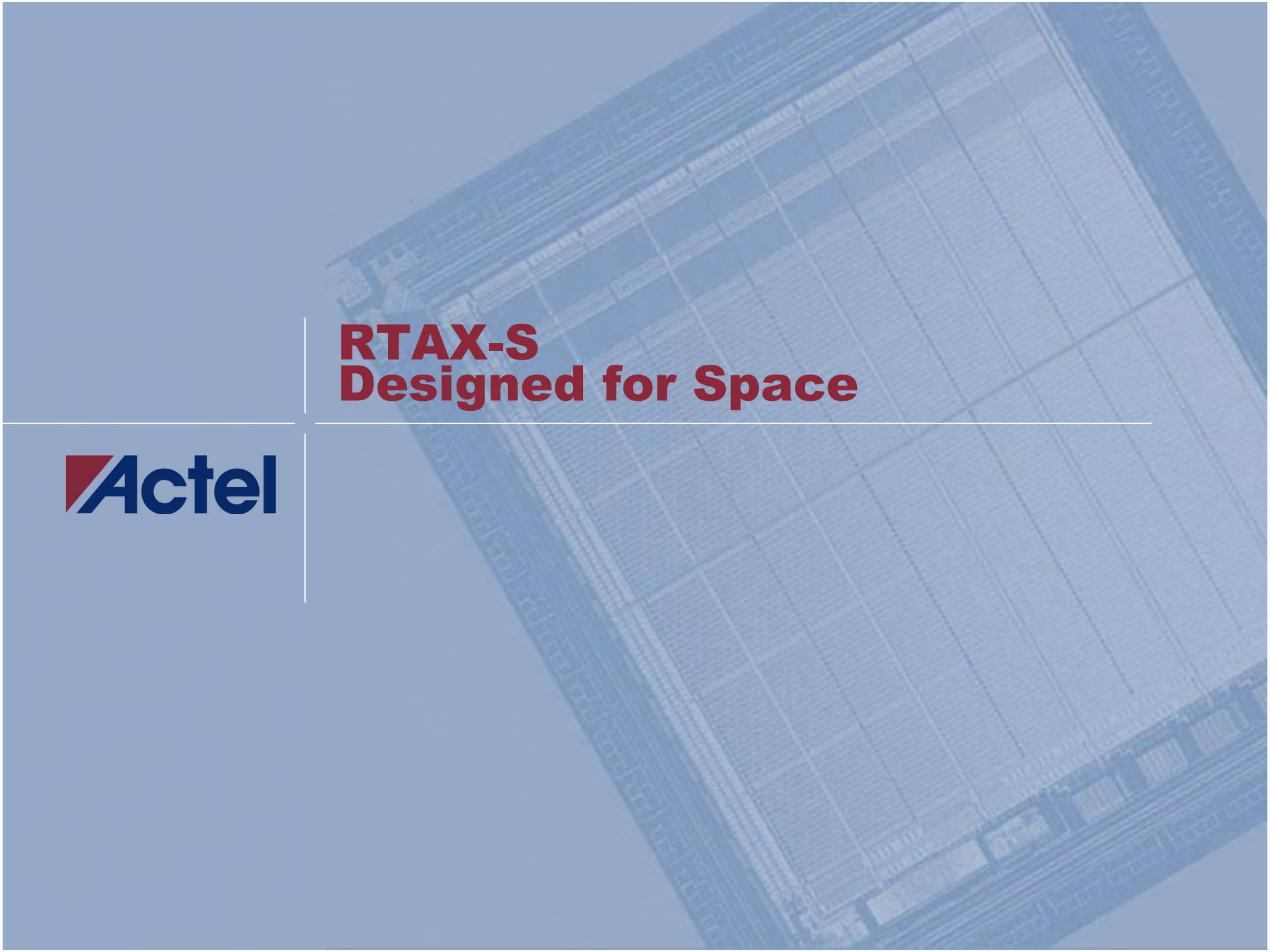
TerraSar X
Launched June 2007



Actel RTSX-SU On Board

- **Many more programs preparing to fly RTSX-SU**

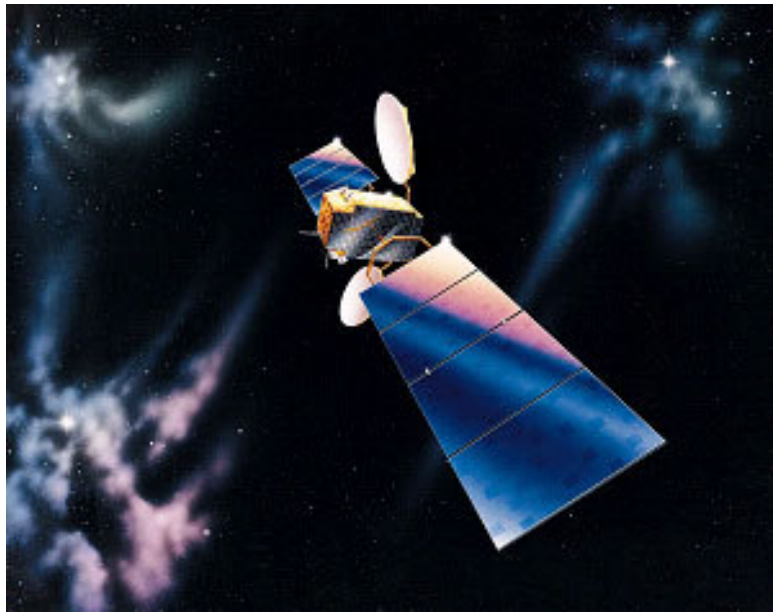
RTAX-S
Designed for Space



RTAX-S

Radiation-tolerant FPGA alternative to RH ASICs

- High density — up to 2 million system gates (approximately 250,000 ASIC gates)
- Five times larger than previous largest space FPGA
- Designed for space — Single Event Upset (SEU) enhancements
- 0.15µm, 7-layer metal CMOS with Antifuse, manufactured at UMC
- Embedded block RAM
- Multiple Flexible I/O standards
- Live at Power-up (LAPU)
- Single chip
- Low power consumption



RTAX-S FPGA Family

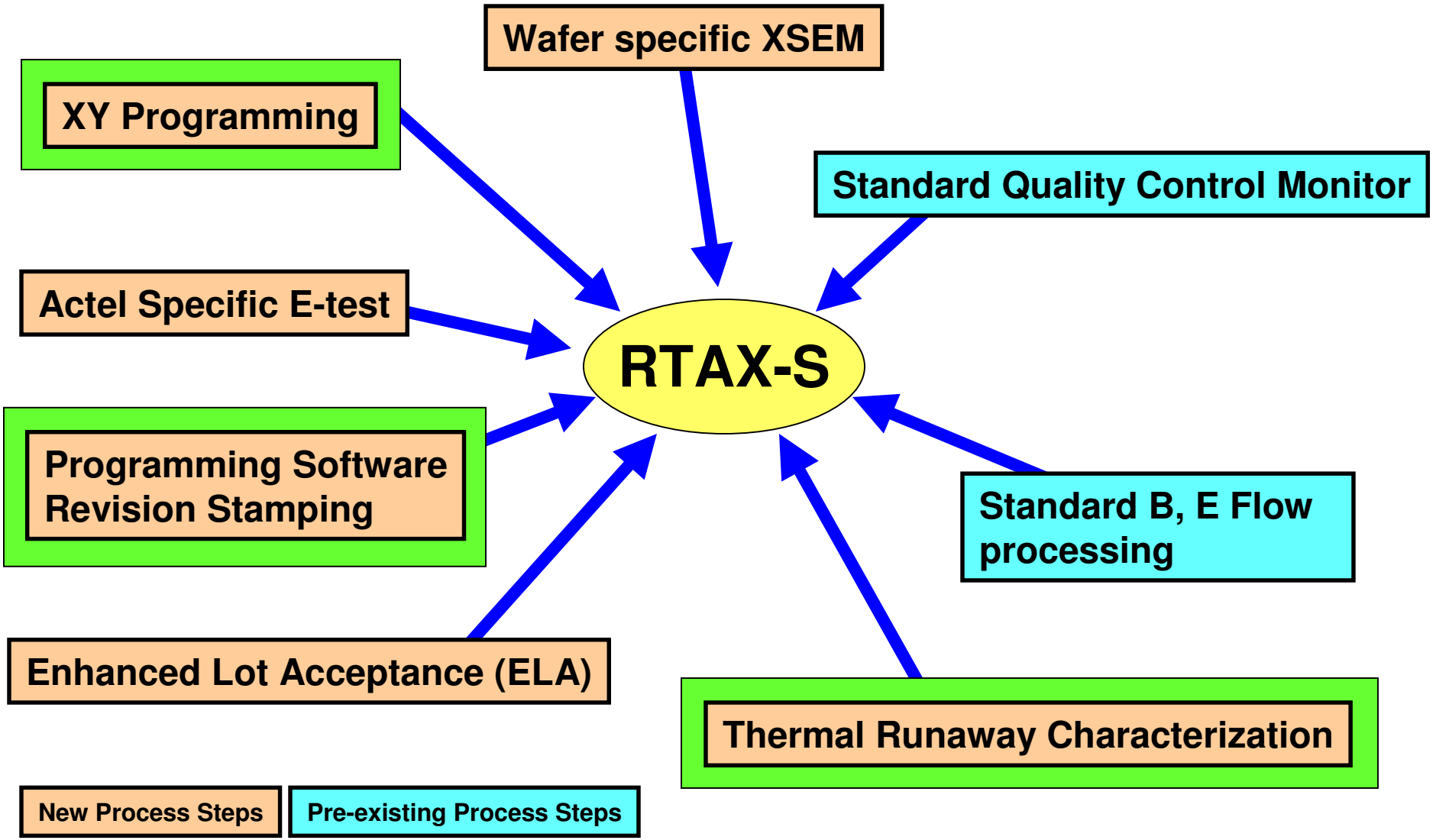
	RTAX250S	RTAX1000S	RTAX2000S	RTAX4000S
Dedicated Registers	1,408	6,048	10,752	20,160
I/O Registers	744	1,548	2,052	2,520
Total Modules	4,224	18,144	32,256	60,480
RAM Blocks	12	36	64	120
Total RAM Bits	54K	162K	288K	540K
Max User I/Os	248	516	684	840
Packages	208-CQFP 352-CQFP	352-CQFP 624-CCGA/LGA	256-CQFP 352-CQFP 624-CCGA/LGA 1152-CCGA/LGA	352-CQFP 1272-CCGA/LGA
Status	***QUALIFIED SILICON NOW SHIPPING!***			***QUAL IN PROGRESS***

RTAX-S Radiation Data

- **Single-event Latch-up (SEL)**
  - Testing performed up to LET 117 MeV-cm^{2}/mg (125ºC)
  - No SEL observed; No control logic upset observed
- **R-Cell Single-event Upset (SEU)**
  - LET_{TH} in excess of 37 MeV-cm^{2}/mg
  - Cross-section < 1E^{-9} cm^{2}
  - SEU per R-Cell < 4E^{-11} Errors/bit-day (worst case GEO)
- **Memory SEU**
  - Cross section / word ~ 4E^{-9} cm^{2}
    - EDAC operational, background scrubbing at 2MHz
  - SEU < 1E^{-10} upsets/bit-day (worst case GEO)
- **Single-event Transient (SET)**
  - High frequency testing to 150 MHz with NASA GSFC
  - Testing of SET mitigation strategies planned for 4Q2007 and 1Q2008
- **Total Ionizing Dose (TID)**
  - Results indicate suitability for vast majority of space missions
    - Stays within parametric limits beyond 200Krads (si)
    - No functional failure up to 300Krads (si)
  - TID performed on each production wafer lot

All reports posted to http://www.actel.com/products/milaero/hireldata.aspx

RTAX-S Production Process Enhancements



RTAX-S Production

XY Wafer Location Programming

- Wafer number and die location on wafer is programmed into each unit during wafer sort
  - Assists with traceability and failure analysis

Programming Software Revision Stamping

- Silicon Sculptor Programming SW revision is programmed into device concurrent with customer design programming
  - Assists with traceability and failure analysis

Thermal Runaway Characterization

- This test is required per wafer lot (started with 2007 fab out lots)
- 2 sample units are programmed with ELA design and characterized at oven temperature of 125°C, 130°C, and 135°C
- Lots that exhibit thermal runaway are scrapped
- Datasheet maximum junction temperature remains unchanged
  - Max T_J = 125°C

RTAX-SL Low Power Family

New family

- Reduced stand-by current
- New part numbers
  - Existing SMDs will be updated with new part numbers
- Applies to all members of the RTAX-S family

Stand-by current spec

- Reduced by 50% relative to standard RTAX-S (worst case conditions)
  - For example RTAX2000SL spec is 250mA at 125°C
- Dynamic current spec is unchanged
- Device timing is unchanged

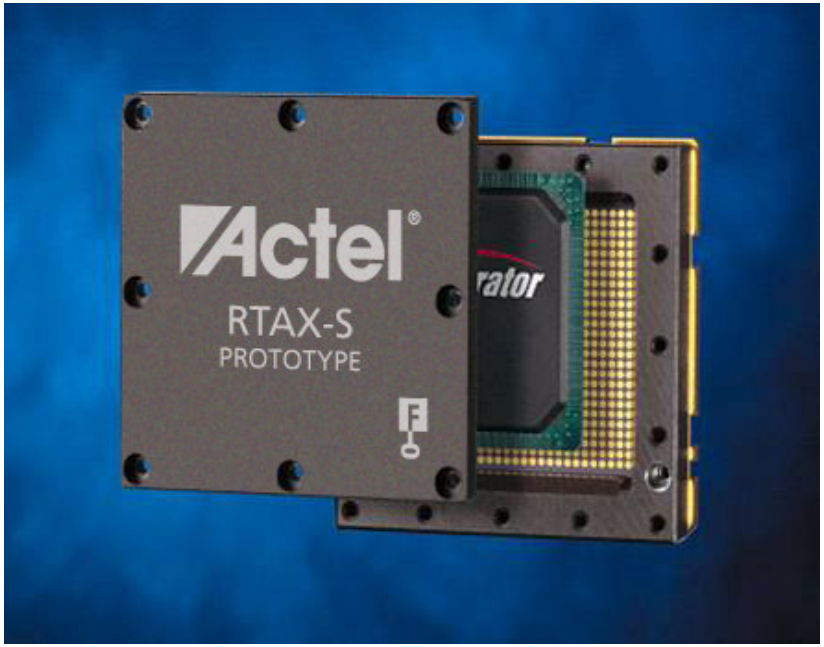
Schedule

- Open for orders NOW
  - Usual lead times will apply

RTAX-S Prototyping

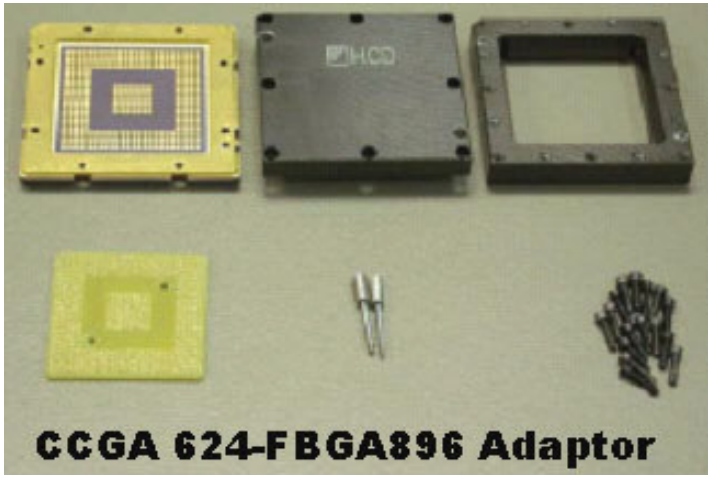
Low Cost Prototyping solution available *NOW!*

- Allows design activity to start immediately
- Uses commercial Axcelerator (AX) silicon in FG896 package for functional verification
- FG896 – CQ352 adaptor
  - Matches CQ352 PCB footprint
- FG896 – CG624 adaptor
  - Matches CG624 PCB footprint

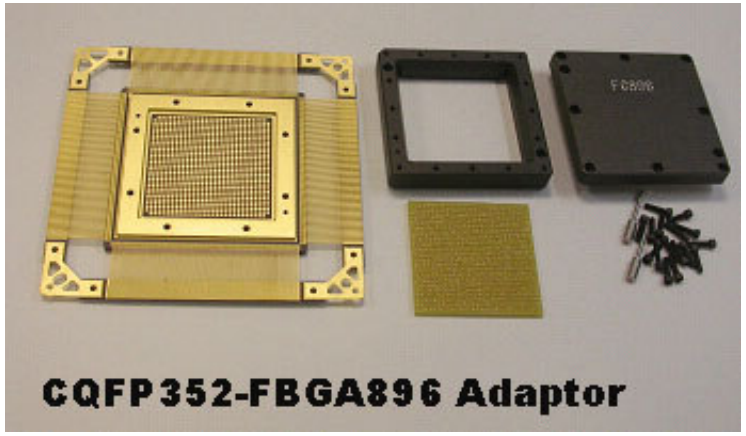


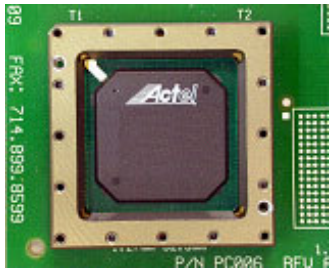
- CQ208 can be prototyped with commercial PQ208 AX FPGAs
- CG1152 can be prototyped with commercial FG1152 AX FPGAs

RTAX-S Low Cost Prototyping Solutions



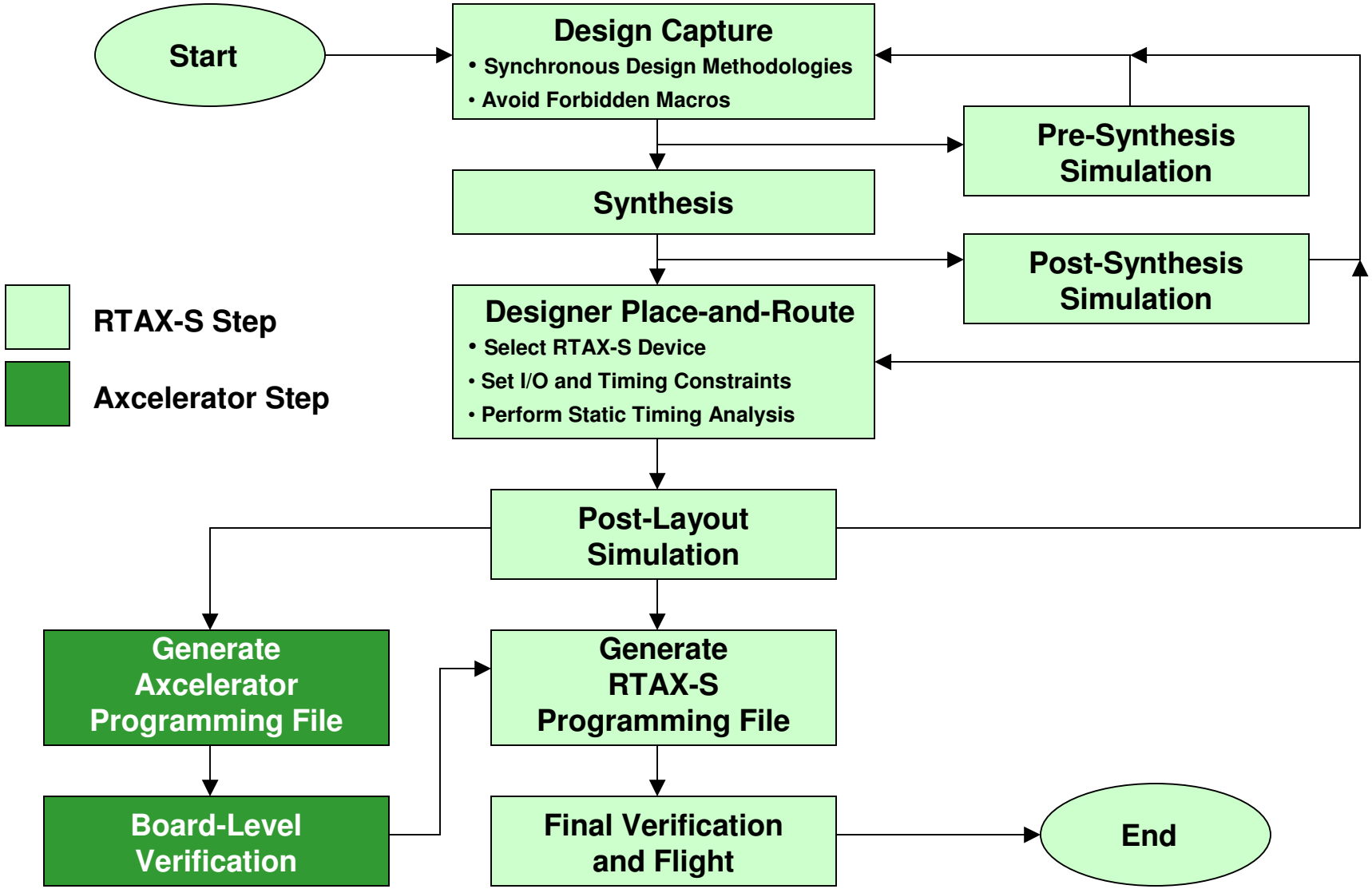
- Low cost prototyping solution
- CCGA and CQFP footprints available
- CCGA adaptor uses solder balls (not columns)
  - Eliminates costly column attach
  - Requires no re-layout





Fully Assembled CCGA 624-FBGA896 Adaptor

RTAX-S Prototyping Flow



Final Verification with RT Silicon

- **Introducing low-cost RT devices for final timing verification**
- **RT-proto FPGAs**
  - RTSX-SU and RTAX-S prototypes
  - RT die, in cost-reduced packages
    - Identical timing and functionality to space-flight RTSX-SU and RTAX-S FPGAs
    - Military temperature testing
    - No Mil-Std 883B processing
    - Non-hermetic lids
    - *Not suitable for space-flight* devices marked to indicate this
    - *Not intended for qualification of space-flight hardware*
  - Open for orders NOW
  - Shipments will start 4Q2007

RTAX-S Qualification Update

RTAX-S Qualification

Mil-Std 883B Qualification

- Qualification completed June 2005
- DSCC released and certified SMDs April 2006
  - RTAX-S devices can now be ordered to the DSCC SMD "5962" number

Enhanced Antifuse Qualification (EAQ)

- Uses design with high observability of timing changes
- 120 units RTAX1000S-CG624 tested
  - ***6000 hours*** HTOL completed
  - 250 hours LTOL completed

Additional Engineering Testing

- HTOL – 1000 Hrs, 125ºC, 173 units
- LTOL – 1000 Hrs, -55ºC, 77 units

No antifuse failures observed in testing to date

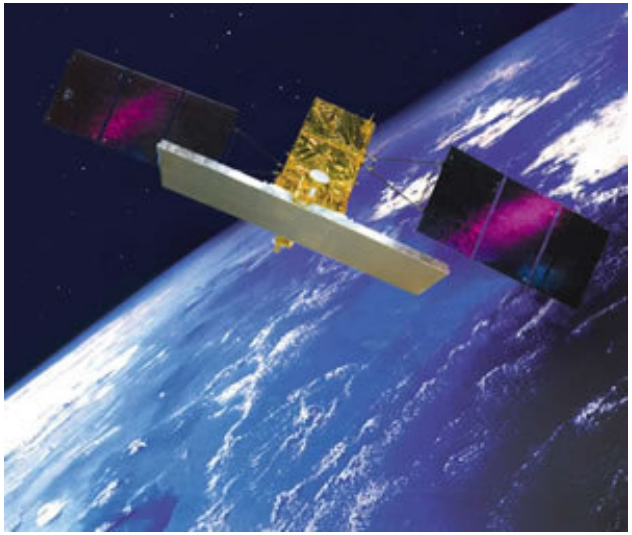
- Over 1.93M device hours of Actel life testing to date
- Additional 1.5M+ device hours of AX testing at Aerospace Corporation
- Overall product FIT rate calculated <7 FIT (60% confidence level, E_A = 0.7eV)

Actel RTAX-S Class V Plan

- **Class V process flow is being established ("EV")**
  - Will comply with current rev of MIL-PRF-38535 (Rev H)
    - Wafer lot specific Group C life test
    - 100% Pre-Cap Source Inspection
    - Lot-specific DPA
  - Actel will offer "EV" class V flow prior to official class V certification
  - Expect no silicon or process differences between official QML class V and Actel "EV" devices
  - Expect availability of Actel "EV" product by end 2007
  - NOTE: Actel has no plans to discontinue existing B-flow or E-flow
- **Will seek QML-V certification**
  - DSCC and Aerospace now reviewing Actel class V proposal
  - Hoping for QML class V certification by end 2008
- **Radiation Hardened Assurance (RHA) development is also under discussion**

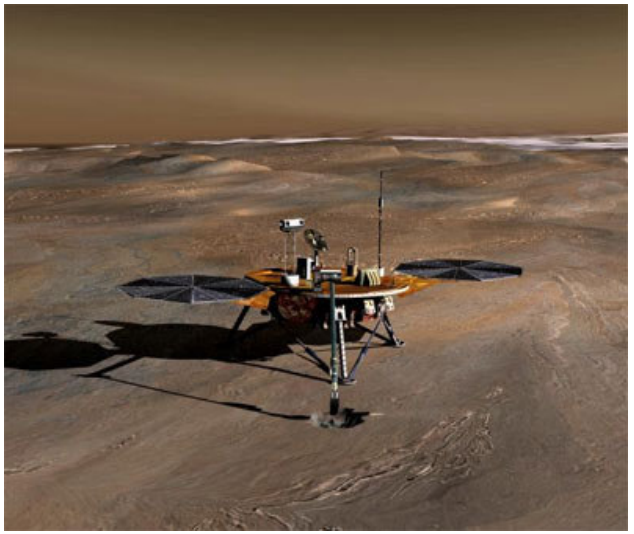
RTAX-S Now in Space!

COSMO SkyMed 1
Launched June 2007



Actel RTAX-S On Board

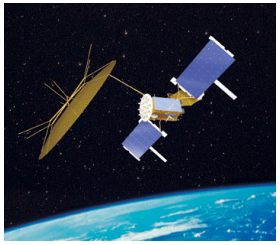
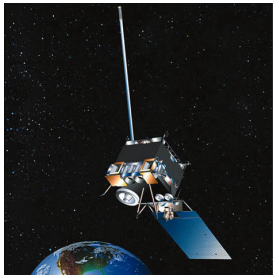
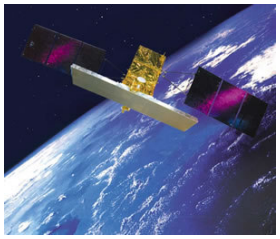
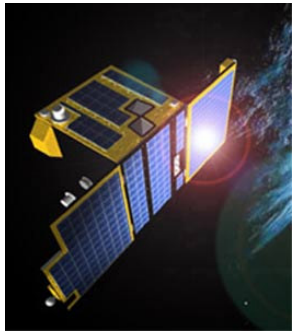
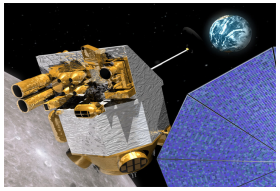
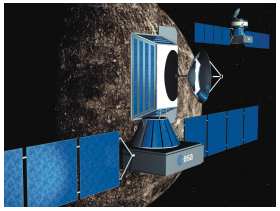
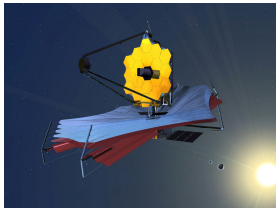
Mars Phoenix
Launched August 2007



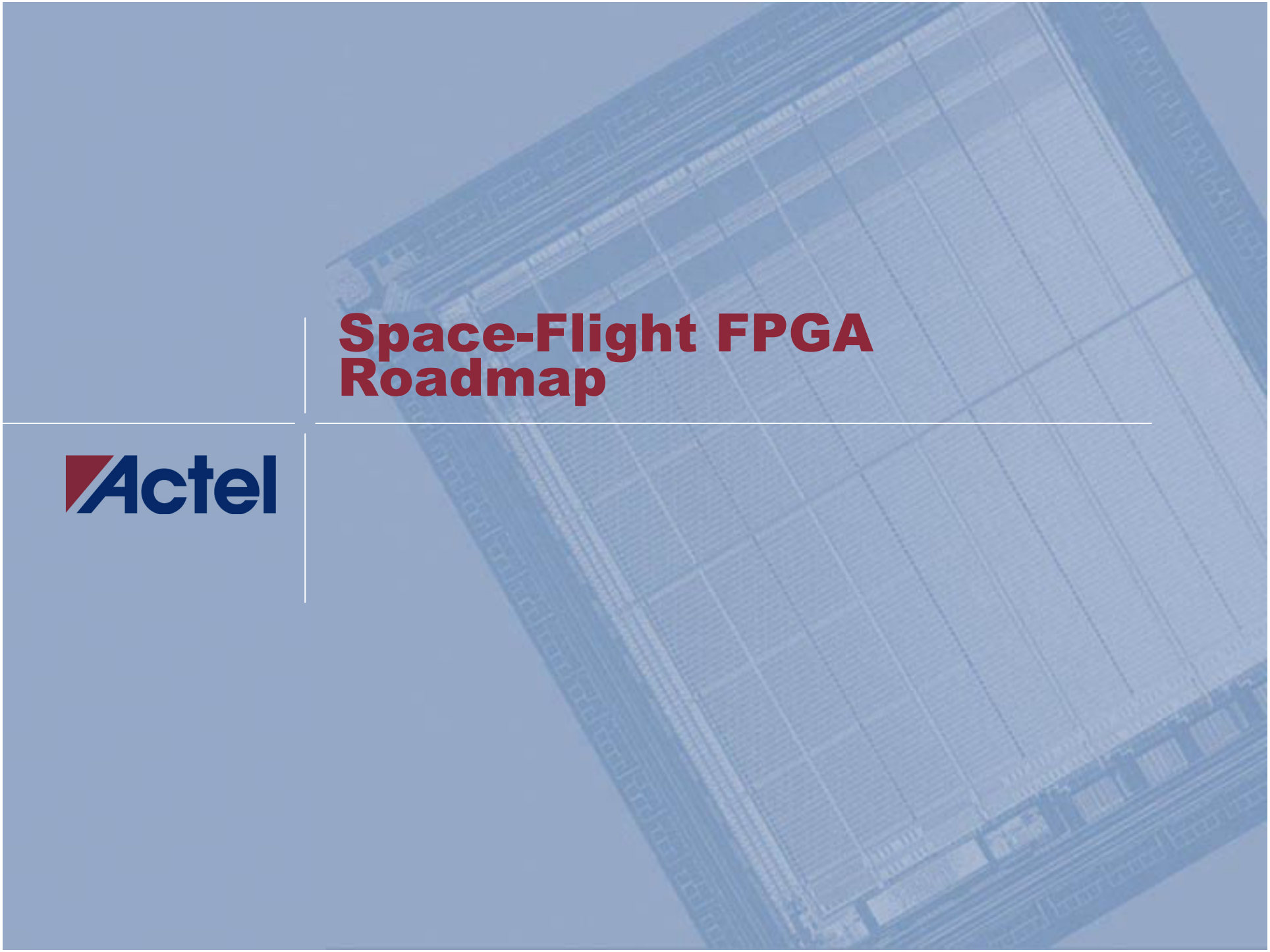
Actel RTAX-S On Board

Programs Planning to Fly RTAX-S

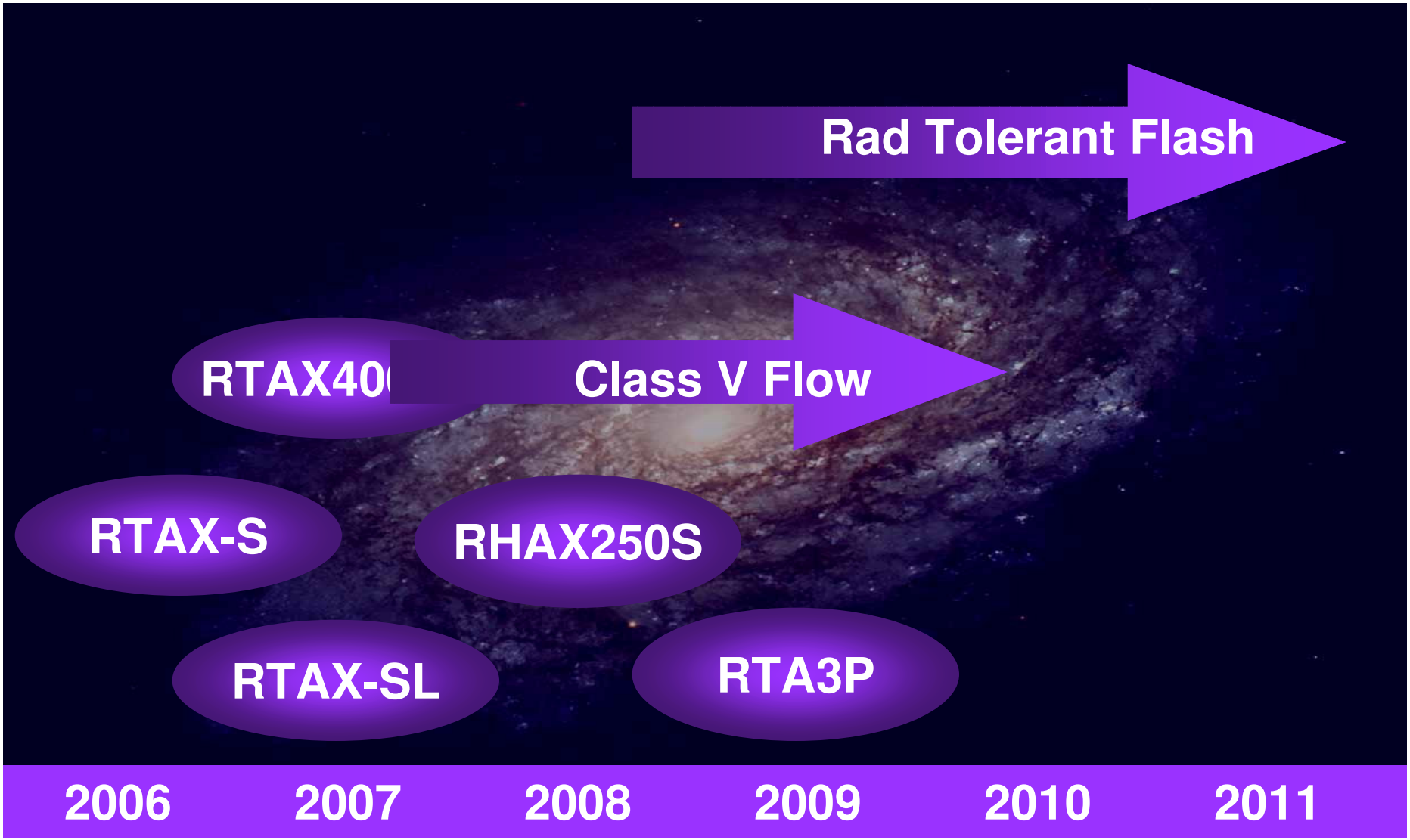
Actel

Galileo	**Advanced EHF**	**NPOESS**	**MUOS**	**GOES-R**	**COSMO SkyMed 2-4**
					
Proba 2	**Lunar Recon. Orbiter**	**Mars Science Lab**	**Bepi Colombo**	**Gaia**	**James Webb Space Telescope**
					

Space-Flight FPGA Roadmap



Roadmap for Space-Flight FPGAs



RTAX4000S Details

Features and Benefits

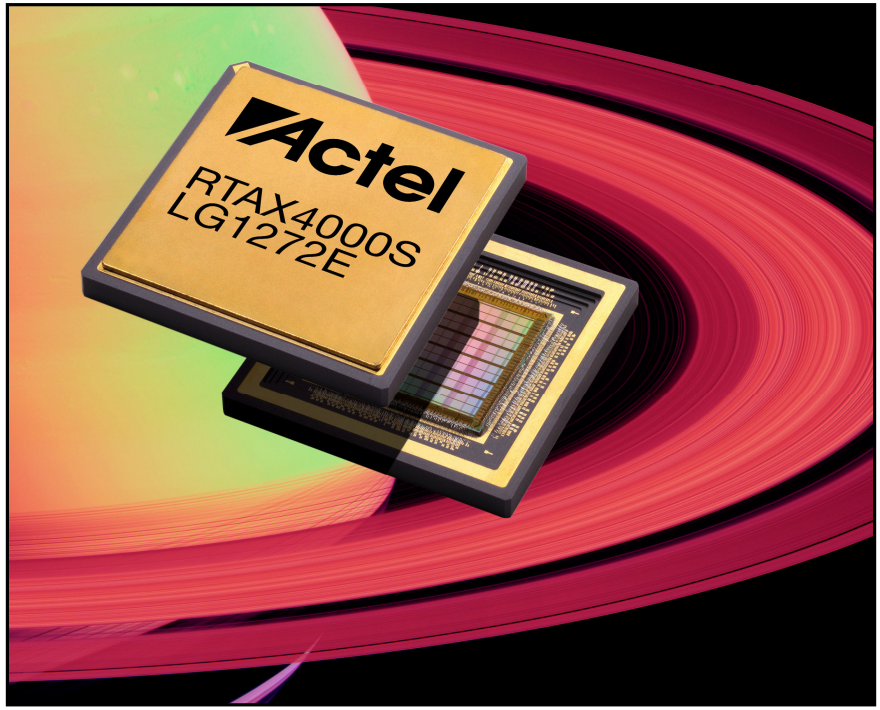
- Double the density of prior largest part – now 500K ASIC gates
  - Enables further reduction of part count, board space, system mass
- 352-CQFP and 1272-CCGA/LGA packaging
- Same process, foundry and architecture as other RTAX-S parts
  - Expect the same radiation specifications
  - Expect the same high reliability

Prototyping

- Special prototyping versions
  - Features, architecture, timing will be identical to flight silicon
  - Lower cost, non-hermetic packages

Schedule

- First silicon at Actel NOW!
- Software available NOW!
- Prototypes available NOW!
- Qualified flight units 1Q2008



RTAX4000S Qualification

Preparation for qualification

- Multiple wafer lots needed to supply qual material
- All required wafer lots have completed wafer sort
- Wafers now going through assembly
  - Long assembly process: production process intended to meet future class V requirement
- Target for Mil-Std 883B qualification complete by early 2008
  - Includes 1000 hour Group C HTOL with 77 units

QML Class V

- Additional qualification activities to occur 2007 ~ 2008
  - To include additional reliability testing
    - *Consulting with Aerospace in defining additional testing*
  - Approval by DSCC, NASA and SMC/Aerospace required
  - Best case targeted for certification by end 2008

RHAX-S

- **Fabricated at BAE-Manassas**
  - RH CMOS process
  - On-shore foundry
  - Using RTAX-S antifuse architecture
- **Easy migration to RHAX-S**
  - Pin compatible with AX250 and RTAX250S
  - Expect timing to be identical to RTAX250S
- **QML Class-V with Rad Hard Assurance**
  - Expect TID to 1 MRad parametric
  - No SEL to >> LET_{TH} 100MeV
  - No configuration SEU
  - Logic SEU < $1E^{-10}$ upsets/bit-day
  - Memory SEU < $1E^{-10}$ upsets/bit-day
- **Software support 1H2008**
- **Flight units 2H2008**

	RHAX250S
Dedicated Registers	1,408
I/O Registers	744
Total Modules	4,224
RAM Blocks	12
Total RAM Bits	54K
Max User I/Os	248
Packages	208-CQFP

Space-Flight Flash FPGAs

RTA3P

- Same silicon as commercial A3P family
- Radiation projections
  - No radiation-induced configuration changes
  - Immune to SEL
  - TID to ~ 20 Krads
  - Soft TMR for protection against data SEUs
  - Suitable for LEO / short duration payloads
- Flight units expected 2009
  - Mil-Std 883B qualified

	RTA3PE600	RTA3PE3000
System Gates	600K	3M
Tiles	13,824	75,264
RAM (Kbits)	108	504
RAM (blocks)	24	112
Flash (ROM) bits	1K	1K
PLLs	6	6
Globals	18	18
Package	CG484	CG484

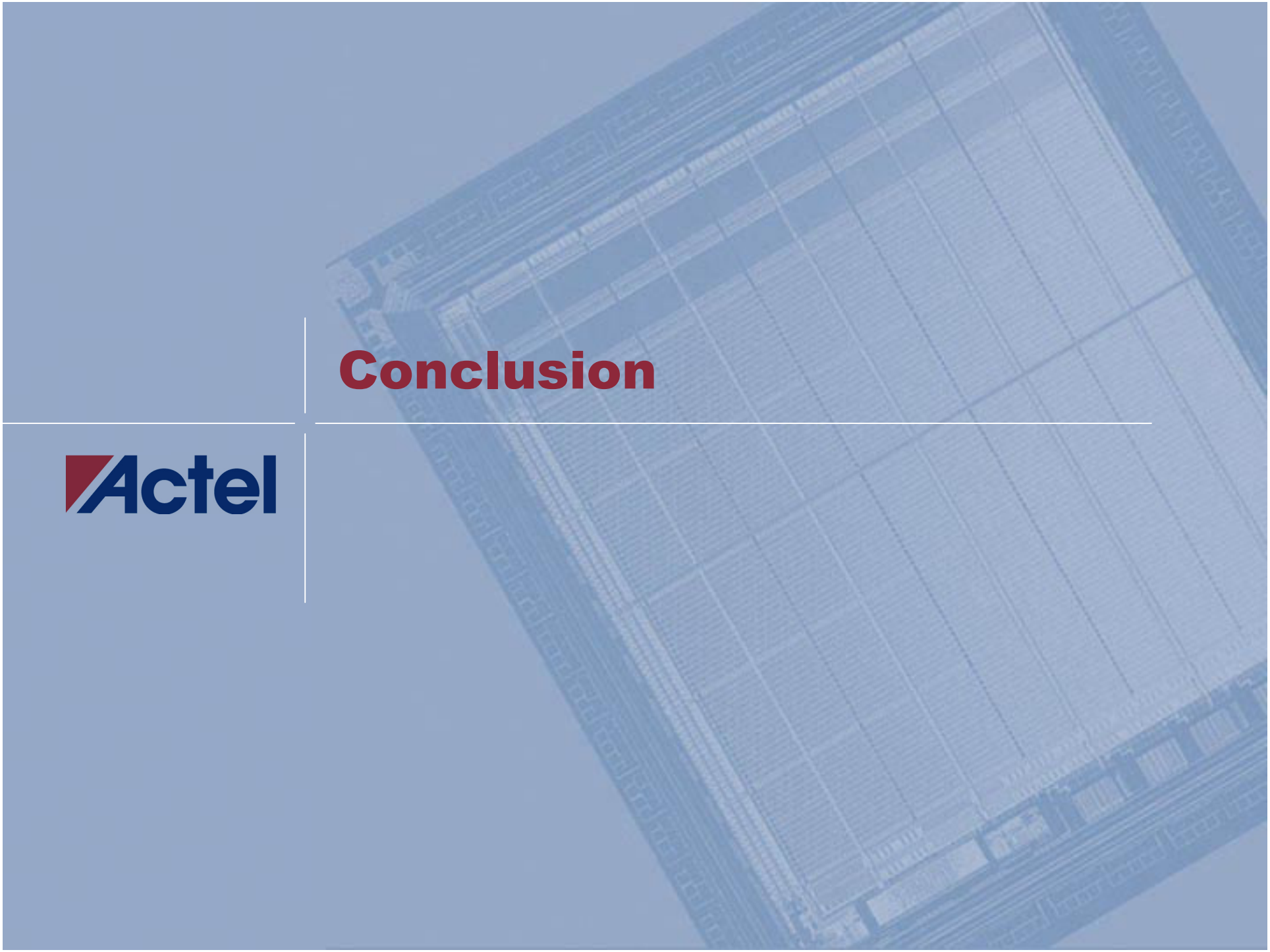
RT Fusion (AFRL Funding)

- Features and schedule being defined currently

RT-G4 (DTRA Funding)

- In architecture concept phase
- Expect flight units 2010 to 2012
- Target TID to 300 Krad
- 5M to 10M system gates

Conclusion



Actel Space Heritage... Second to None!

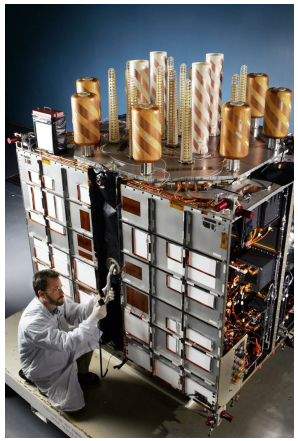
Launchers / Missiles
Delta IV
Sea Launch
VLS
MinuteMan III
THAAD
Pegasus
Arianne Y
H-2A
D5 ENTB
Patriot
Atlas II, V

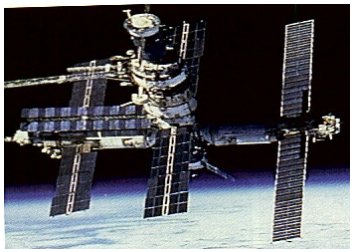
Commercial
Globalstar
Anik F2
Intelsat IX
GE-1,2, . . . 18
Echostar
Telstar
Radarsat I, II
CRSS / IKONOS
OrbView
IndoStar
QuickBird
Hispasat
Astra
WorldStar
Orion 2
KompSa
Orbcom
PanAmSat

Military
MightySat
P81 (Classified)
P59 (Classified)
HESSI
Clementine
SBIRS
AEHF
Myter Joint
GeoLite
WarFighter 1
TSX-5
MTI
STEP
STSS
Midcourse Space Exp
NPP / NPOESS
GPS
MUOS

International
EnviSat
Cluster II
METOP
Rosetta
Champollion
Stentor
Yamal 100
SAC
Sicral
ACeS
L-Star
SOHO
SILEX
Integral
Int'l Space Station
MDS
N-Star
MTSat
ETS VII
JEM
ADEOS II
OICETS
DRTS

Civilian / Scientific
Deep Space I
Mars Pathfinder, Surveyor
Mars MER1 and 2, MRO
Mars: MSL
Contours
Seawinds
SIRTF
Messenger
Lunar Prospector
GALEX
GIFTS
TIROS
Landsat VII
EOS-AM1, Chem1, PM1
Cassini
TDRS
Space Shuttle
Hubble Space Telescope
Windsat
GOES
AXAF
TRMM
XTE
ACE
SMEX
MIDEX
GLAS
NEAR
Timed
FUSE
Genesis





Summary

- **Actel is committed to supporting Military and Aerospace customers**
- **New products bring added value to Space designers**
  - Higher density
  - More features
  - Simplified board design
    - Single-chip
    - Live at power-up
    - Free from configuration radiation effects
  - Non-volatile AND reprogrammable
- **Roadmap to future products which extend these benefits**