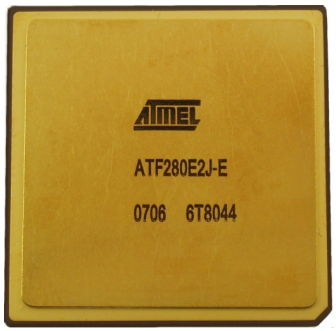
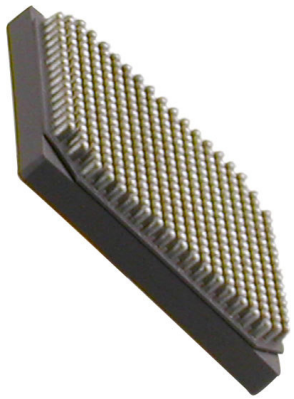
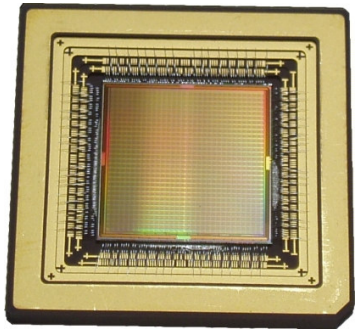
ATMEL ATF280E
Rad-Hard reprogrammable FPGA







Overview

- ATMEL rad-hard FPGA family
- The ATF280E rad-hard reprogrammable FPGA
  - Features
  - Architecture overview
- Securing the ATF280E configuration
- ATF280E hardware & software design tools
- Applications
- The AT69170E serial EEPROM

ATMEL rad-hard FPGA family

- Re-programmable (SRAM based technology)
  - Reliability
  - Unlimited reprogramming
  - Easy to debug
  - Engineering models representative of flight models
- No need for SEU mitigation
  - SEU hardened memory points
- Heritage from existing AT40KEL040 40Kgates rad-hard FPGA
  - Current designs on-going for space applications
- Complemented with a rad-hard EEPROM for FPGA configuration
  - 1 Mbit serial
  - 4 Mbit serial

ATF280E Overview

- Second generation of ATMEL rad-hard FPGAs
  - Relies on ATMEL rad-hard 0.18µm ASIC technology for space
    - DSCC qualified
    - ESCC qualification ongoing
  - Supported by CNES (french space agency)

- Radiation Hardened
  - Heavy ions induced SEU Fault-Tolerance by design
  - SET hardening (clocks and reset)
    - 1 E-6 error/device/day in GEO
  - Total Ionizing Dose up to 300 Krad
  - No Single Event Latchup at 95 MeV/mg/cm2 – 125°C

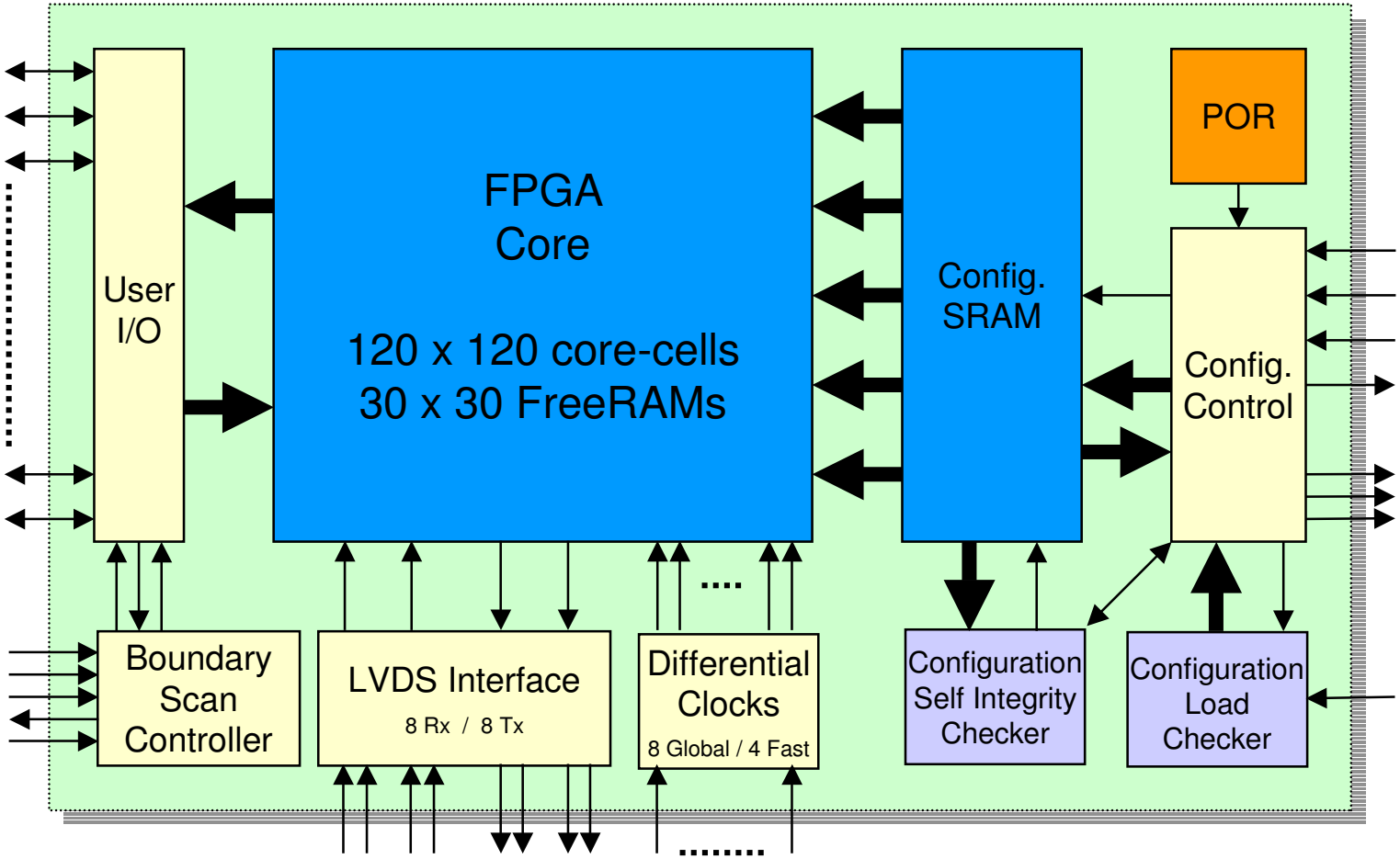
ATF280E Key Features

- 280K equivalent ASIC gates
- 50 MHz clock speed
- 14400 core-cells (each 2 LUT + 1 DFF)
- 115 Kbit SRAM/TPRAM (900 modules of 32x4 blocks)
- 1.8V Core / 1.8V and 3.3V I/Os
- LVDS: 8 Rx + 8 Tx
- Cold-sparing and 3.3V PCI-compliant I/Os

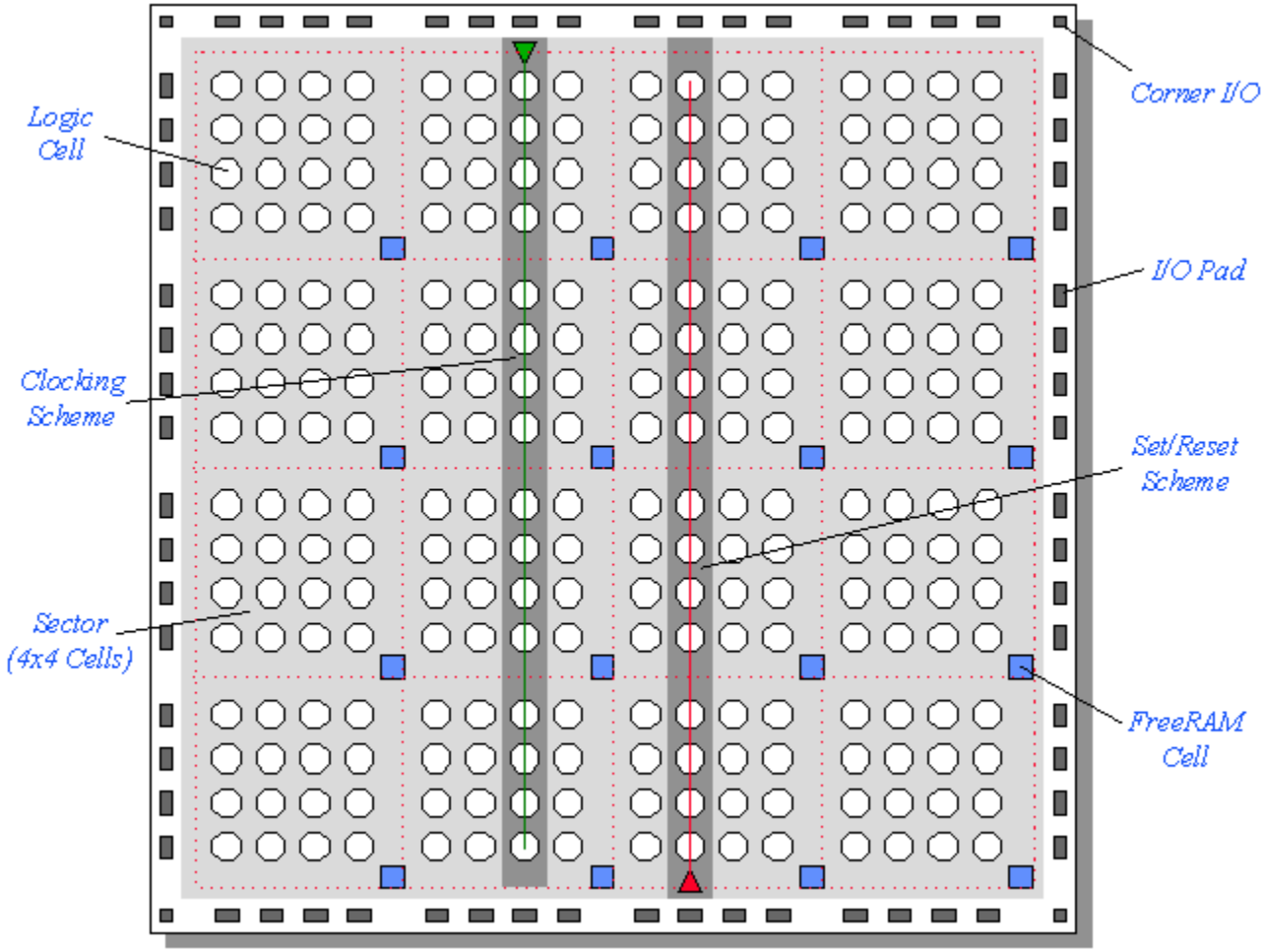
- MCGA 472 (308 User I/O) / MQFP-256 (150 User I/O)

- Configuration load integrity check
- Configuration self-integrity check
- Boundary scan interface

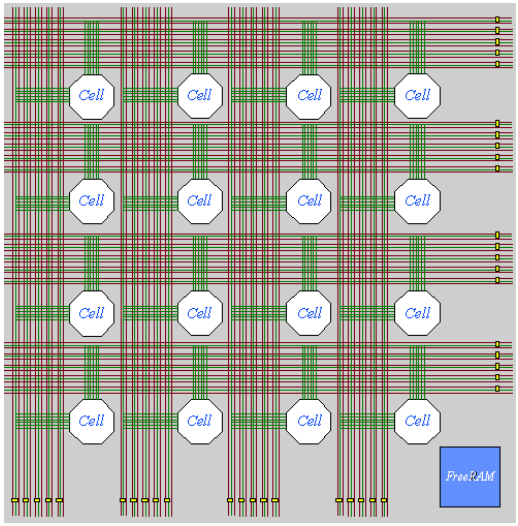
ATF280E Block-Diagram



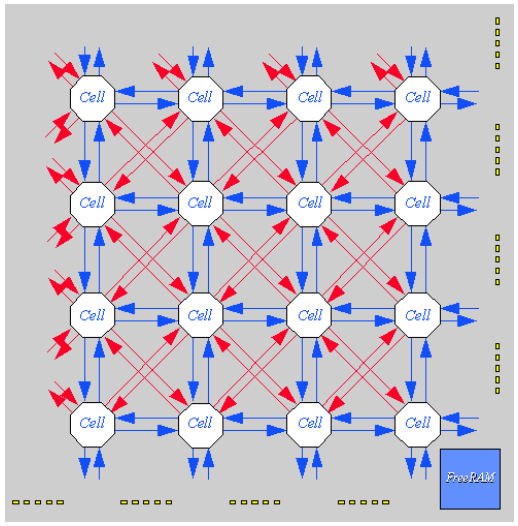
FPGA Architecture Overview



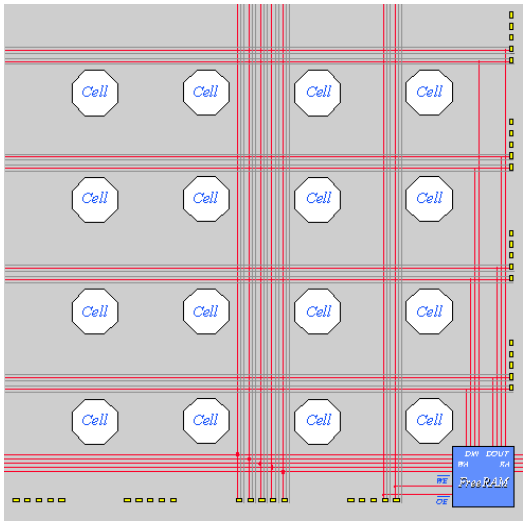
Efficient Routing Architecture



Cell to bus connection



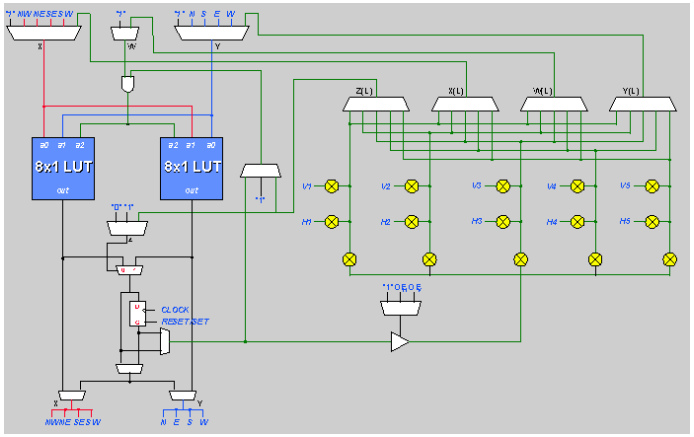
Cell to cell connection



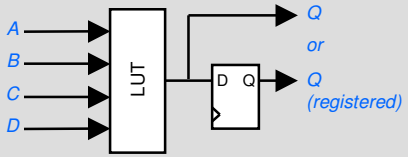
FreeRAM to bus connection

- **Efficient functions using almost only cell to cell connections**
- **FreeRAM uses very few global routing (address) and local (data) routing bus (free otherwise)**
- **Most of the routing structure is still available even if using all core-cells and FreeRAM**

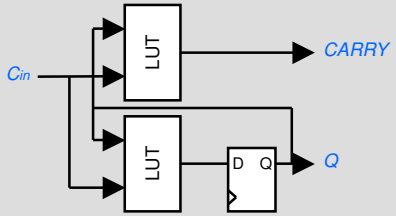
Core-Cell Modes



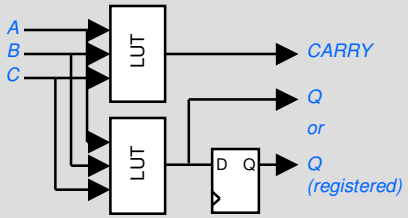
Synthesis Mode



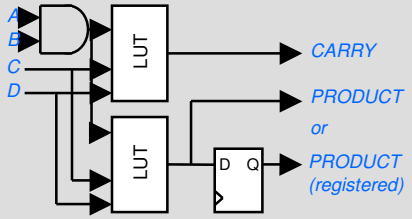
Counter Mode



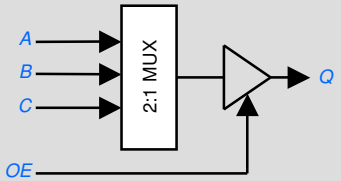
Arithmetic Mode



DSP/Multiplier Mode

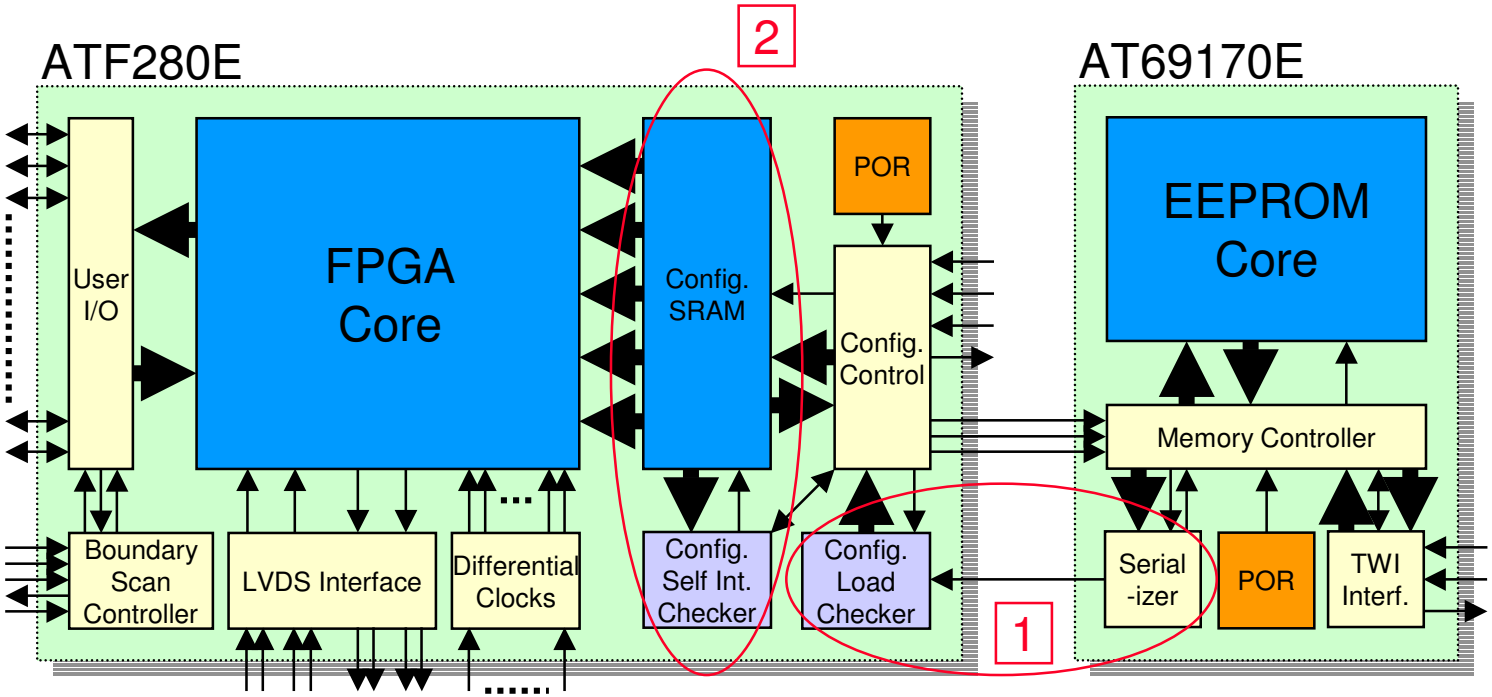


Tri-State/Mux Mode



- Efficient operators only use 1 core-cell / bit
- Fast multi-bit operators using cell to cell diagonal/orthogonal connections
- Pipelining (DFF) possible inside core-cell

Securing FPGA Configuration

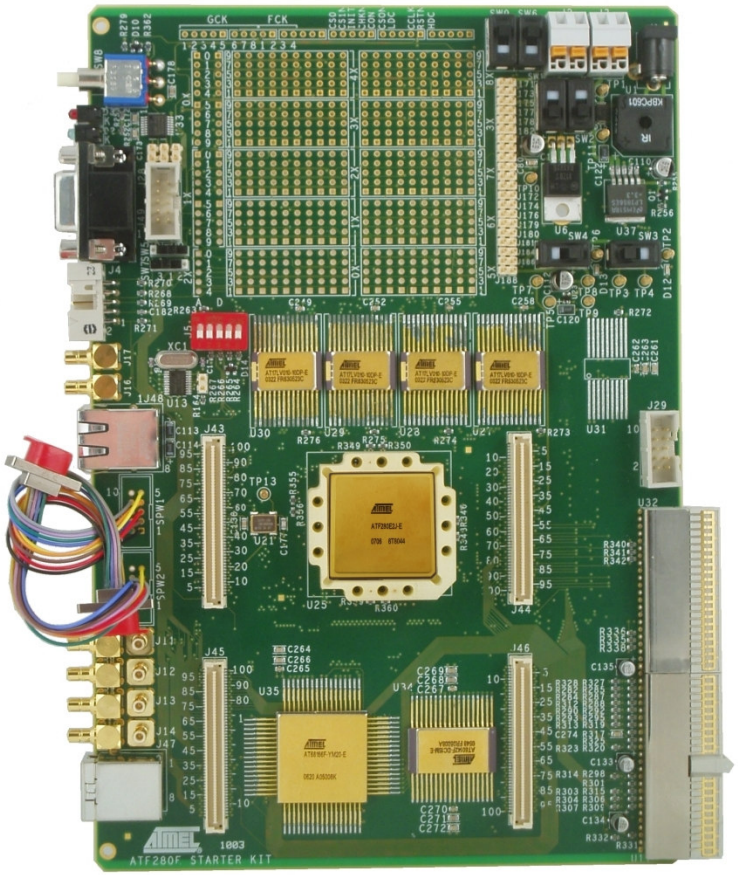


- SRAM-based FPGAs reload their configuration on power-up

  [1] Configuration Load checker (CRC) secures bitstream download

  [2] Configuration Self-Integrity checker secures internal configuration during operation

ATF280E Compact-PCI Evaluation Board



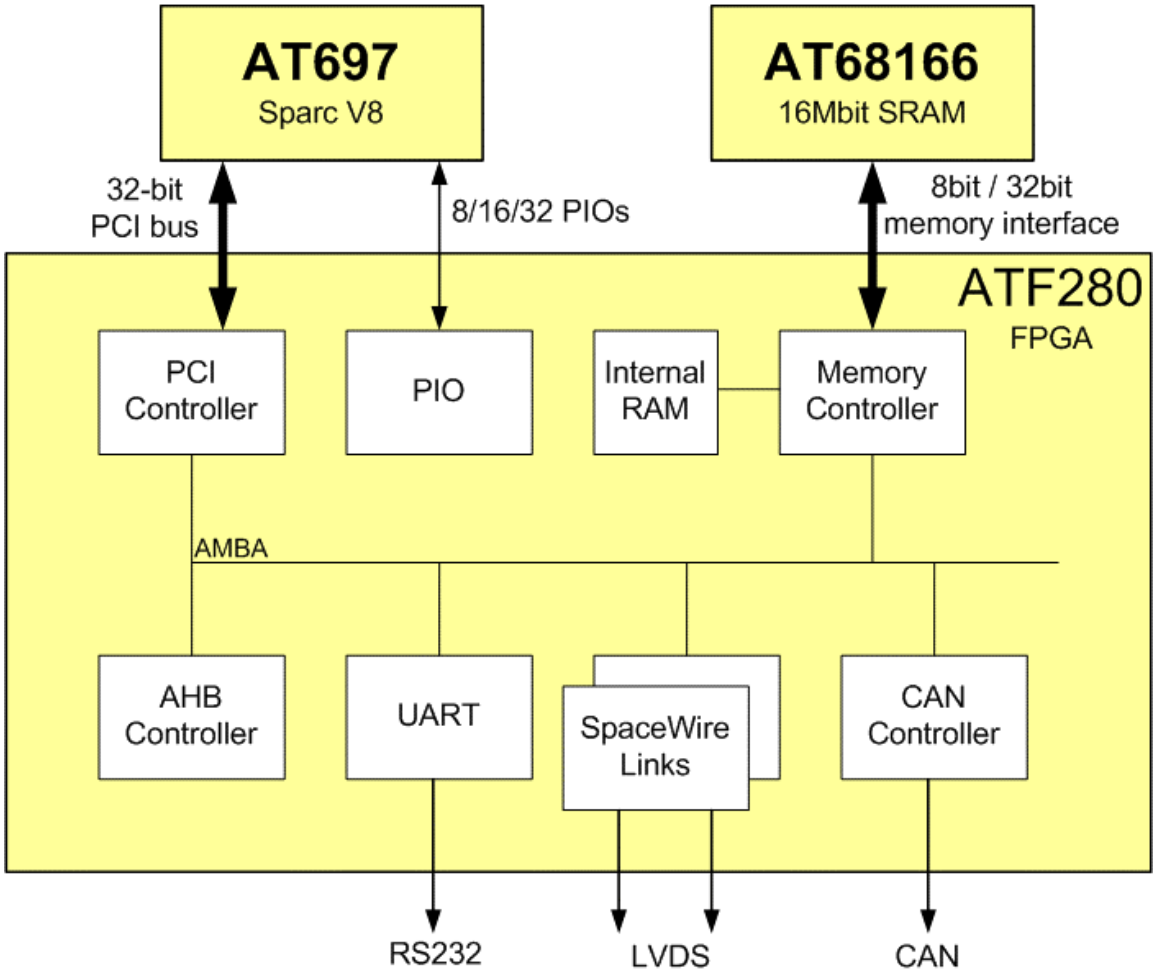
- Compact PCI plug-in format
  - 6U format, 32 bit, 33MHz interface
  - Suitable for Peripheral slot
- On-board Atmel devices
  - ATF280E (MCGA-472)
  - AT69170E / 4 x AT17LV010 EEPROM
  - AT60142 + AT68166 SRAM
- Front-panel connectors
  - 2 x Mini-DB9 (LVDS: 4Tx + 4Rx)
  - 8 x SMB (LVDS: 2Tx + 2Rx)
  - 1 x RJ45 (LVDS: 2Tx + 2Rx)
  - 1 x DB9 (RS232)
- On-board supply for standalone use
- On-board clock sources
- Probe / extension capability

ATF280E Design Tools

- **Front-End**
  - Mentor Graphics Modelsim for VHDL/VERILOG simulation
  - Mentor Graphics Precision Synthesis
    - VHDL / Verilog entry
    - Automatic IDS Macro detection and mapping
- **Back-End**
  - Atmel Figaro IDS
    - Automated Place & Route
    - VHDL / Verilog netlist export with SDF back-annotation
    - Bitstream generation
  - Atmel Configurator Programming Tool
    - Atmel EEPROM support
    - Used during development and ISP in final application

Applications

- the ATF280 as a companion chip for the AT697 processor



AT69170E rad-hard EEPROM

- Atmel's first rad-hard by design serial EEPROM
  - AT58K85RHA 0.18µm technology
  - 5 E-7 error/device/day target in GEO
  - TID target > 60 Krad
- ATF280E configuration download companion chip
- Supported by ESA

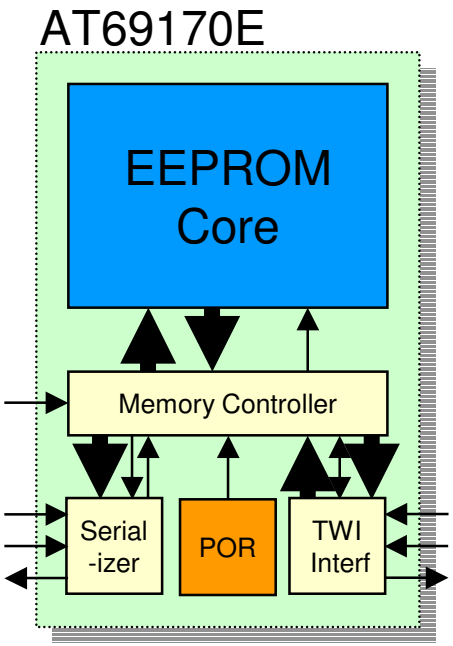
AT69170E Key Features

- 4 Mbit Rad Hard EEPROM
- 512 bytes Pages

- FPGA serial configuration interface
- Standard TWI programming interface

- 3.3V Supply Voltage
- FP18 Package

- Endurance: 10K cycles
- Data retention: 10 years



Schedule

- ATF280E
  - Engineering models in April 2008
  - Flight models by the end of 2008
  - Design kit and tools available
- AT69170E
  - Engineering models in Q1 2008
  - Flight models by the end of 2008

Conclusion

- Building of a family of reprogrammable FPGAs for space
  - AT40KEL040
    - 40 Kgates
  - ATF280E
    - 280 Kgates
  - Rad-hard 4 Mbit EEPROM for FPGA configuration
  - Long-term strategy

- Re-enforce the ATMEL rad-hard products family
  - Sparc processors
  - SRAM memories
  - SpaceWire communication chips, SpW Router
  - ASIC families