New Reprogrammable & Non-Volatile Radiation Tolerant FPGA RTA3P “Low Power”

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This work is partially supported by AFRL/DUS&T and DTRA

Military and Aerospace FPGA and Applications (MAFA) Meeting
11/27/2007
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   1. FPGA’s Features
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## Motivations & Objectives

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<th>SWITCH</th>
<th>SRAM</th>
<th>FLASH</th>
<th>Antifuse</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PROGRAMMABILITY</strong></td>
<td><strong>Re-programmable</strong> (&lt;10⁶ times)</td>
<td><strong>Re-programmable</strong> (1000 times)</td>
<td><strong>One time programmable</strong></td>
</tr>
<tr>
<td><strong>VOLATILITY</strong></td>
<td>Volatile</td>
<td><strong>Non-volatile</strong></td>
<td><strong>Non-volatile</strong></td>
</tr>
<tr>
<td><strong>POWER CONSUMPTION</strong></td>
<td><strong>Medium to High</strong></td>
<td><strong>Very Low</strong></td>
<td><strong>Low</strong></td>
</tr>
<tr>
<td><strong>MANUFACTURABILITY</strong></td>
<td>Standard CMOS process</td>
<td><strong>Standard FLASH process</strong></td>
<td><strong>Special Antifuse process</strong></td>
</tr>
<tr>
<td><strong>SEE SENSITIVITY</strong></td>
<td>Very sensitive to SEE</td>
<td><strong>Relatively insensitive to SEE</strong></td>
<td><strong>Immune to SEU</strong></td>
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### SEE Sensitivities

#### ASIC
- CMOS Logic is SET Sensitive

#### Antifuse: “One Time Programmable ASIC”
- CMOS Logic is SET Sensitive

#### SRAM-Based FPGA: “Volatile Re Programmable ASIC”
- CMOS Logic is SET Sensitive
- SRAM switches are **SEU** sensitive

#### 2T Flash-Based FPGA: “Non-Volatile Reprogrammable ASIC”
- CMOS Logic is SET Sensitive
- 2T Flash switches are **SET** sensitive
For Volatile FPGA: TMR is required for the Combinational Logic

+ Fast Scrubbing to avoid accumulation of errors
Non-Volatile FPGA: TMR is not required for Combinational Logic or the scrubbing of the configuration memory
1. Sequential Logic should be TMR’d.
2. Combinational Logic should be filtered at the inputs of the sequential logic.
3. No Scrubbing of the configuration memory is required because the configuration memory simply does not upset.
SET Characterization & Mitigation

M. Baze, Boeing, NSREC 2006.

FPGA Implementation

SET Cross-Section Measurements

SET Pulse Width Measurements & Mitigation
Proposed SEE Mitigation Technique

With No Logic Duplication

With Logic Duplication
FlashROM is SEU immune and could be used for boot code for embedded processors.

- SRAM is SEE sensitive but EDAC could be employed for mitigation.
SEU in DFF can be mitigated by TMR.

At low frequency (2 MHz), no SET was observed on the IOs (including the Clock).

At 16MHz, SET on the IOs (including the Clock) were seen only at very high LET (68 MeV/cm²/mg).
Each set of tripled Input or Output must use 3 different IO banks

**Design:** 486 LCI: So 100% of logic tiles are used
A3P SET Mitigation

![Graph showing SET cross-sections vs LET (MeV-cm\(^2\)/mg)](image)

- XS_1LCI
- SET-Wd>1ns
- SET-Wd>2ns
- SET-Wd>3ns
- SET-Wd>4ns

Parameters:
- LET\(_{th}\)
- \(O_{sat}\)
Partial SEE Mitigation

Without Mitigation of the IO Banks

- **SET Filtering** (Comb. Logic) + TMR (Seq. Logic)
  - 75% of the FPGA Core
  - All IOs are tripled and separated on 3 # IO Banks

Full SEE Mitigation

With Mitigation of the IO Banks

- **TMR ALL**
  - 85% of the FPGA Core
  - All IOs are tripled and separated on 3 # IO Banks
A3P Radiation Test Results

**Partial SEE Mitigation**

- **TMR-ALL**
  - XS/IO-Bank= 2x 10^{-6} cm^2/IO-Bank
  - 10 % time penalty

- **SET Filtering (+ TMR)**
  - XS/IO-Bank= 2x 10^{-6} cm^2/IO-Bank
  - XS/IO-Bank= 2x 10^{-7} cm^2/IO-Bank if Clock filtered
  - 30 % time penalty

**Full SEE Mitigation**

- **TMR-ALL**
  - Full SEE Immunity
  - 10 % time penalty

- **SET Filtering (+ TMR)**
  - A delay of 6 LCI guarantee SEE immunity for LET < 43 MeV-cm^2/mg
  - 30 % time penalty
A3P SEE Mitigation With Logic Duplication

![Diagram of logic circuits and graphs showing SET Filtering and cross-sections.](image-url)

- SET_Filtering (3ns)_50MHz
- TMR_ALL_50MHz
- SET_Filtering (Duplication)
- SET_Filtering (Duplication with Opt)

Graph: SET Cross Section (cm²/Design) vs. LET (MeV/cm²/mg)

- D1
- D2
- GG
- Out
- Clk
AGL ‘IGLOO’ FPGA Features

- CCC
- RAM Block: 4,608-Bit Dual-Port SRAM or FIFO Block
- I/Os
- VersaTile
- RAM Block: 4,608-Bit Dual-Port SRAM or FIFO Block (AGL600 and AGL1000)

- ISP AES Decryption
- User Nonvolatile FlashRom
- Charge Pumps
Low-Power FPGA (AGL)

AGL

- Flash FPGA

Cyclone3

- SRAM FPGA

Spartan3AN

- SRAM Hybrid FPGA

CoolRunner2

- Low-Power CPLD

Battery Life (hours)

Calculated with 50% Idle and 50% at 100 MHz Operation
AGL SEE Characterization

**IOs**

- IO_Ch_SET
- IO_Bk_SET
- IO_Bk_WSET

**SEU - DFF**

- 2 MHz
- 16 MHz
- DFF_XS_A3P

**SET - Comb. Logic**

- XS_1LCI
- A3P_SET_XS
AGL SEE Mitigation

A3P

Faster

AGL

Lower In Power

To Be Done

- SET Characterization (measurements of SET pulse widths)
- SEE Characterization in Freeze Mode
Telecommunications (SDR..)
As long as it meets the TID Requirements
Summary & Recommendations

- Complete SEE Characterization & Mitigation of A3P => RTA3P
  - **TMR All**
    - Full SEE Immunity
    - 4 times Hardware overhead; 15% time penalty
  - **SET Filtering (combinational logic) + TMR (sequential logic)**
    - A delay of 6 LCI guarantee SEE immunity for LET < 43 MeV-cm²/mg
      - 30% time penalty
    - A delay of 8 LCI guarantee Full SEE immunity for LET < 96 MeV-cm²/mg
      - 40% time penalty
    - Logic Duplication guarantee SEE immunity for LET < 43 MeV-cm²/mg
      - 10% time penalty
  - **Embedded Systems Applications: Processors (8051, ARM, FT-Leon3, DSP...)**
  - **Flight Parts should be available in 2009**

- AGL: Lowest Power FPGA
  - SEE Characterization & Mitigation
  - Results show the same radiation sensitivity as for the A3P
  - TBD: SEE Characterization in Freeze Mode