New Reprogrammable & Non-Volatile Radiation Tolerant FPGA RTA3P "Low Power"

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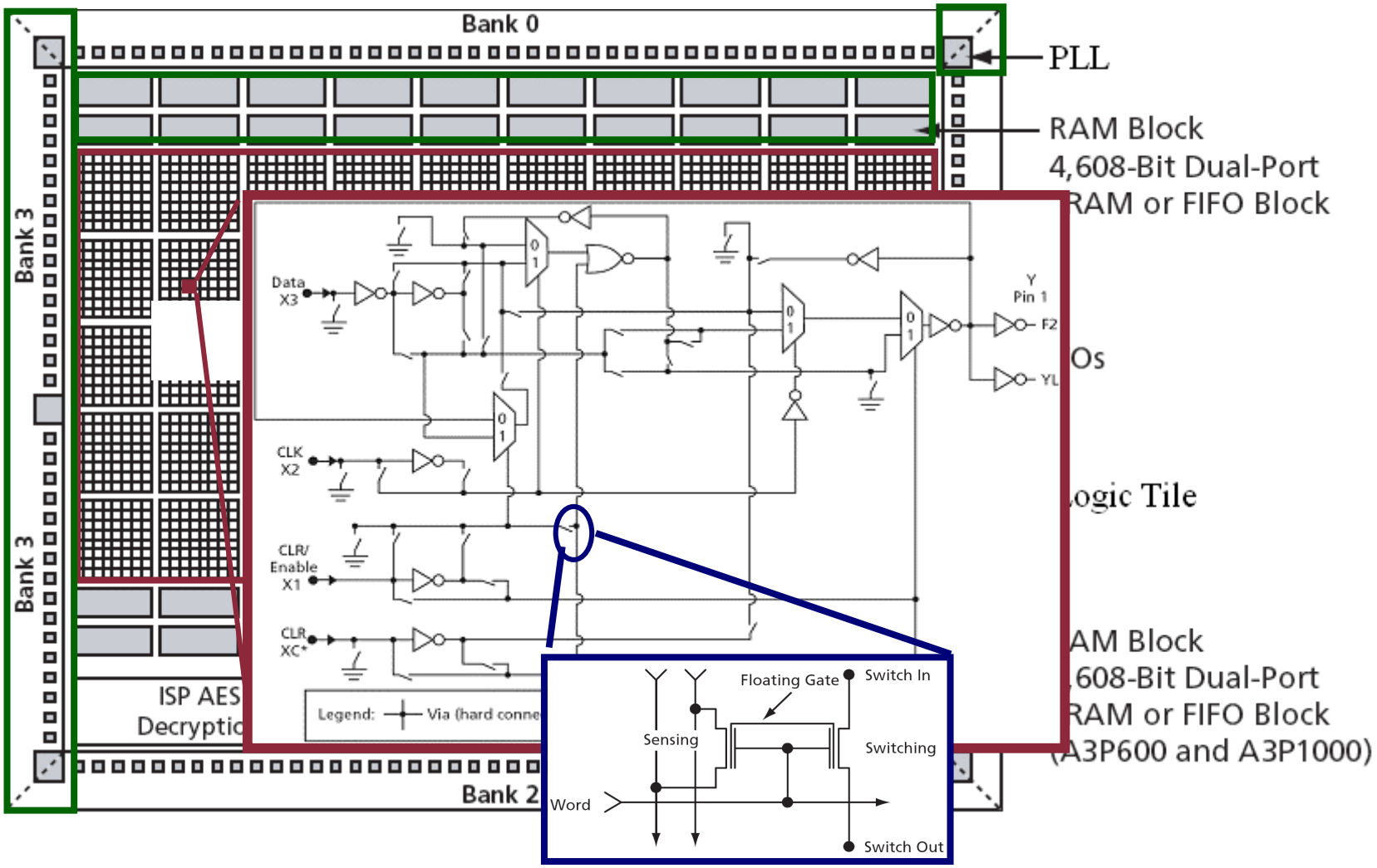
    3. **SEE Mitigation**
3. Low-Power Flash-Based FPGA: IGLOO (AGL)
    1. **FPGA's Features**
    2. **SEE Characterization**
    3. **SEE Mitigation**
4. Summary & Recommendations

Motivations & Objectives

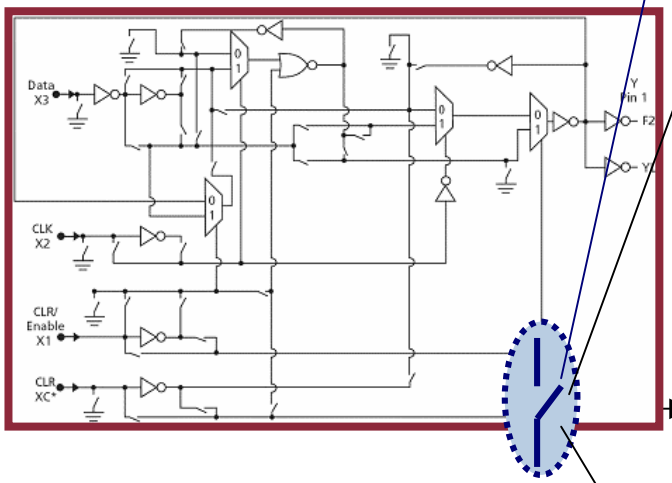
SWITCH	SRAM	FLASH	Antifuse
PROGRAMMABILITY	*Re-programmable (>10^6 times)*	*Re-programmable (1000 times)*	*One time programmable*
VOLATILITY	*Volatile*	*Non-volatile*	*Non-volatile*
POWER CONSUMPTION	*Medium to High*	*Very Low*	*Low*
MANUFACTURABILITY	*Standard CMOS process*	*Standard FLASH process*	*Special Antifuse process*
SEE SENSITIVITY	*Very sensitive to SEE*	*Relatively insensitive to SEE*	*Immune to SEU*

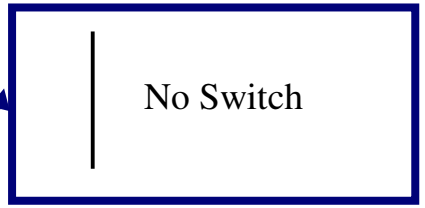
A3P 'ProASIC3' FPGA Features



ASIC and FPGAs

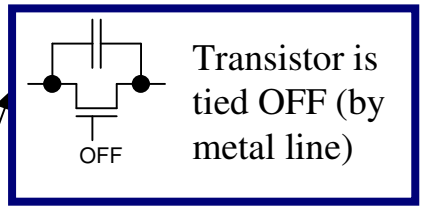
SEE Sensitivities





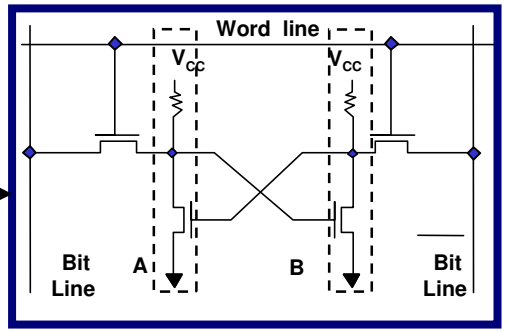
ASIC

CMOS Logic is SET Sensitive



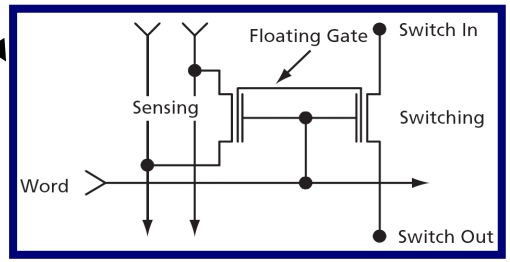
Antifuse: "One Time Programmable ASIC"

CMOS Logic is SET Sensitive



SRAM-Based FPGA: "Volatile Re Programmable ASIC"

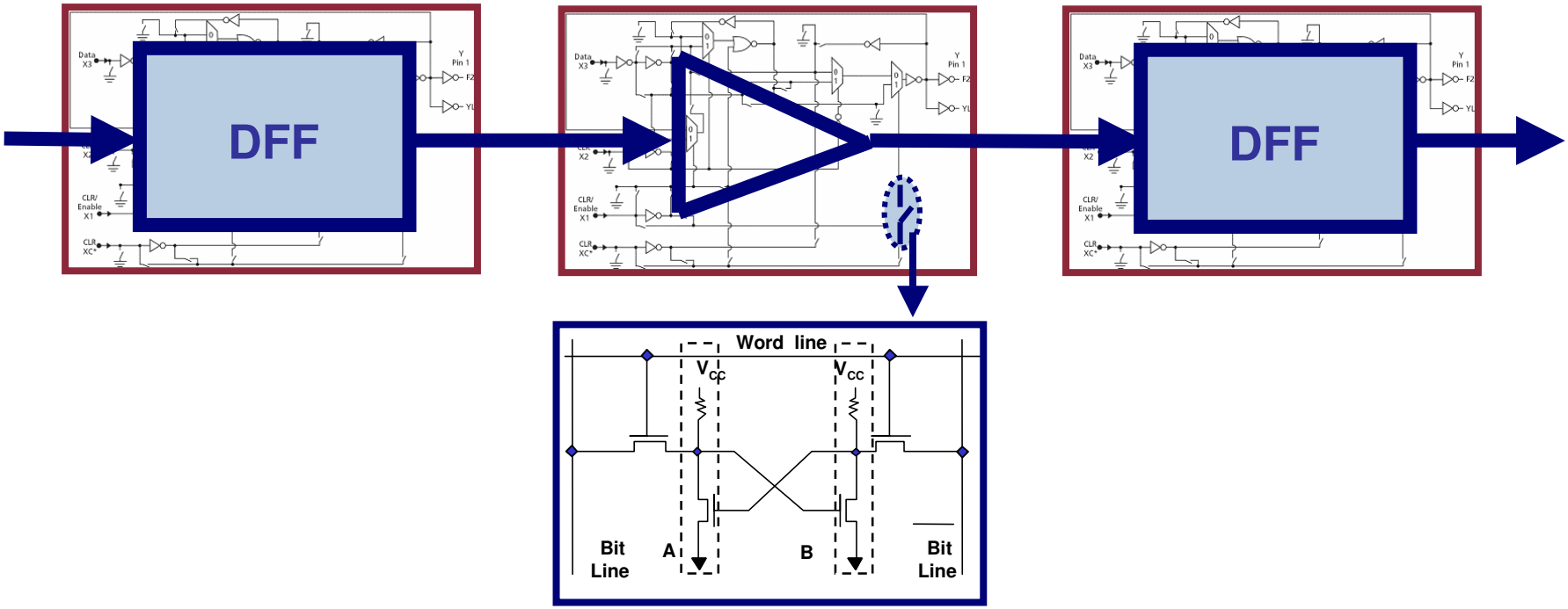
- CMOS Logic is SET Sensitive
- SRAM switches are SEU sensitive



2T Flash-Based FPGA: "Non-Volatile Reprogrammable ASIC"

- CMOS Logic is SET Sensitive
- 2T Flash switches are SET sensitive

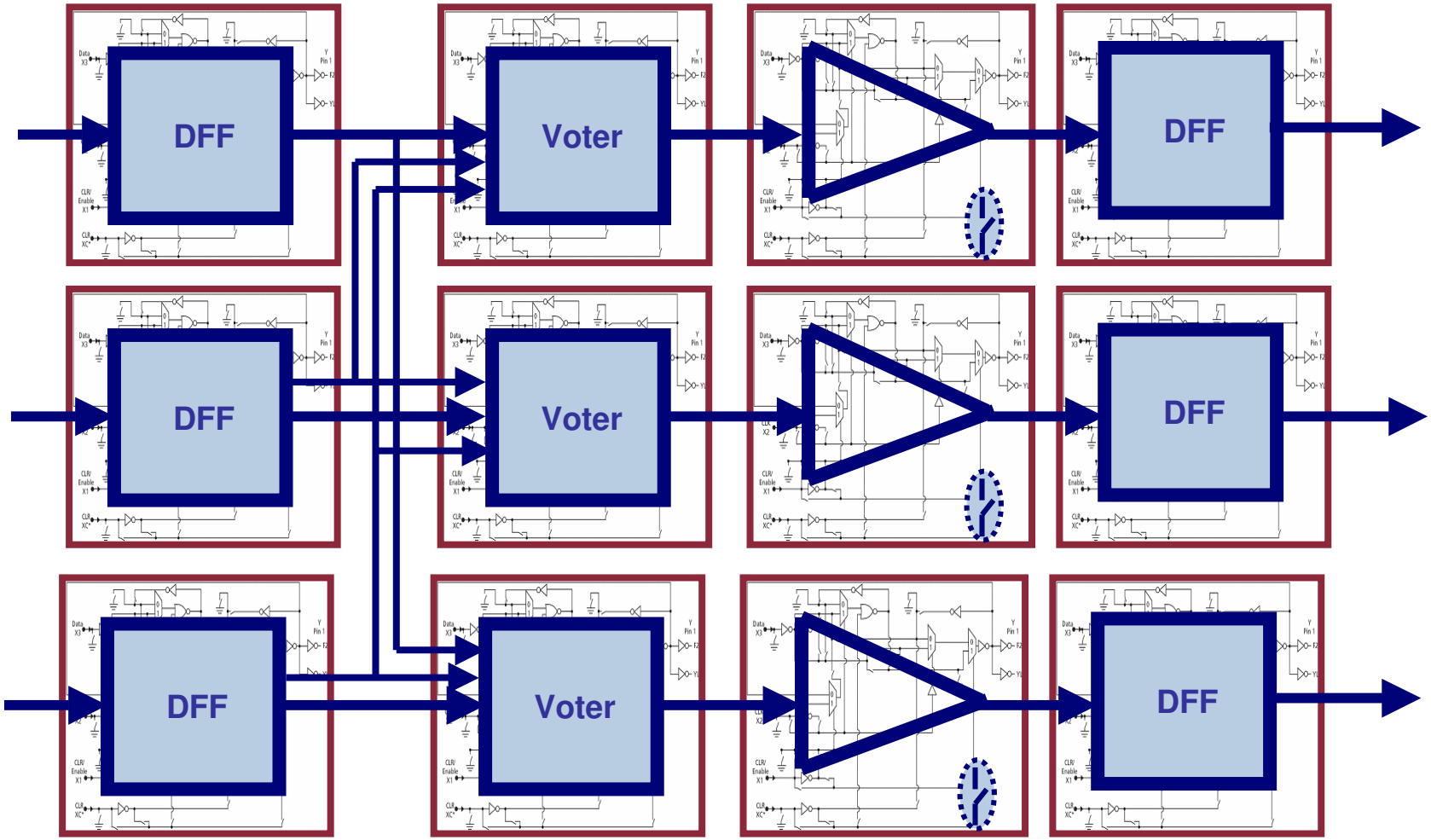
Volatile FPGA



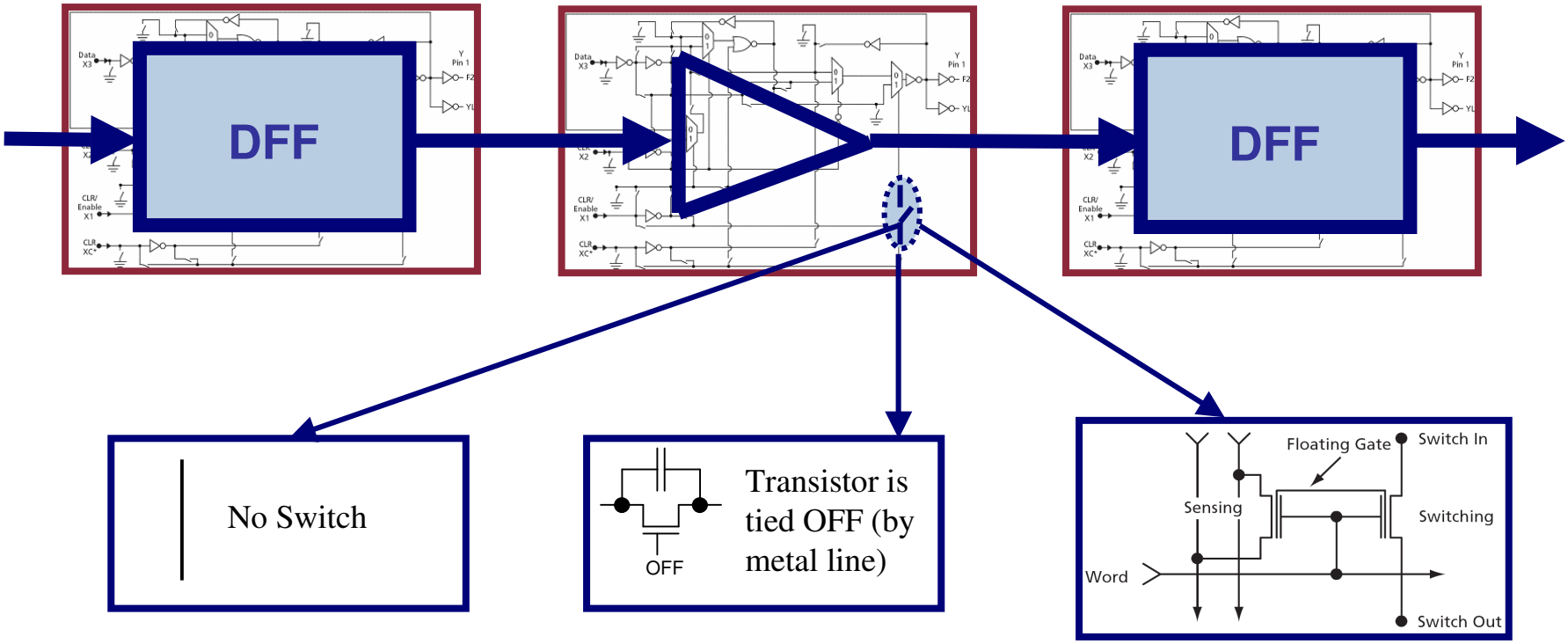
For Volatile FPGA: TMR is required for the Combinational Logic

+ Fast Scrubbing to avoid accumulation of errors

Volatile FPGA

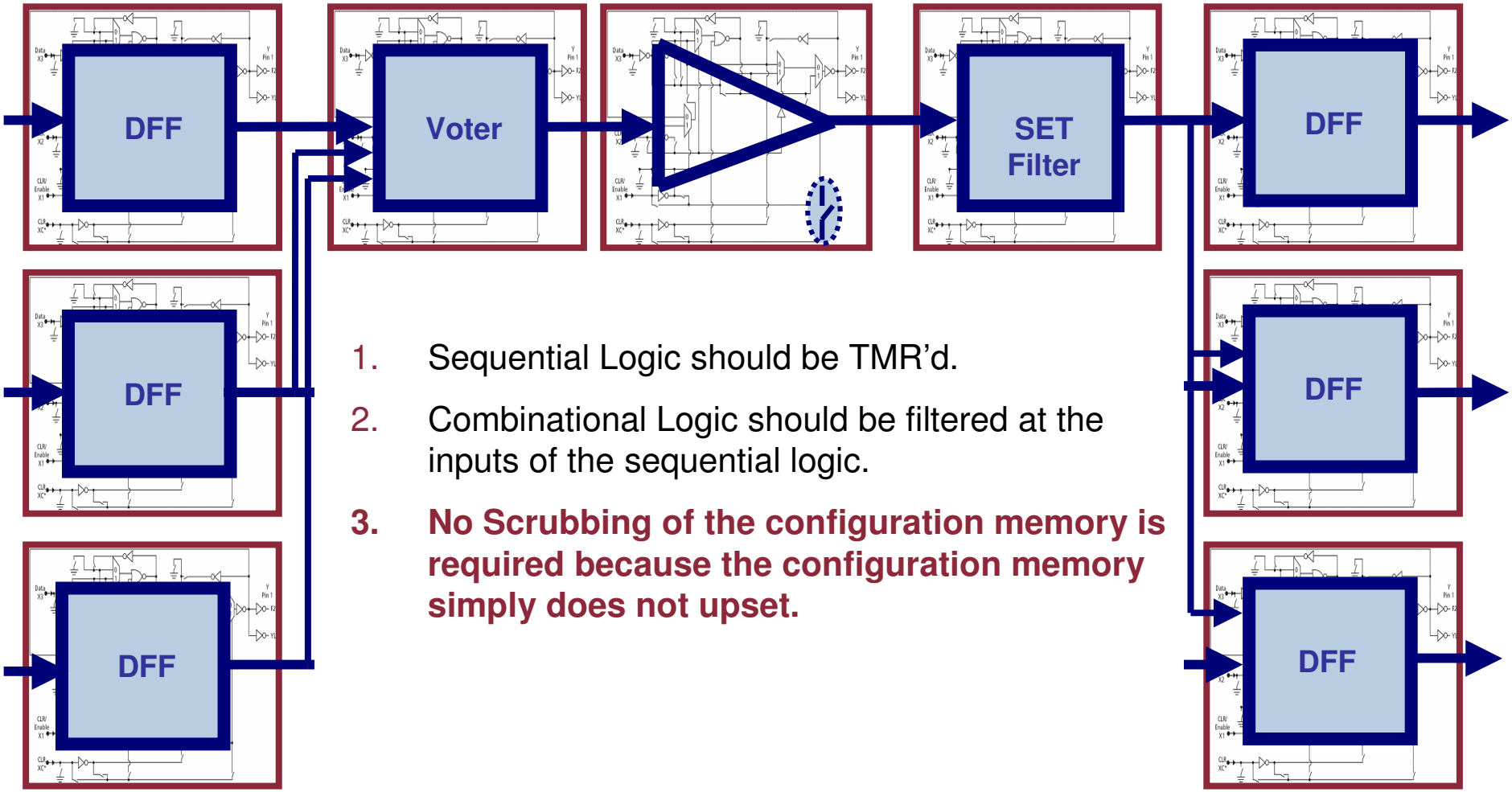


Non-Volatile FPGA



Non-Volatile FPGA: TMR is not required for Combinational Logic or the scrubbing of the configuration memory

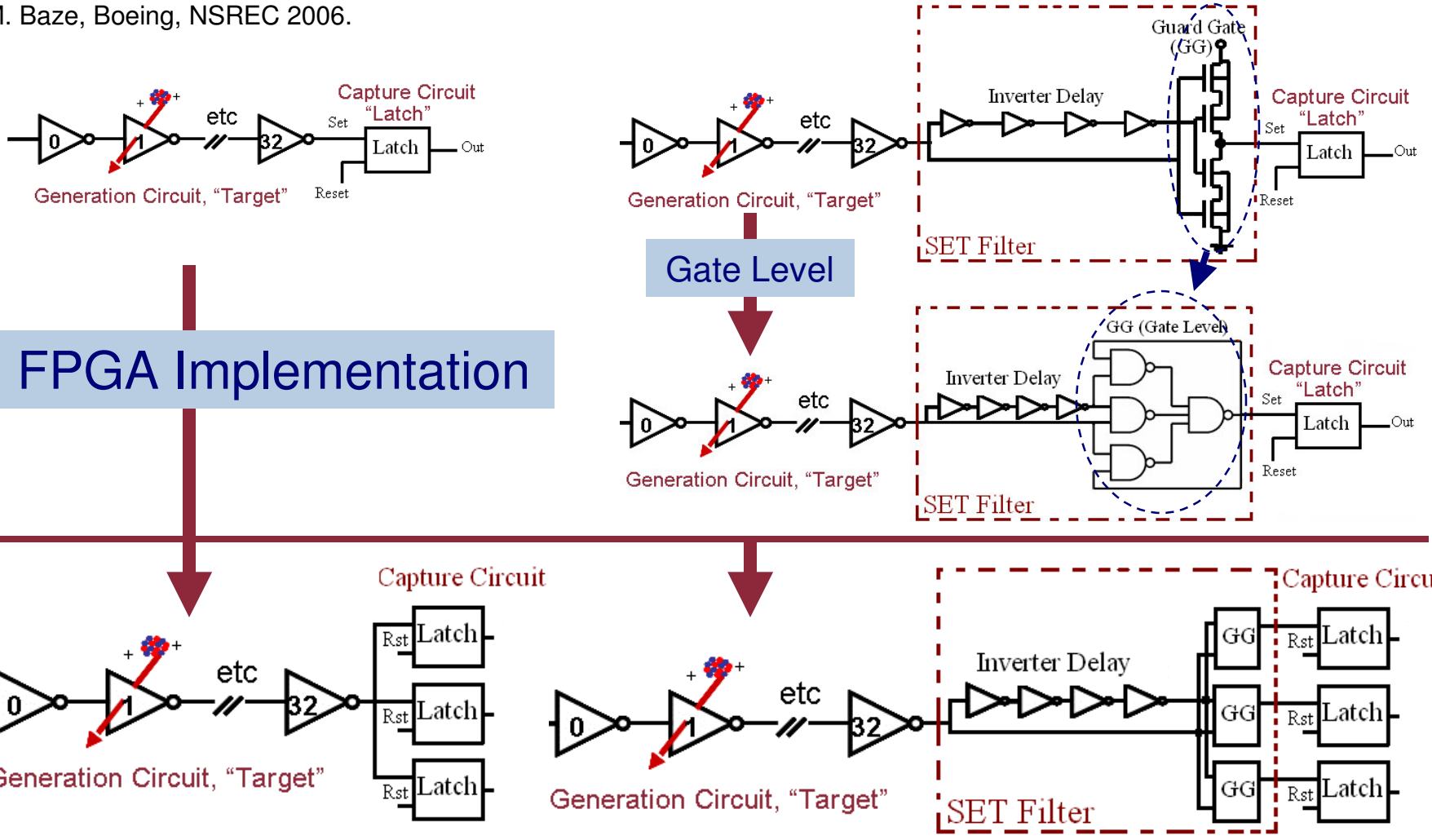
Non-Volatile FPGA



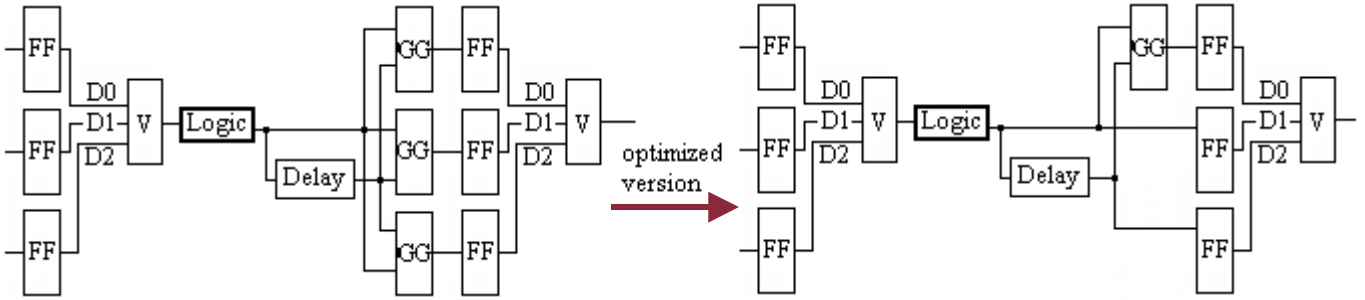
1. Sequential Logic should be TMR'd.
2. Combinational Logic should be filtered at the inputs of the sequential logic.
3. **No Scrubbing of the configuration memory is required because the configuration memory simply does not upset.**

SET Characterization & Mitigation

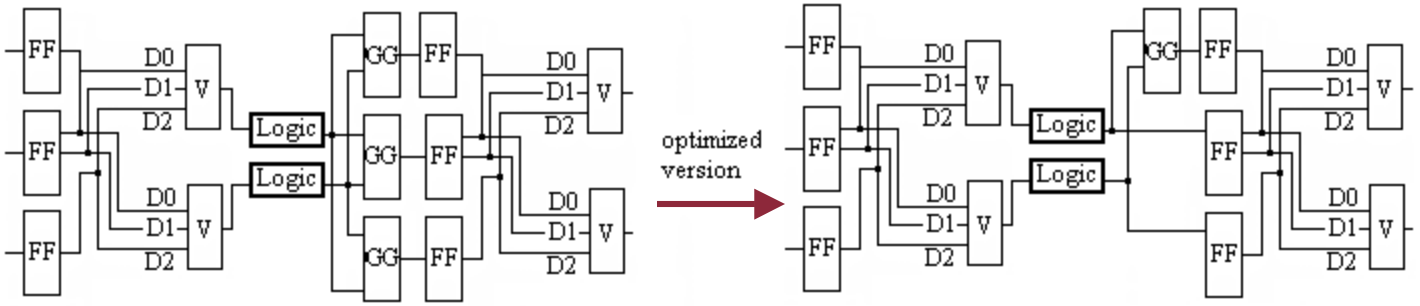
M. Baze, Boeing, NSREC 2006.



Proposed SEE Mitigation Technique

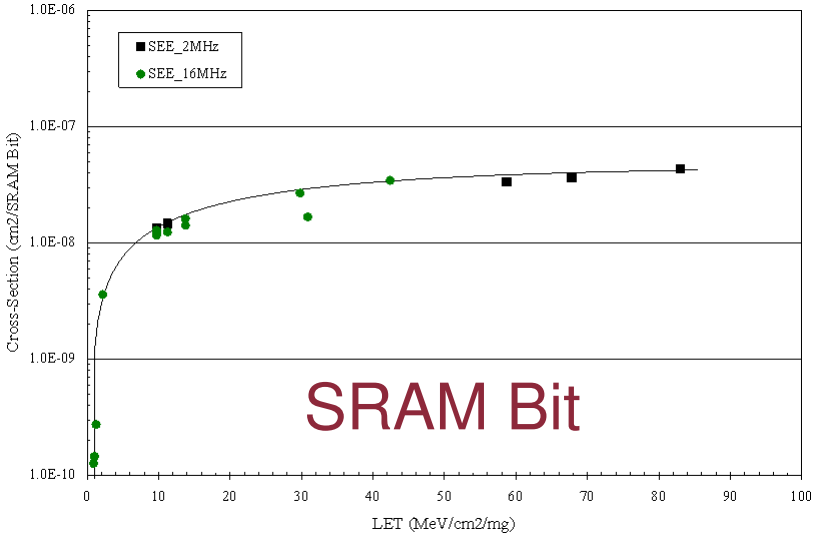


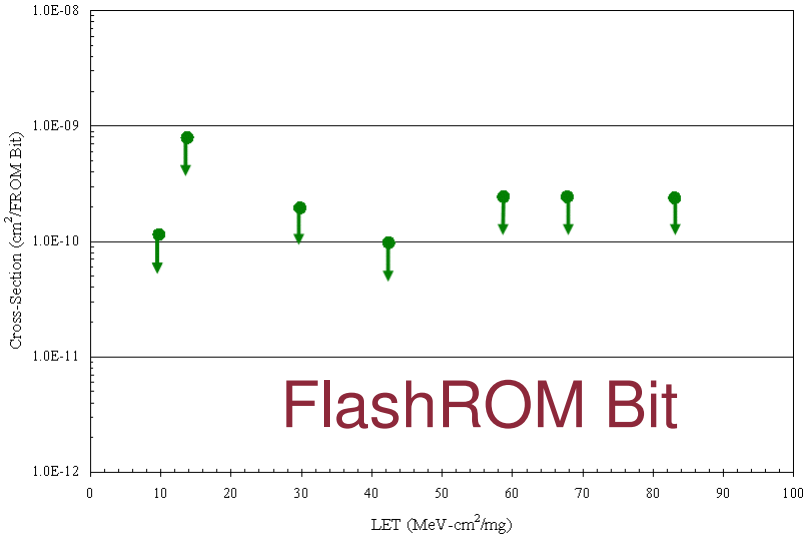
With No Logic Duplication

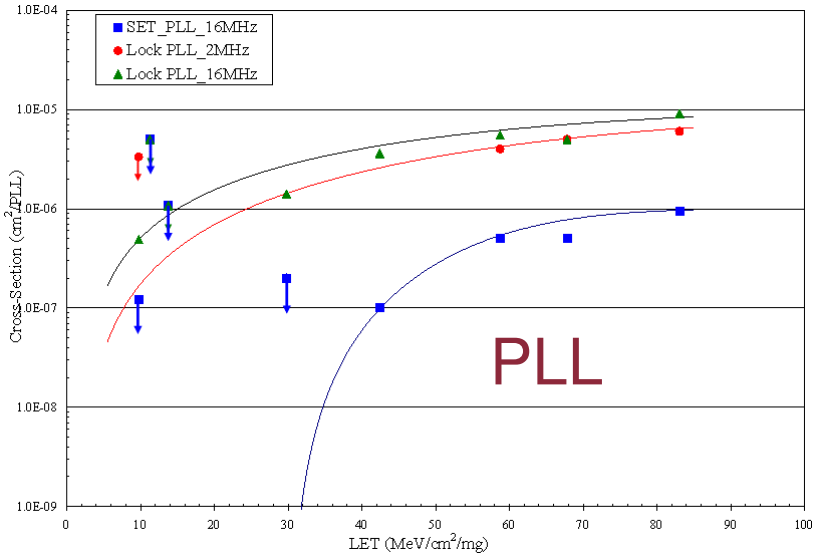


With Logic Duplication

A3P SEE Characterization (1)

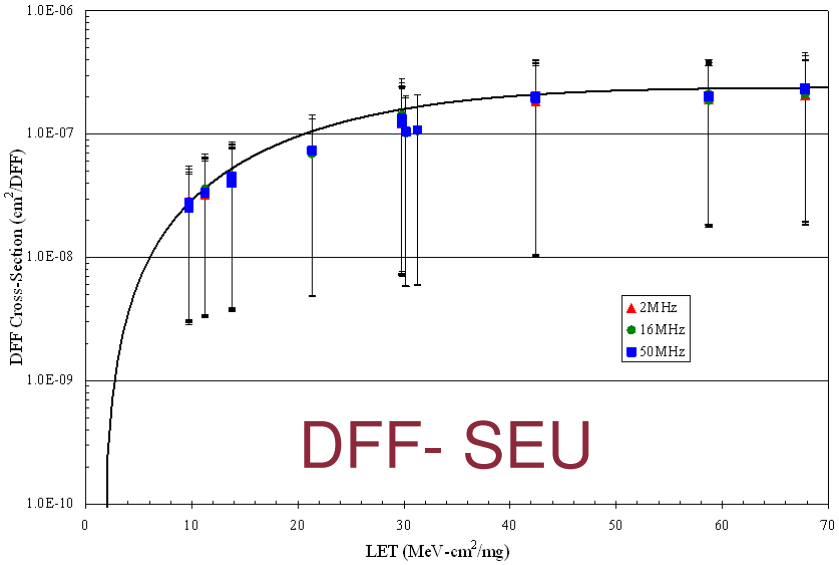




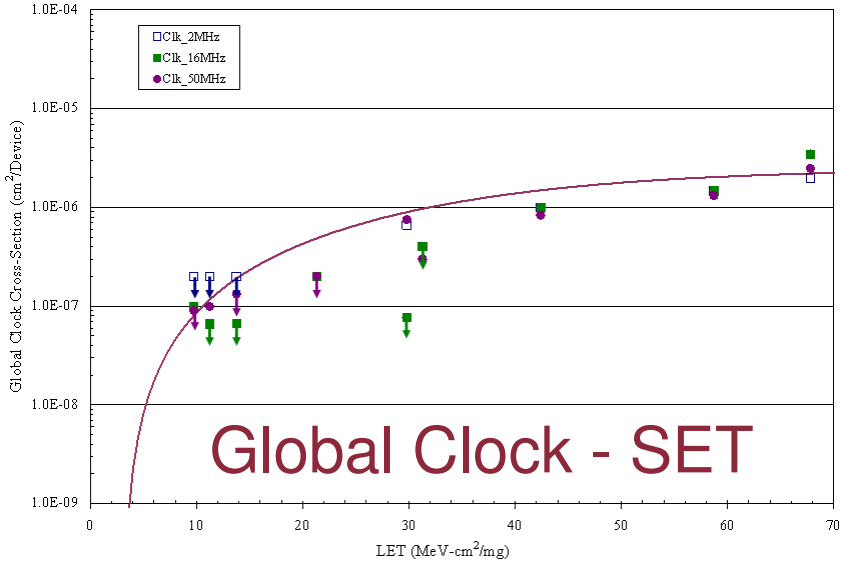


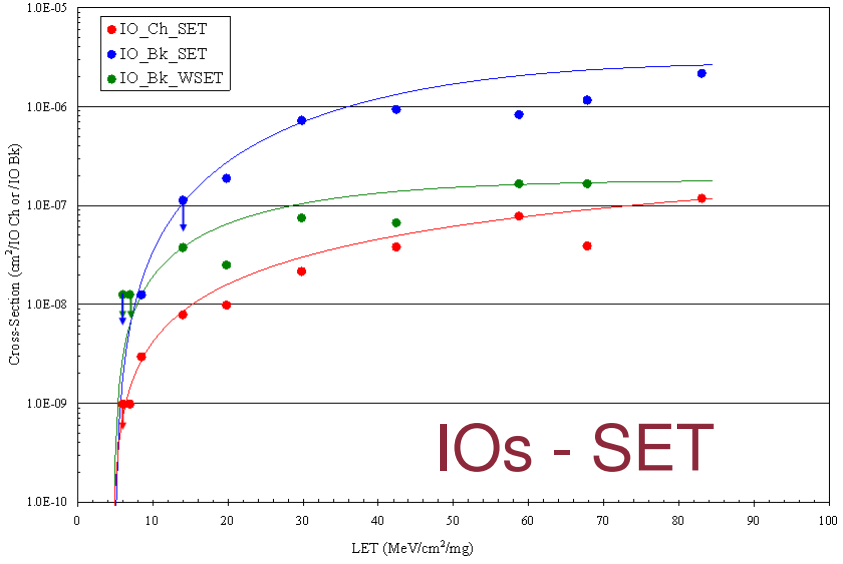
- FlashROM is SEU immune and could be used for boot code for embedded processors.
- SRAM is SEE sensitive but EDAC could be employed for mitigation

A3P SEE Characterization (2)

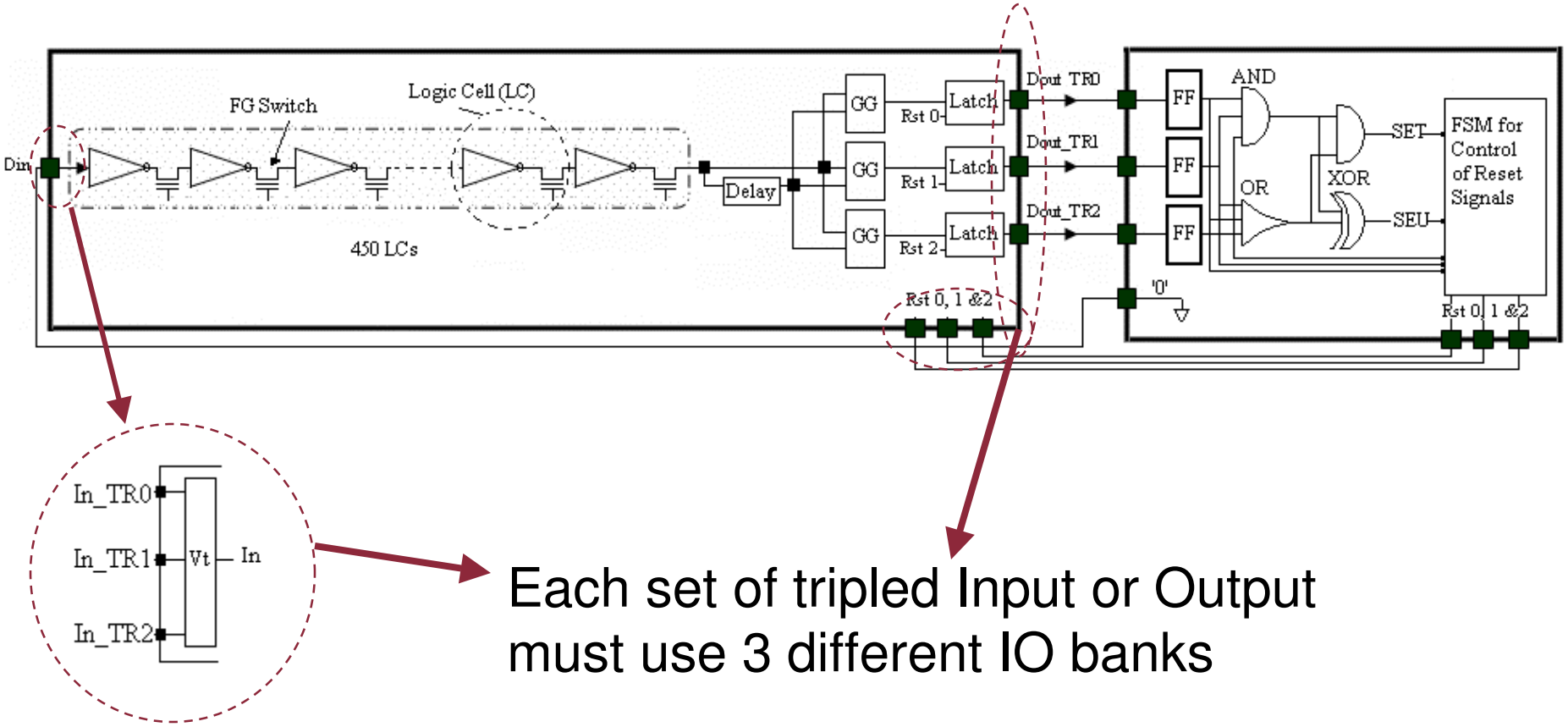


- SEU in DFF can be mitigated by TMR
- At low frequency (2 MHz), no SET was observed on the IOs (including the Clock).
- At 16MHz, SET on the IOs (including the Clock) were seen only at very high LET (68 MeV/cm2/mg).





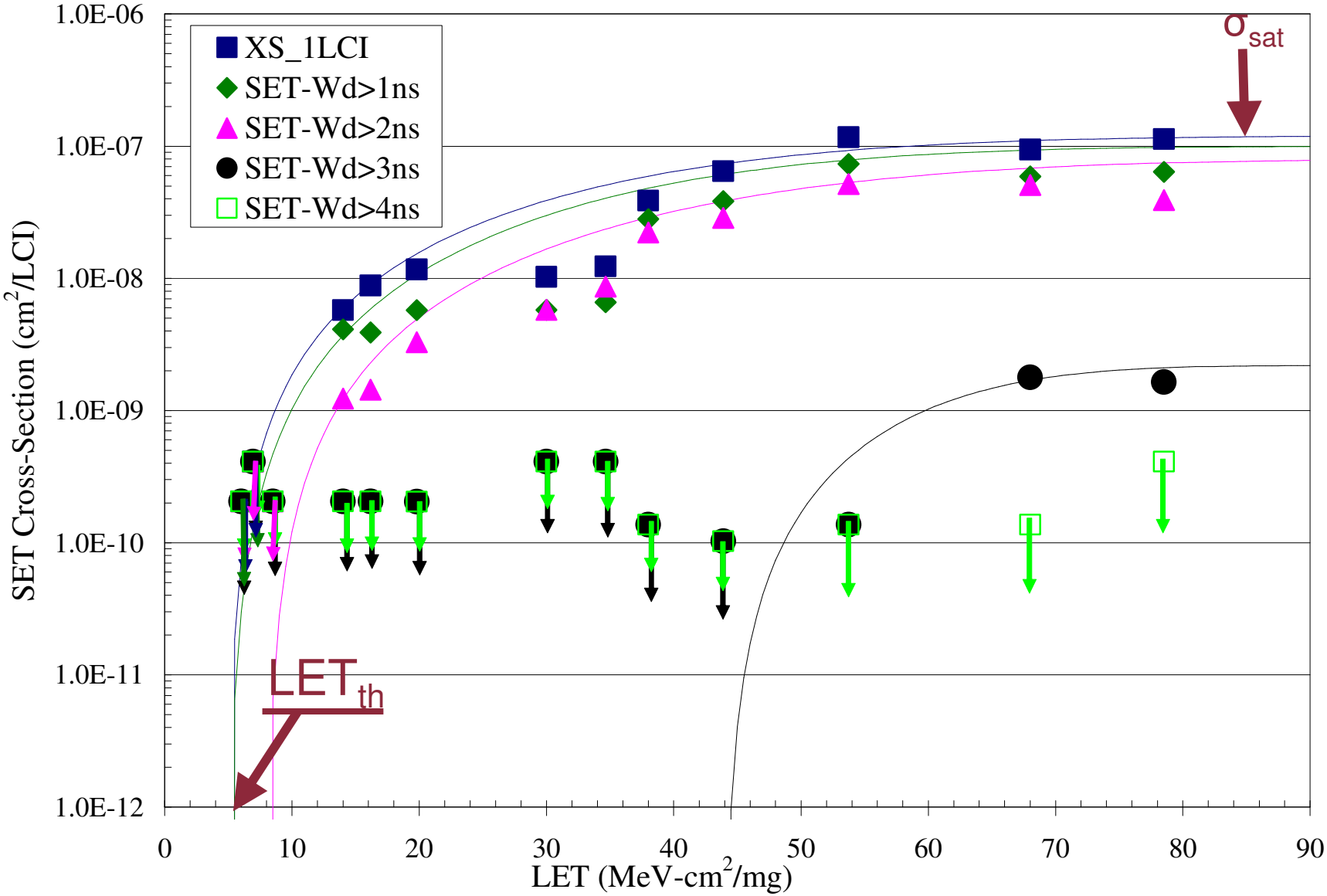
A3P SET Mitigation



Each set of tripled Input or Output must use 3 different IO banks

Design: 486 LCI: So 100 % of logic tiles are used

A3P SET Mitigation



SET/SEU Mitigation on A3P

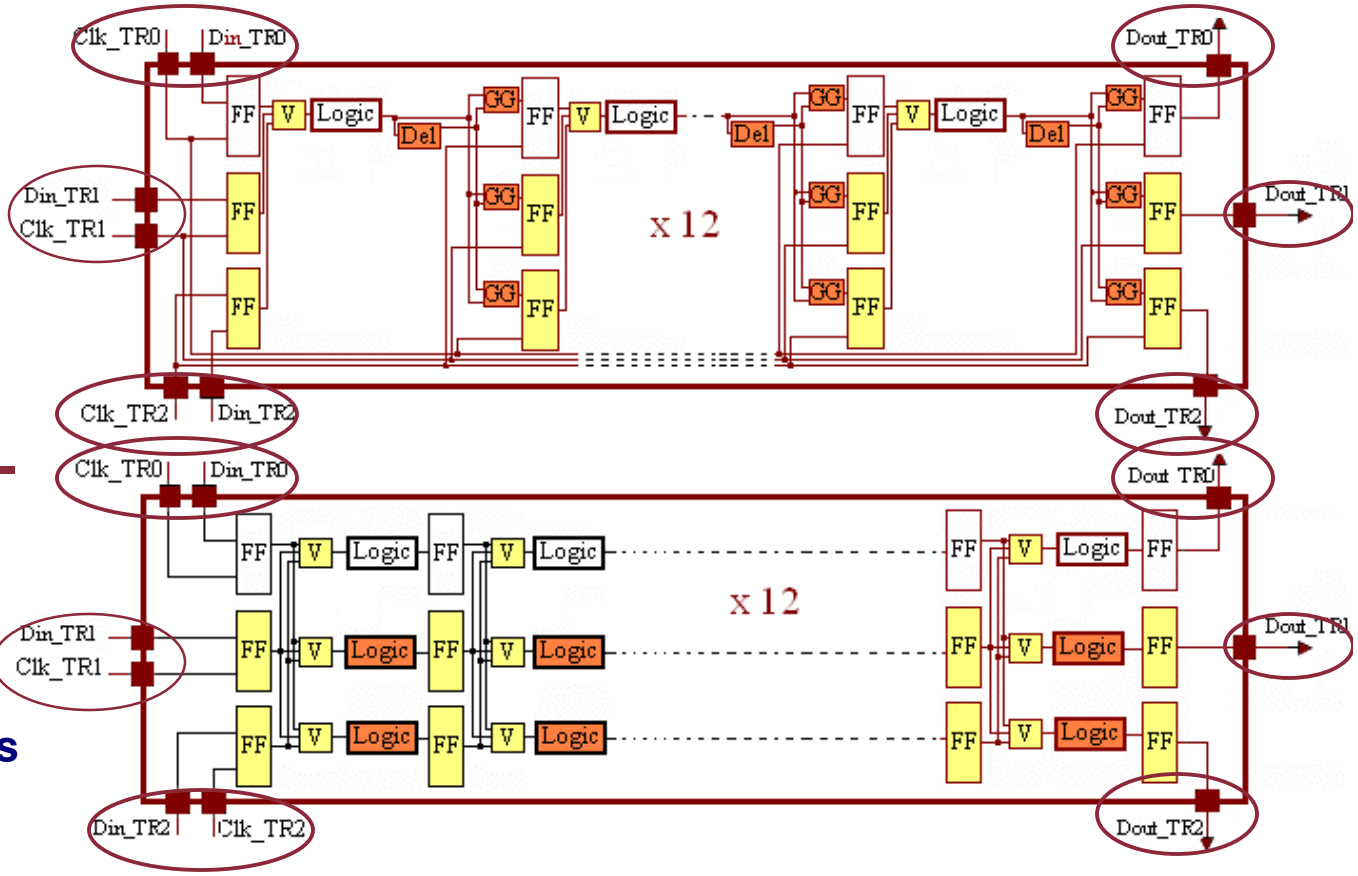
- Partial SEE Mitigation
- Full SEE Mitigation

Without Mitigation of the IO Banks

- **SET Filtering** (Comb. Logic) + TMR (Seq. Logic)
- 75 % of the FPGA Core
- **All IOs are tripled and separated on 3 # IO Banks**

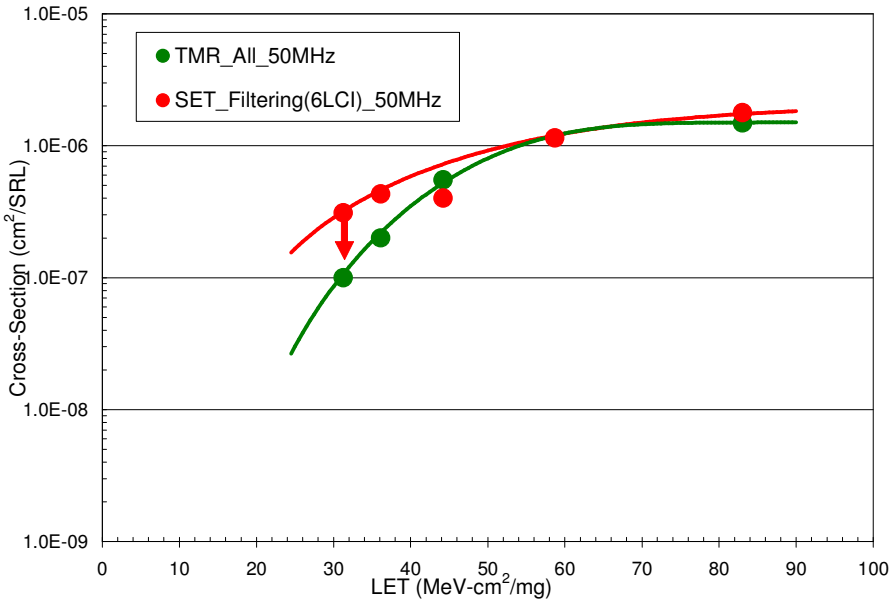
With Mitigation of the IO Banks

- **TMR ALL**
- 85 % of the FPGA Core
- **All IOs are tripled and separated on 3 # IO Banks**



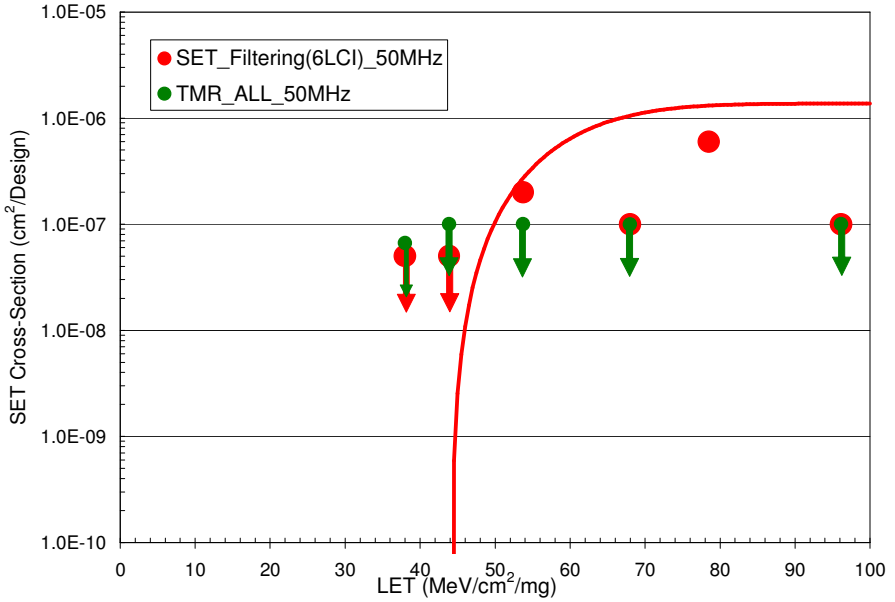
A3P Radiation Test Results

Partial SEE Mitigation



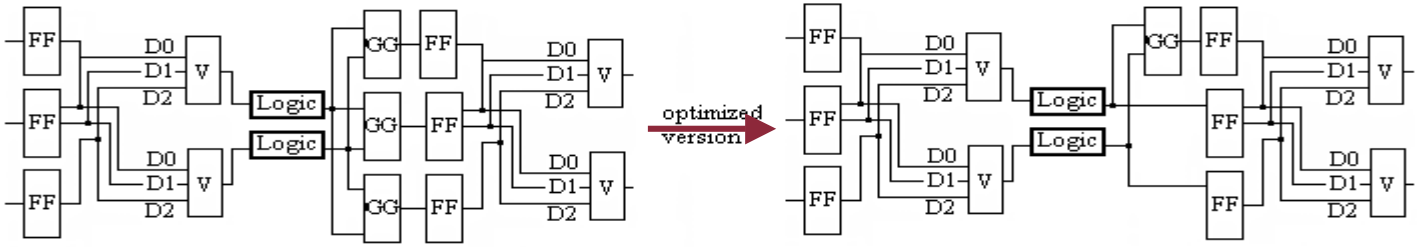
- **TMR-ALL**
  - XS/IO-Bank= 2x 10^{-6}cm²/IO-Bank
  - 10 % time penalty
- **SET Filtering (+ TMR)**
  - XS/IO-Bank= 2x 10^{-6}cm²/IO-Bank
  - XS/IO-Bank= 2x 10^{-7}cm²/IO-Bank if Clock filtered
  - 30 % time penalty

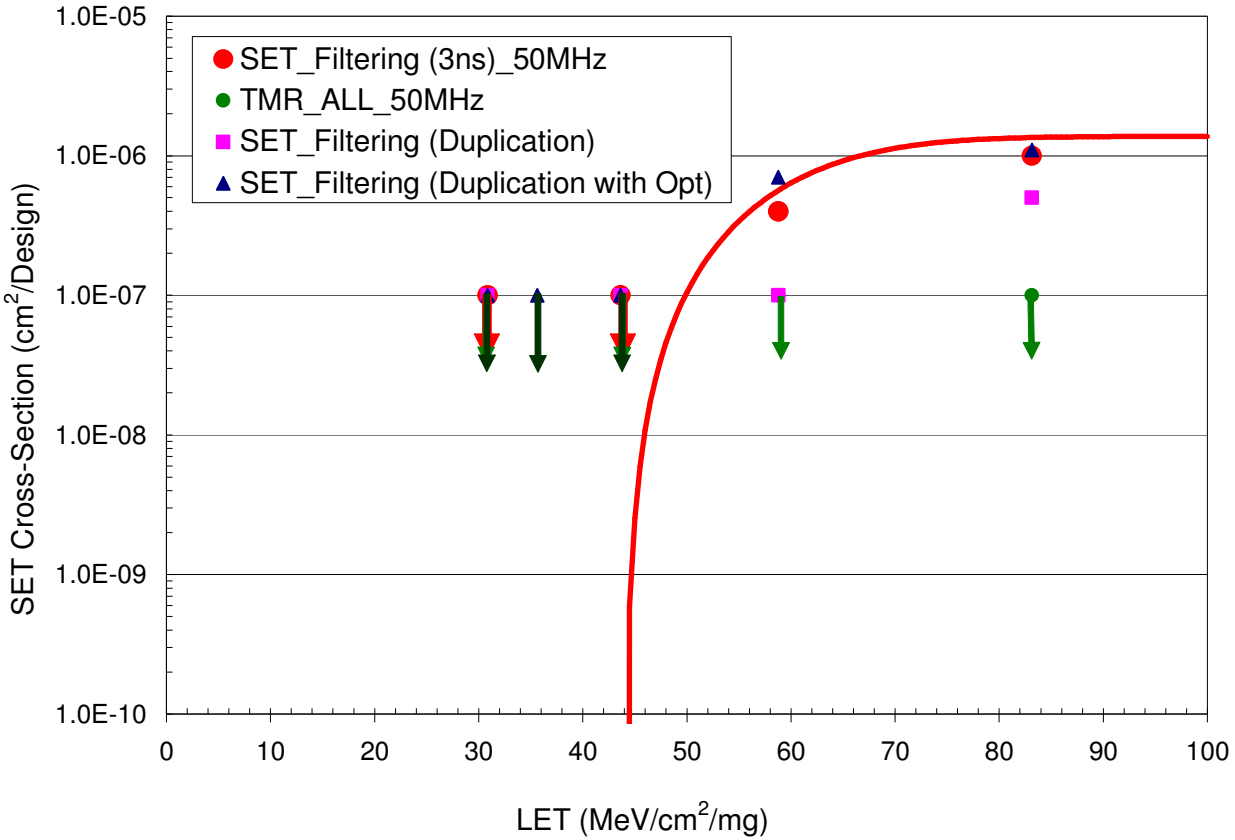
Full SEE Mitigation

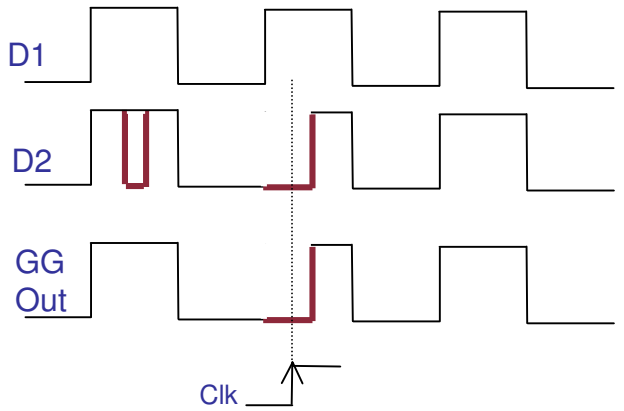


- **TMR-ALL**
  - Full SEE Immunity
  - 10 % time penalty
- **SET Filtering (+ TMR)**
  - *A delay of 6 LCI guarantee SEE immunity for LET < 43 MeV-cm²/mg*
  - 30 % time penalty

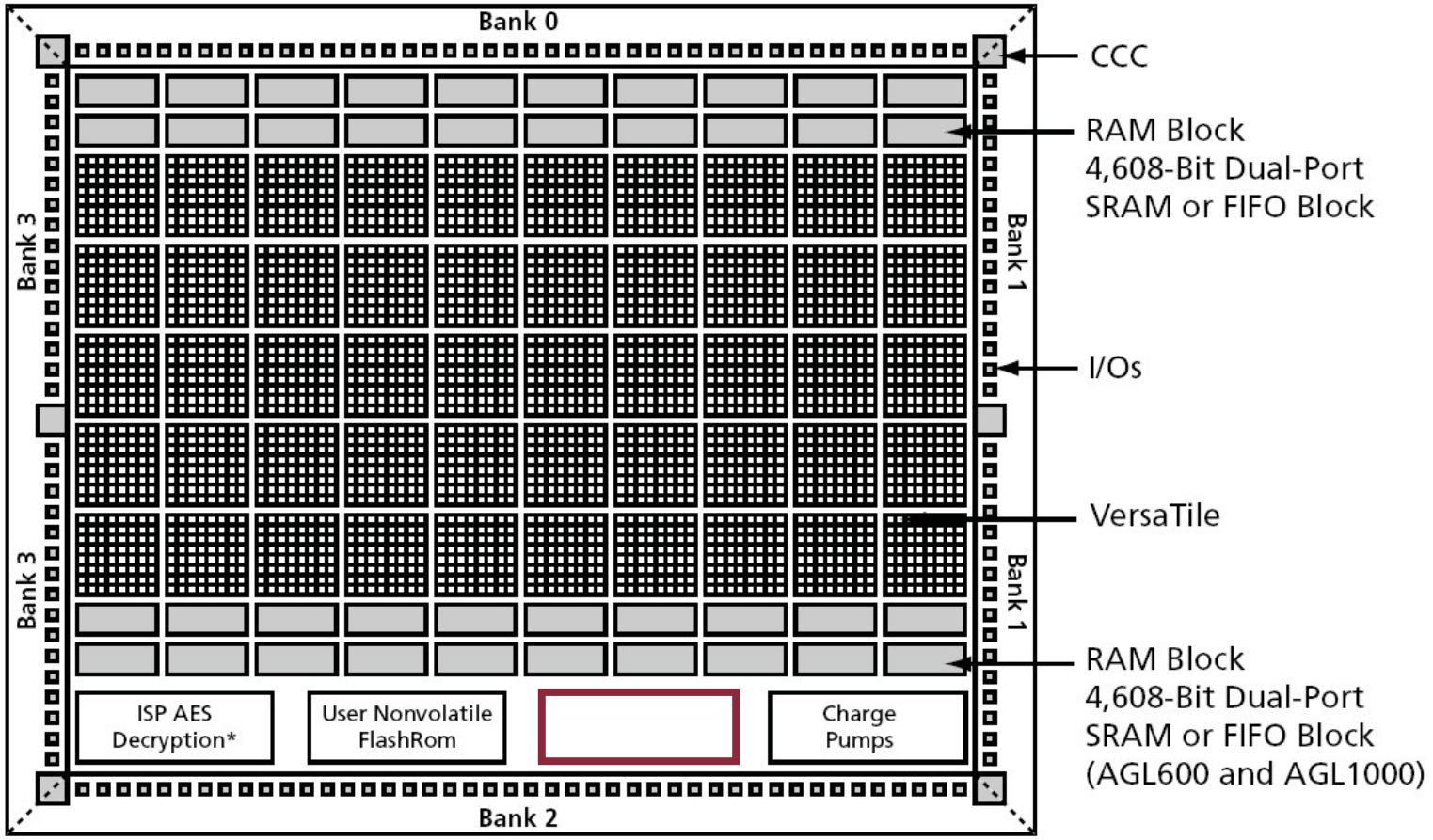
A3P SEE Mitigation With Logic Duplication







AGL 'IGLOO' FPGA Features



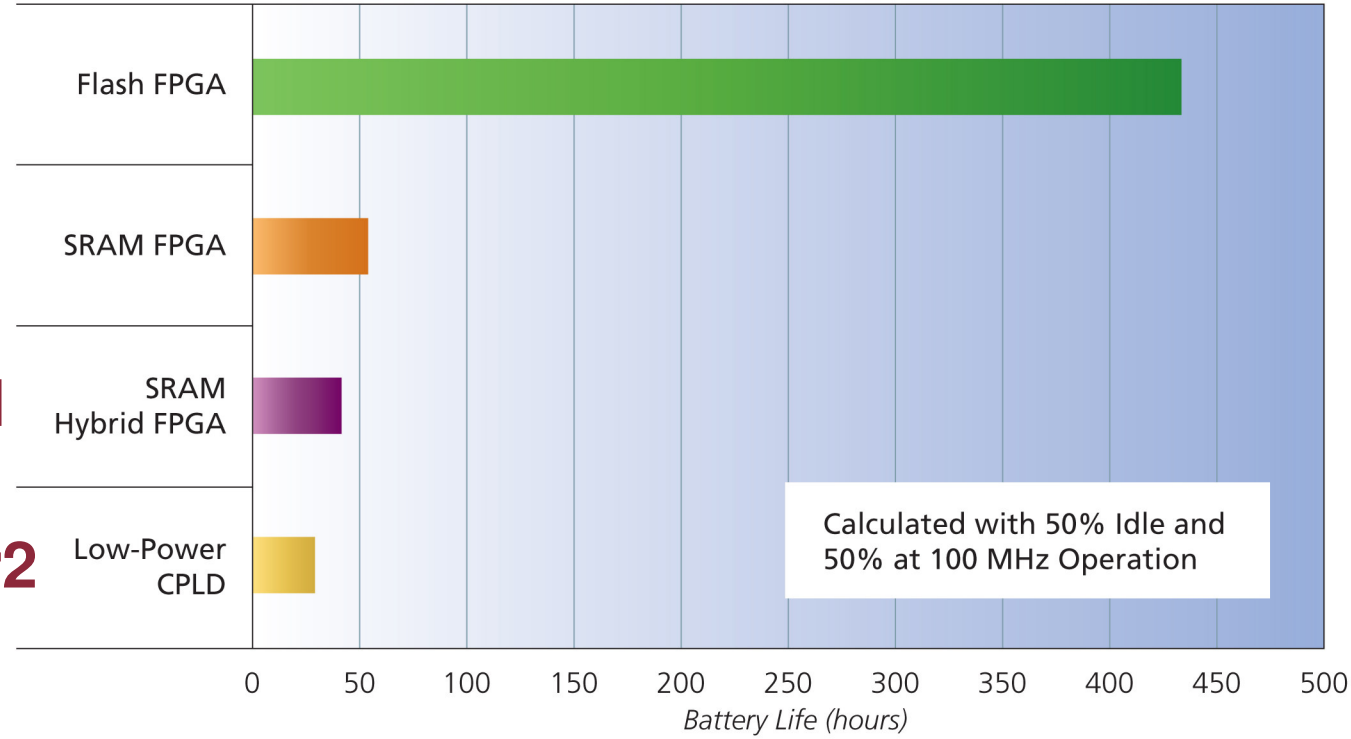
Low-Power FPGA (AGL)

AGL

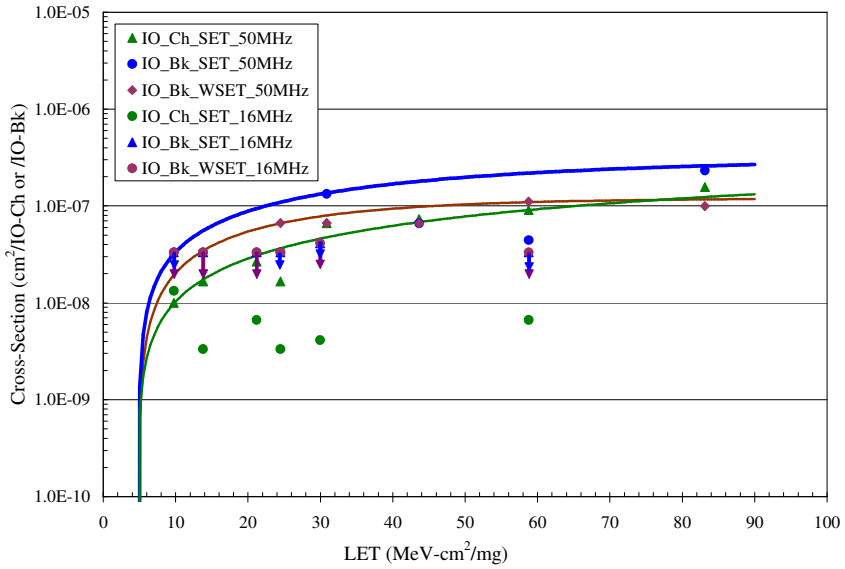
Cyclone3

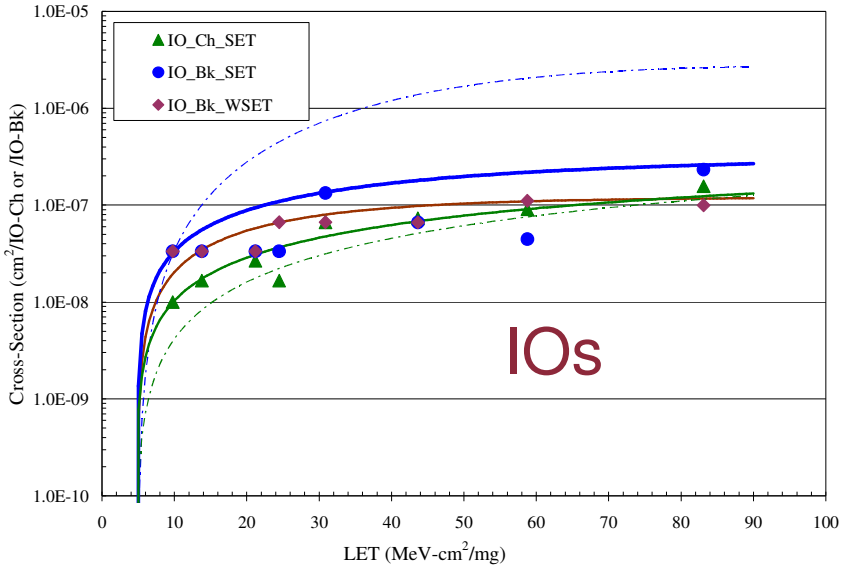
Spartan3AN

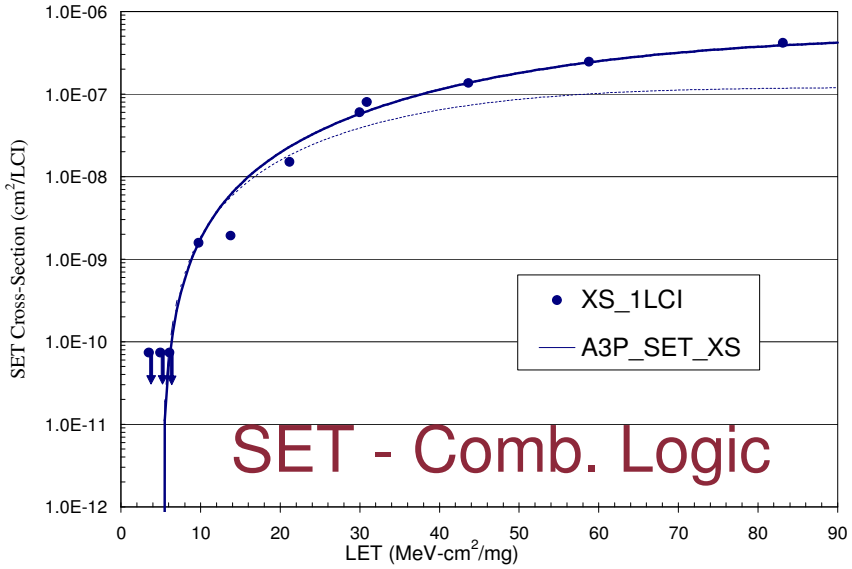
CoolRunner2

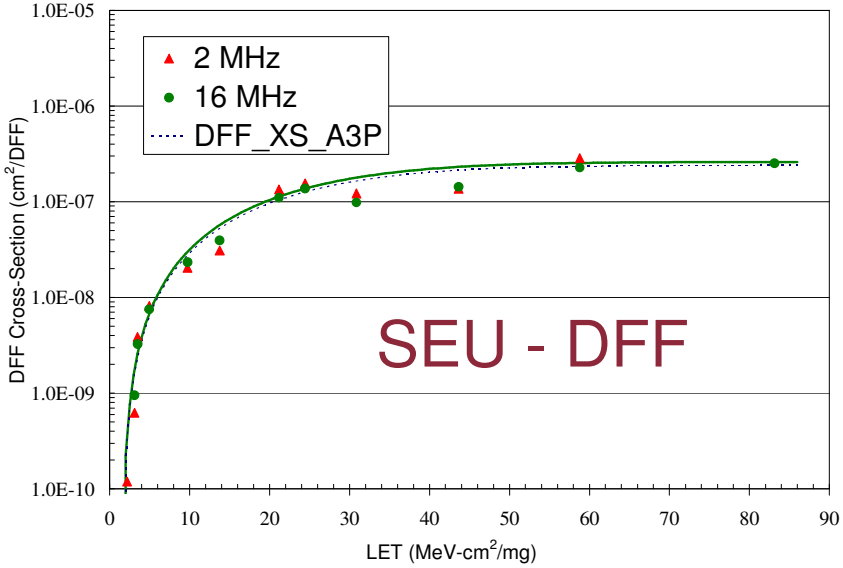


AGL SEE Characterization



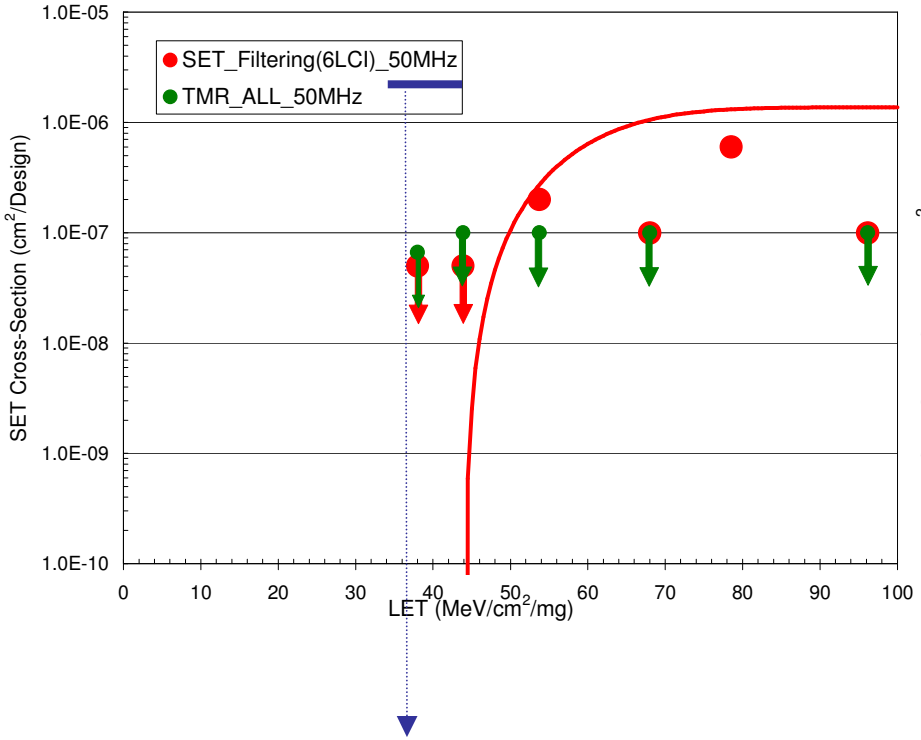






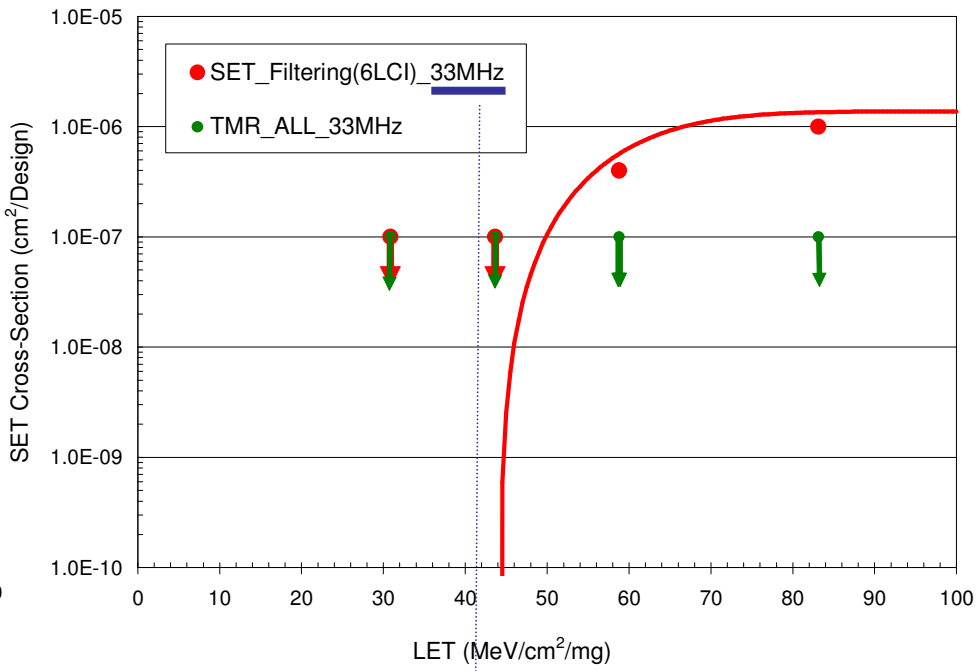
AGL SEE Mitigation

A3P



Faster

AGL



Lower In Power

To Be Done

- SET Characterization (measurements of SET pulse widths)
- SEE Characterization in Freeze Mode

Market Opportunities

Launchers / Missiles	Commercial	Military	International	Civilian / Scientific
Delta IV	Globalstar	MightySat	EnviSat	Deep Space I
Sea Launch	Anik F2	P81 (Classified)	Cluster II	Mars Pathfinder, Surveyor
VLS	Intelsat IX	P59 (Classified)	METOP	Mars MER A and 2, MRO
MinuteMan III	GE-1,2,...8	HESSI	Rosetta	Mars MSL
THAAD	Echostar	Clementine	Champollion	Contours
Pegasus	Telstar	SBIRS	Stentor	Seawinds
Arianne Y				
H-2A				
D5 ENTB				
Patriot				
Atlas II, V				

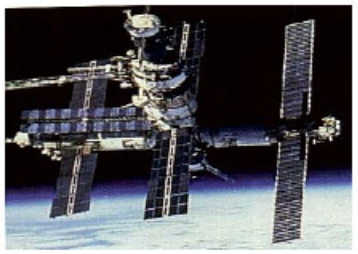
Telecommunications (SDR..)

As long as it meets the TID Requirements

KompSa
Orbcom
PanAmSat

NPP / NPOESS
GPS
MUOS

MDS
N-Star
MTSat
ETS VII
JEM
ADEOS II
OICETS
DRTS



TDRS
Space Shuttle
Hubble Space Telescope
Windsat
GOES
AXAF
TRMM
XTE
ACE
SMEX
MIDEX
GLAS
NEAR
Timed
FUSE
Genesis

Summary & Recommendations

- **Complete SEE Characterization & Mitigation of A3P => RTA3P**
  - **TMR All**
    - Full SEE Immunity
    - 4 times Hardware overhead; 15% time penalty
  - **SET Filtering (combinational logic) + TMR (sequential logic)**
    - A delay of 6 LCI guarantee SEE immunity for LET < 43 MeV-cm^2/mg
      - *30 % time penalty*
    - A delay of 8 LCI guarantee Full SEE immunity for LET < 96 MeV-cm^2/mg
      - *40 % time penalty*
    - Logic Duplication guarantee SEE immunity for LET < 43 MeV-cm^2/mg
      - *10 % time penalty*
  - **Embedded Systems Applications: Processors (8051, ARM, FT-Leon3, DSP…)**
  - **Flight Parts should be available in 2009**
- **AGL: Lowest Power FPGA**
  - **SEE Characterization & Mitigation**
  - **Results show the same radiation sensitivity as for the A3P**
  - **TBD: SEE Characterization in Freeze Mode**