Reconfigurable, High Density, Gigahertz Speed Low Power Radiation Hardened FPGA Technology

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27- 29 November 2007
BAE/Achronix RH FPGA Program

- Background
- Introduction
  - Achronix Company
  - Achronix FPGA Overview
- BAE/Achronix Radiation Hardened Test Chip Data
- BAE/Achronix RH FPGA Program Overview
  - Product Features
  - Product Development Strategy
- Summary
**RH FPGA Roadmap**

**Legacy ONO Antifuse Based RH FPGA**
- 5V Legacy Product: *Actel* RH1020 and RH1280 FPGA’s
- Production stopped in 2002; Build-out Inventory - exhausted
- Significant product demand continues
- **Actions being taken:** Re-install FPGA process into recently modernized foundry; Restart production.

**Next Generation M2M Antifuse Based RH FPGA**
- *Actel* RTAX FPGA’s are being used in space missions
- Rad Hard (RHAX) FPGA’s are better suited for certain missions
- **Actions being taken:** Migrate RTAX FPGA designs to RH foundry to build RHAX FPGA equivalents; Start flight-qualified production.

**Reconfigurable Reprogrammable RH FPGA**
- Critical need exists for re-configurable/ re-programmable, rad hard FPGA’s
- **Actions being taken:** Develop & demonstrate Multi-million gate RH FPGA using *Achronix* fabric built on radiation hardened process/designs.
Background

Program History
- Investigated Achronix Base Technology Starting in 2006
- Test chips fabricated & successfully tested for SEU in 2007
- BAE/Achronix Joint Development Program started under government funding in 2007

Program Goal
- Develop a SRAM based Multimillion Gate Reconfigurable Radiation Hardened FPGA based on Achronix architecture using BAE’s Radiation Hardened Process Technology
Introduction

Achronix Company Overview

- Well funded, privately held fabless semiconductor company
- Founded in New York in 2004
- Headquarters moved to San Jose in 2006, retained New York R&D lab
- Working 90nm and 180nm prototype silicon
- Series of Patents protect key IP
- Partnerships with Major Fabs, IP and EDA vendors
Achronix Commercial FPGAs

- Standard SRAM-based FPGA fabric
- Embedded multipliers and memory blocks
- Pipelined implementation for high frequency operation (> 1 GHz)
  - Pipelining is transparent to designers
    - Designers write standard VHDL/Verilog
- Industry-standard I/Os
Achronix FPGA Architecture

**Familiar Silicon & Familiar Tools**

**Familiar Silicon**
- Traditional 4-input LUT architecture
  - With GHz performance
- SRAM-based reprogrammable FPGA
- Requires no knowledge of underlying technology

**Familiar Tools**
- SYNP Synplify-Pro and Mentor Precision Synthesis Flows
- Full compatibility with existing third party simulation, debug, and verification tools
Achronix FPGA History

- 180 nm prototype (Sep 2005)
  - 674 MHz
  - World’s fastest CMOS FPGA by 2x

- 90 nm prototype (Apr 2006)
  - 1.93 GHz
  - World’s fastest CMOS FPGA by 5x
Achronix patented Redundancy Voting Circuits (RVC) SEU mitigation

- Redundancy Voting Circuits (RVC)
  - Two copies of all circuits implemented
  - Copies are non-adjacent avoiding the risk of a single upset affecting both
  - Every stage (combinatorial and state) has local voting mechanism

- Local voting waits until both copies agree
  - no SEU, no delay
  - If SEU on either, circuit resolves to the correct value after event energy dissipates
BAE/Achronix RH FPGA Test Chip
**RHFPGA Test Site**

**BAE-Achronix 54 mm² RADHARD FPGA**
- Low density design,
- 27K gate, 250 MHz,
- reconfigurable

**BAE-Achronix 9 mm² RADHARD FPGA with BAE hard SRAM cells**
- Low density design,
- 4K gates, 250 MHz
- reconfigurable

**BAE-Achronix 9 mm² RADHARD FPGA with Achronix hard SRAM cells**
- Low density design,
- 4K gates, 250 MHz
- reconfigurable
BAE-Achronix 3x3 RADHARD Testsite
Design SPICE results predicted 275 MHZ – We averaged 289.3 MHz
Test Site Performance and Power Summary

Speed Test Results (Running Program) - Serial#BAE-A9

Core Power Test Results (Running Program) - Serial#BAE-A9
Radiation Test Overview

- The Test Chip contained a 4x4 array of FPGA Tiles implemented with RVC

- One dedicated tile had an 8 bit counter (implemented in RVC) on output acknowledge to observe the functioning of the various FPGA configurations at a reasonable frequency with standard I/O

- Five different FPGA patterns were utilized during testing running at different frequencies (37 MHz to 290MHz)
SEU Test Summary

- Testing completed at Texas A&M Cyclotron with Argon (0°), Krypton (0° and 45°), and Xenon (45°) did not cause any of the 5 patterns to lock-up or fail.

- No observed SET or SEU events in SEE testing up to an effective LET threshold of 58 MeV-cm²/mg.

- This testing validates that the Achronix Redundancy Voting Circuits (RVC) are achieving the intended goals.
BAE/Achronix RH FPGA Product
RH FPGA Product Approach

BAE RH15 Radiation Hardened Technology

Reconfigurable Radiation Hardened FPGA

Achronix FPGA Architecture

- RH15 Radiation Hardened Process
- RH15 RH SRAM
  - Configuration Memory
  - Block RAM (BRAM)
  - Registers
- Synchronous Frame
- ESD resistant Programmable I/Os
- PLL

- FPGA Fabric
  - Reconfigurable Logic Blocks
  - Redundancy Voting Circuits
  - Block RAM Wrapper
  - Multipliers
  - Routing Resources
  - Synchronous/Asynchronous Wrapper
RH15 Density Capabilities

16M SRAM Chip Statistics

- > 113 Million Transistors; > 1 Billion Inter-Level Connects; 176 meters of Resistor
- 16M SRAM is the highest density part built in Manassas
RH15 Performance Capabilities

High Speed Circuit Testing to measure on-chip gate delay.

Logic Representation of High Speed Signal Paths

PDV3 Chiplet-1 Operation-Frequency versus Gamma-Dose
[Vcore=Vdd+10%]

Results confirm >1GHz performance both pre- and post-irradiation (2 Mrd(SiO_2))

No change in Iddq with dose.
RHIFPGA Features

- Reconfigurable Radiation Hardened FPGA for military, aerospace and industrial applications
- Leverages standard RTL: Eliminates need for TMR design & tools
- High Performance FPGA (Up to 350 MHz)
- Total Dose Hardness through $1 \times 10^6$ rad(Si)
- Single Event Error Rate of $< 1 \times 10^{-11}$ upsets/bit day
- Operating Temperature
  - -55°C to 125°C (Ambient)
  - Extendable to Extreme Temperatures
- Independently Configurable IO (PCI Compatible)
  - Low Voltage TTL/CMOS
  - LVDS
  - SSTL, HSTL
- Existing FPGA EDA Tool Support (Synplicity & Mentor)
RHFGA Product Development Strategy

- Implement design using BAE Systems Radiation Hardened Process Technology Features

- On-chip memory structures
  - Replace Standard SRAM with BAE Systems RADHARD SRAM

- Circuit methodology
  - Use Achronix Redundancy Voting Circuit (RVC) and self-correction capability to actively correct upsets and transients

- Space apart critical nodes to reduce double-error probability
ACX RH FPGA Program Overview

Achronix:
⇒ Product Design
⇒ Architecture Definition
⇒ Reprogrammable Fabric
⇒ Incorporate BAE RHSRAM
⇒ Final Design & Simulation
⇒ Product Testing Support
⇒ Sales/Marketing

BAE:
⇒ Design S-Frame, BRAM, IO, PLL
⇒ Integrate Design
⇒ Wafer Processing/Characterization
⇒ Wafer Sort and Packaging Tests
⇒ Packaging
⇒ Radiation Testing

Product design 09/08

Fab at BAE in RH15 Process 03/09

Package & Test 05/09

POC Ready 3Q09
Start Qualification Option

Radiation Test 07/09
# RH15 CMOS Technology Features

## Radiation Hardness Assurance Levels

<table>
<thead>
<tr>
<th>Environment</th>
<th>RH15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dose (rad(Si))</td>
<td>1M</td>
</tr>
<tr>
<td>SEU (errors/bit-day)</td>
<td>1E-11</td>
</tr>
<tr>
<td>SEL (MeV-cm2/mg)</td>
<td>120</td>
</tr>
<tr>
<td>Neutron Fluence (n/cm2)</td>
<td>1E13</td>
</tr>
<tr>
<td>Prompt Dose Upset (rad(Si)/s)</td>
<td>1E9</td>
</tr>
<tr>
<td>Prompt Dose Survival (rad(Si)/s)</td>
<td>1E12</td>
</tr>
</tbody>
</table>

## Key Features

<table>
<thead>
<tr>
<th>Features</th>
<th>RH15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation</td>
<td>STI</td>
</tr>
<tr>
<td>Thin Oxide / DGO Devices</td>
<td>26 Å / 70 Å</td>
</tr>
<tr>
<td>Vdd Options</td>
<td>1.5 V / 1.8 V / 3.3 V</td>
</tr>
<tr>
<td>Metal Levels</td>
<td>7</td>
</tr>
<tr>
<td>Capacitors</td>
<td>Yes</td>
</tr>
<tr>
<td>Resistors</td>
<td>Yes</td>
</tr>
<tr>
<td>C4 / Wirebond</td>
<td>Y/Y</td>
</tr>
</tbody>
</table>
### RH15 Performance Parameters Test Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Goal</th>
<th>Threshold</th>
<th>Test Results</th>
<th>Status</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage</td>
<td>1.5, 1.8 and 2.5V</td>
<td>1.5, 1.8 and 2.5V</td>
<td>1.5, 1.8 and 2.5V</td>
<td>Complete</td>
<td>Goal level achieved.</td>
</tr>
<tr>
<td>Operating Temp</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Full Performance</td>
<td>0 - 80C</td>
<td>0 - 80C</td>
<td>0 - 80C</td>
<td>Complete</td>
<td>Goal level achieved.</td>
</tr>
<tr>
<td>• Functionality</td>
<td>-55 - 125C</td>
<td>-55 - 125C</td>
<td>-55 - 125C</td>
<td>Complete</td>
<td></td>
</tr>
<tr>
<td>Operating Speed</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Worst Case and Post Radiation</td>
<td>1GHz</td>
<td>500Mhz</td>
<td>&gt; 3GHz</td>
<td>Complete</td>
<td>Goal level achieved.</td>
</tr>
<tr>
<td>Total Ionizing Dose (rd(Si))</td>
<td>= 1M</td>
<td>= 500K</td>
<td>&gt; 2M</td>
<td>Complete</td>
<td>Goal level achieved.</td>
</tr>
<tr>
<td>Single Event</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Upset (errors/bit-day)</td>
<td>&lt;1E-11</td>
<td>&lt;1E-10</td>
<td>3.4E-11 S-ASIC, &lt;&lt;1E-12 SRAM</td>
<td>Complete</td>
<td>Goal level achieved.</td>
</tr>
<tr>
<td>• Latchup (MeV-cm2/mg)</td>
<td>&gt;120</td>
<td>&gt;100</td>
<td>&gt;127</td>
<td>Complete</td>
<td>Goal level achieved.</td>
</tr>
<tr>
<td>Neutron Radiation (n/cm2)</td>
<td>&gt;1E13</td>
<td>&gt;1E12</td>
<td>&gt;1E13</td>
<td>Complete</td>
<td>Goal level achieved.</td>
</tr>
<tr>
<td>Dose Rate (rd(Si)/s)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Upset</td>
<td>&gt;1E10</td>
<td>&gt;1E9</td>
<td>2.2E9</td>
<td>Complete</td>
<td>Threshold level achieved.</td>
</tr>
<tr>
<td>• Survivability</td>
<td>1E12</td>
<td>1E12</td>
<td>1E12</td>
<td>Complete</td>
<td>Goal level achieved.</td>
</tr>
</tbody>
</table>

RH15 KPP testing and verification successfully completed
RHFGPA Package

**Base Package:** (Developed for FG-HPSC (OGA))

- Ceramic Column Grid Array
  - Flip Chip Ceramic Column Grid Substrate (CCGA)
  - Hermetic Seam Weld Sealing
  - Substrate: 35 x 35mm
  - 34 x 34 Column Array
    - 1.0mm pitch
    - 1144 Total I/O
      - 840 signal
      - 304 Vdd and Gnd
  - Die site accommodates up to 20 mm Die

**RHFGPA Package Plans:**

- Package Modeling – 10/08 – 12/08
- Update Substrate Design & Verification – 12/08 – 2/09
- Package Availability – 4/09

Package to be Modified to Accommodate Programmable I/O Features
Summary

- Test Site
  - Electrical performance matches simulation (289 MHz)
  - Preliminary SEU Radiation testing performed by NASA
  - Data shows no SEU observed up to LET of 58 at 0° & 45° angles of incidence

- RHFP GA Program
  - Technical Goals of the Program Established
    - Build a multimillion reconfigurable RHFP GA using:
      - Achronix patented architecture
      - BAE’s RADHARD process technology
  - Preliminary Product Requirements defined
  - Program Plan in place

- Design Activity underway
  - Defined Design Approach Methodology
  - Defined Specification details for BRAM, S-Frame, I/O, PLL.