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MAFA 2007

Update on the Universal FPGA Support Device for Spaceborne Applications

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Figures and technical data from UFSD paper cleared for public release - VS07-0069

Agenda

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- Processing Needs and Reconfigurable Computers
- Universal FPGA Support Device (UFSD) Architecture
- UFSD Phase 1 Products
- UFSD Phase 2 Efforts
- Reconfigurable Computers for Future Missions
- Summary

RAD750 Processing Fabric

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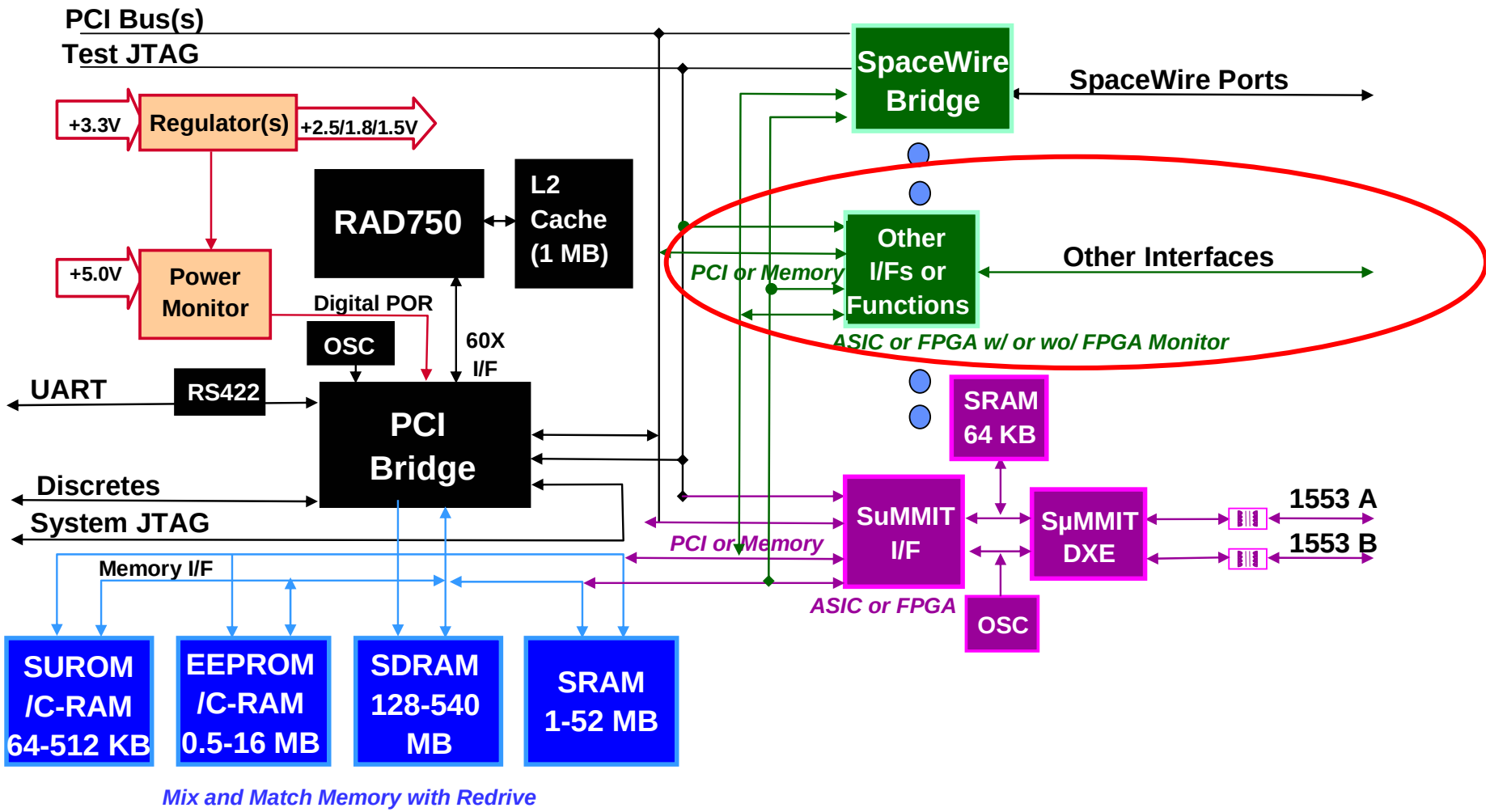

Fuse-based FPGAs Typically Provide non-ASIC C&DH interfaces Today

Filling the Processing Spectrum

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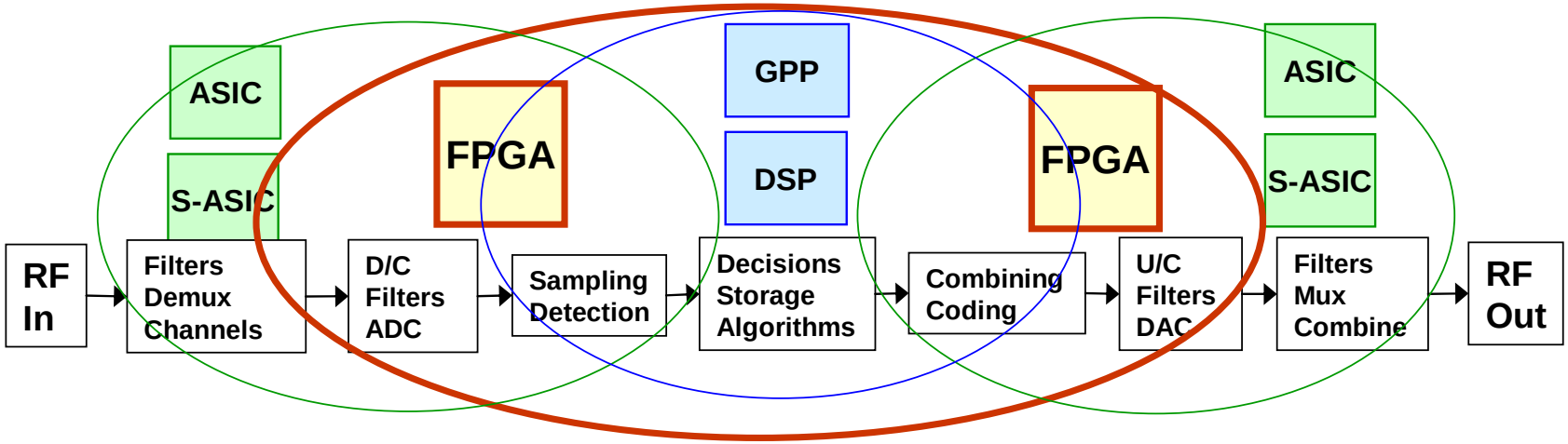

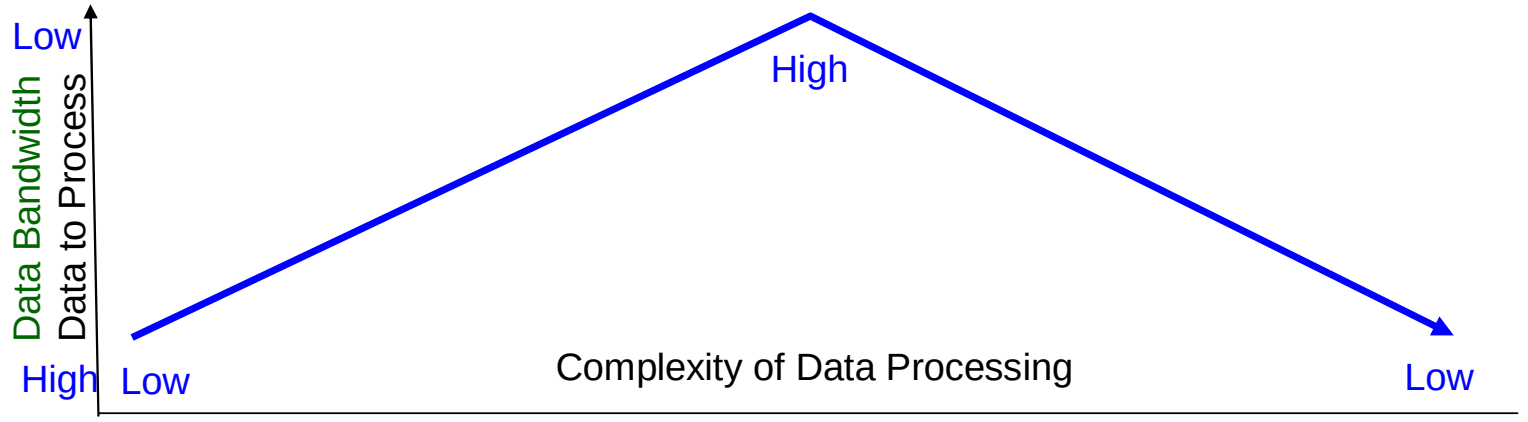

To Produce Processing and Payloads, FPGAs are key to Spacecraft Applications being Optimized across Technologies

Re-Configurable Computing Thru a Spacecraft

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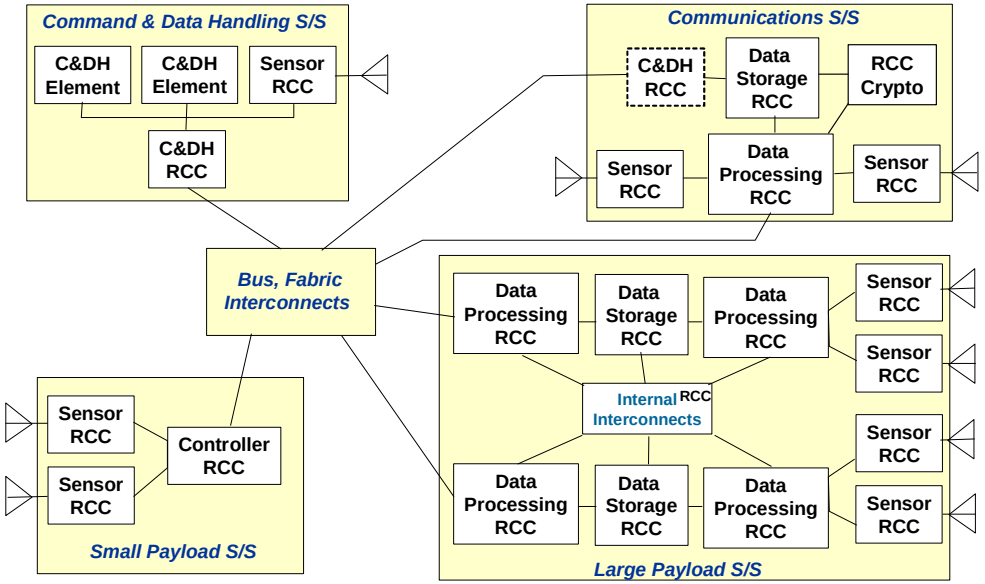
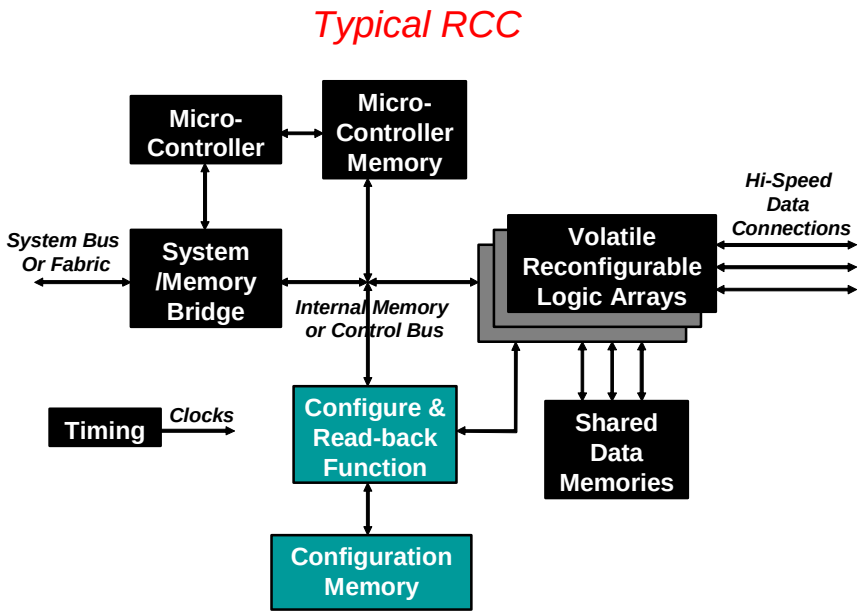


RCC Elements

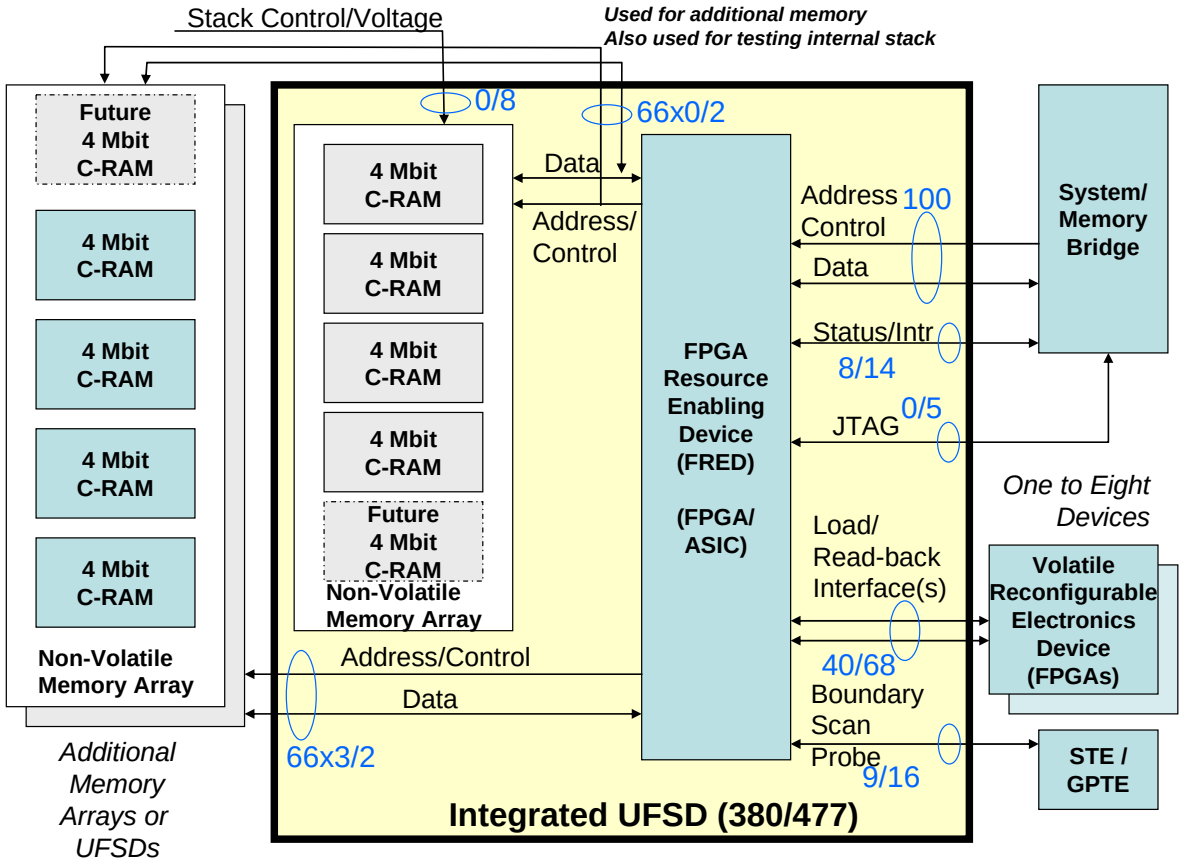


- C&DH: CPU(RAD6000/RAD750) + Memory + I/O
- Sensor: I/O + Device + Conversion
- Controller: Controller (EMC/RAD6000) + Memory + I/O
- Crypto: Crypto ASIC
- Data Storage: Bulk Memory
- Data Processing: Signal Processing
- Interconnect/Routing: Switch Fabric + Mux/Demux + Signal Processing

One RCC size does not fit all; But critical technology (FPGAs, UFSD, C-RAM, infrastructure) to create and use RCCs will be used across most types

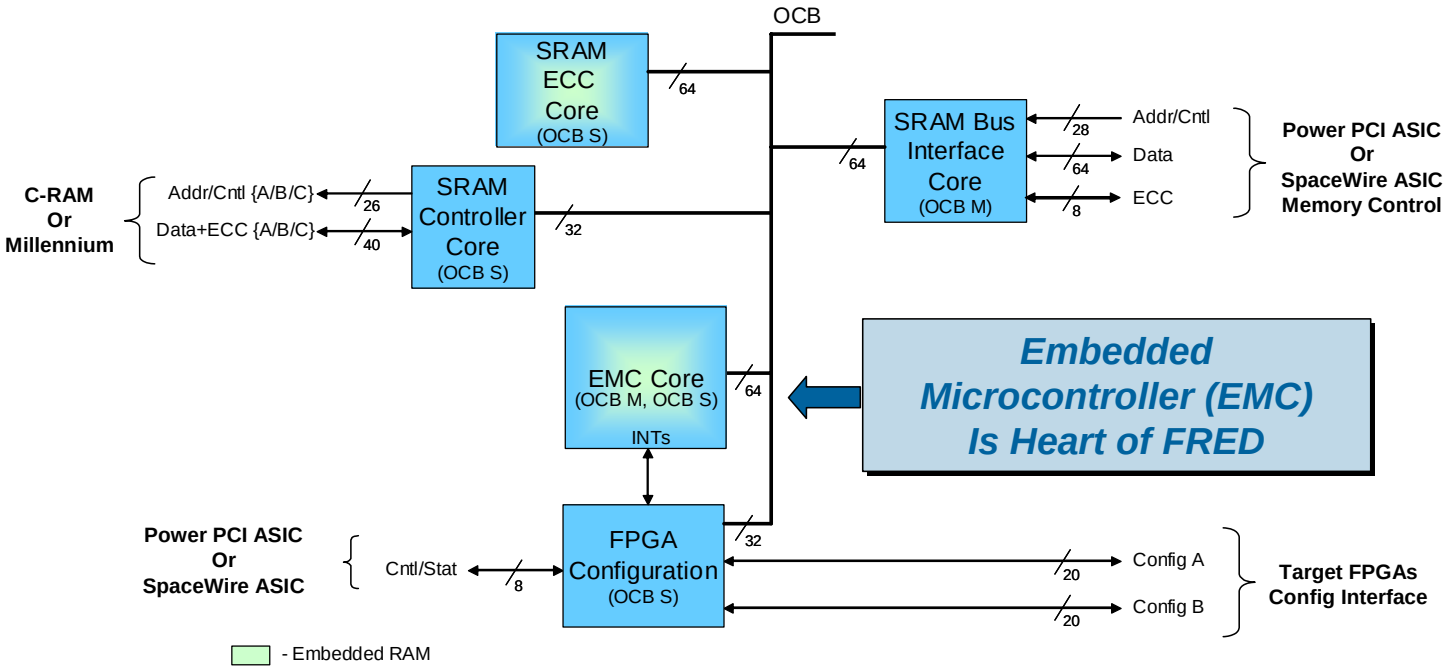
Universal FPGA Support Device

- **UFSD - FRED FPGA or ASIC standalone or stacked with rad-hard C-RAM for configuration and code storage**
- **Rad-hard RTAX2000 or RH15 CMOS ASIC**
- **Embedded EMC controls configuration of up to 8 RAM-Based FPGAs**
- **EMC reads own configuration and code and then programs FPGAs**
- **Looks like memory, PCI or JTAG device to system**
- **Handles scrub, partial and SEFI mitigation**
- **Reconfigurable for new devices**
- **RTAX Actel FRED and Test Board Available now**



UFSD Architecture centered on single FPGA Resource Enabling Device (FRED)

FRED FPGA Block Diagram



- Single Device Controls any Re-programmable Element (FPGA, FPAA,…)
- Supports up to 2 Configuration Interfaces with up to four devices each (Slave Serial, SelectMap, JTAG)
- Supports up to Three Banks of Configuration Memory with 24 MB each
- Loads Configuration Memory and Behavior Algorithms from Attached Non-Volatile Memory
- Attaches as Memory Device with Internal Access to Registers and Pass Through to Memory
- Provides Interrupts to Embedded System

Internal Cross Bar Switch (OCB) Connects Reused Cores in FRED

C-RAM Stack Package

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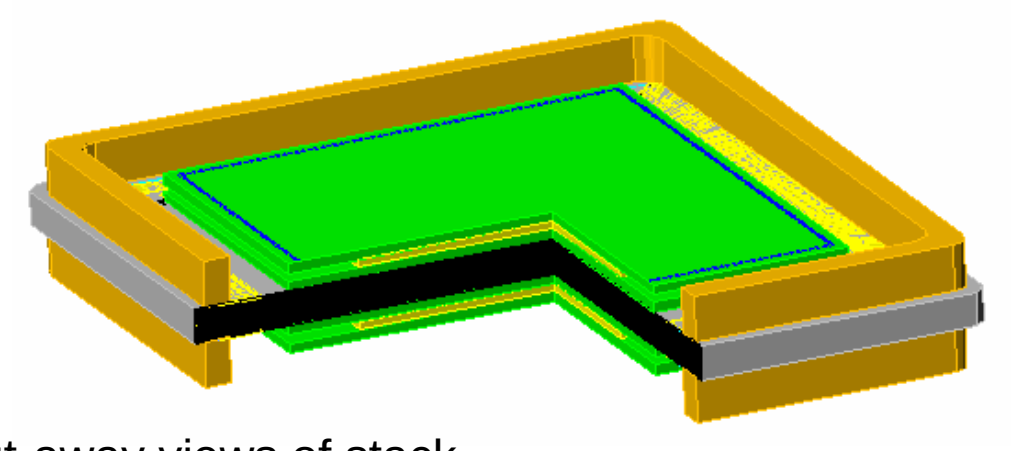
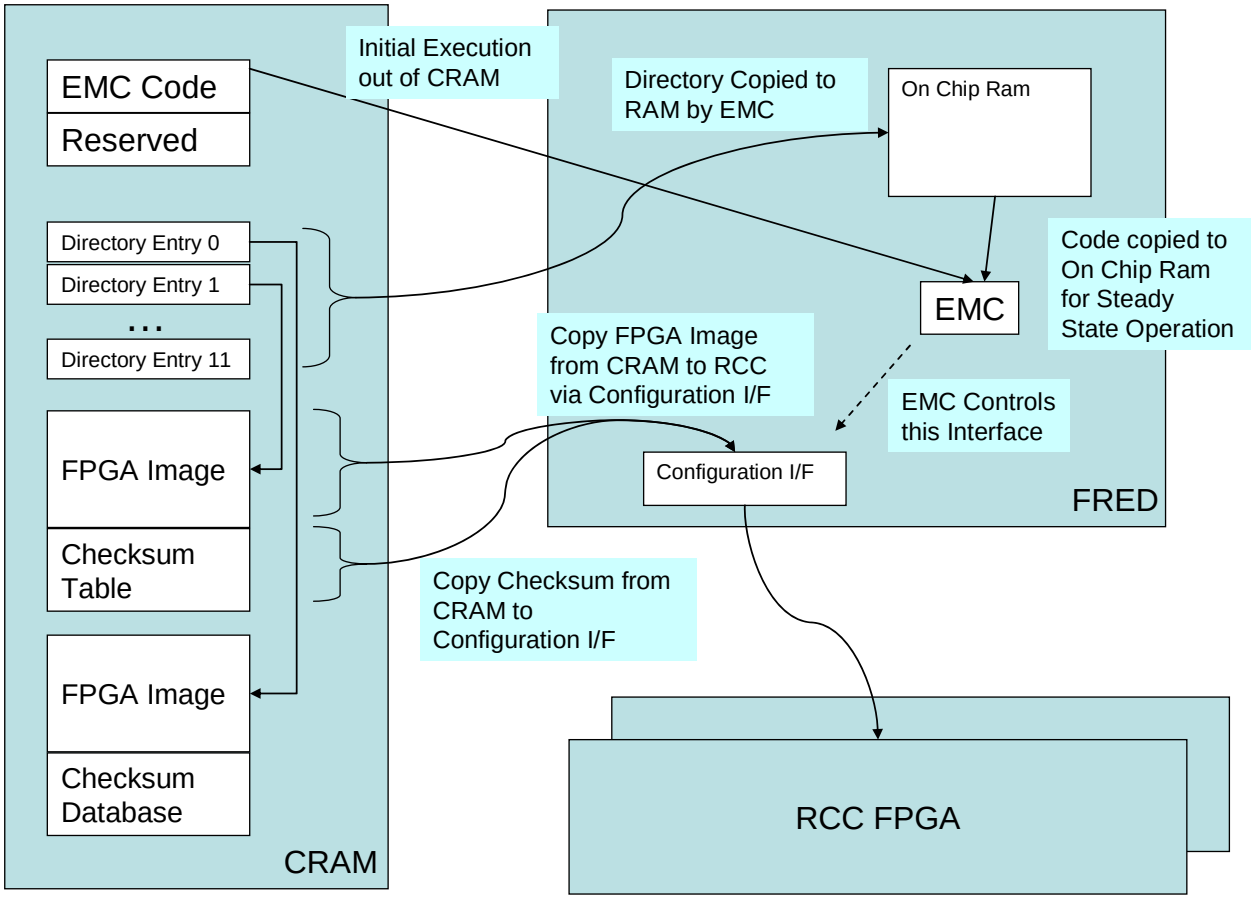
- Design:
  - 4-chip stack;
  - Two-die on each side, stacked
  - Interposer
  - Millennium footprint compatible (with minimal board impact)
  - Footprint supports 5 High Stack (Phase 2)

This provides 16 Mbit of Configuration Memory



Cut-away views of stack

UFSD Programming



The EMC in FRED performs Initialization, Configuration, Readback and Scrubbing of FPGAs

UFSD Test Board

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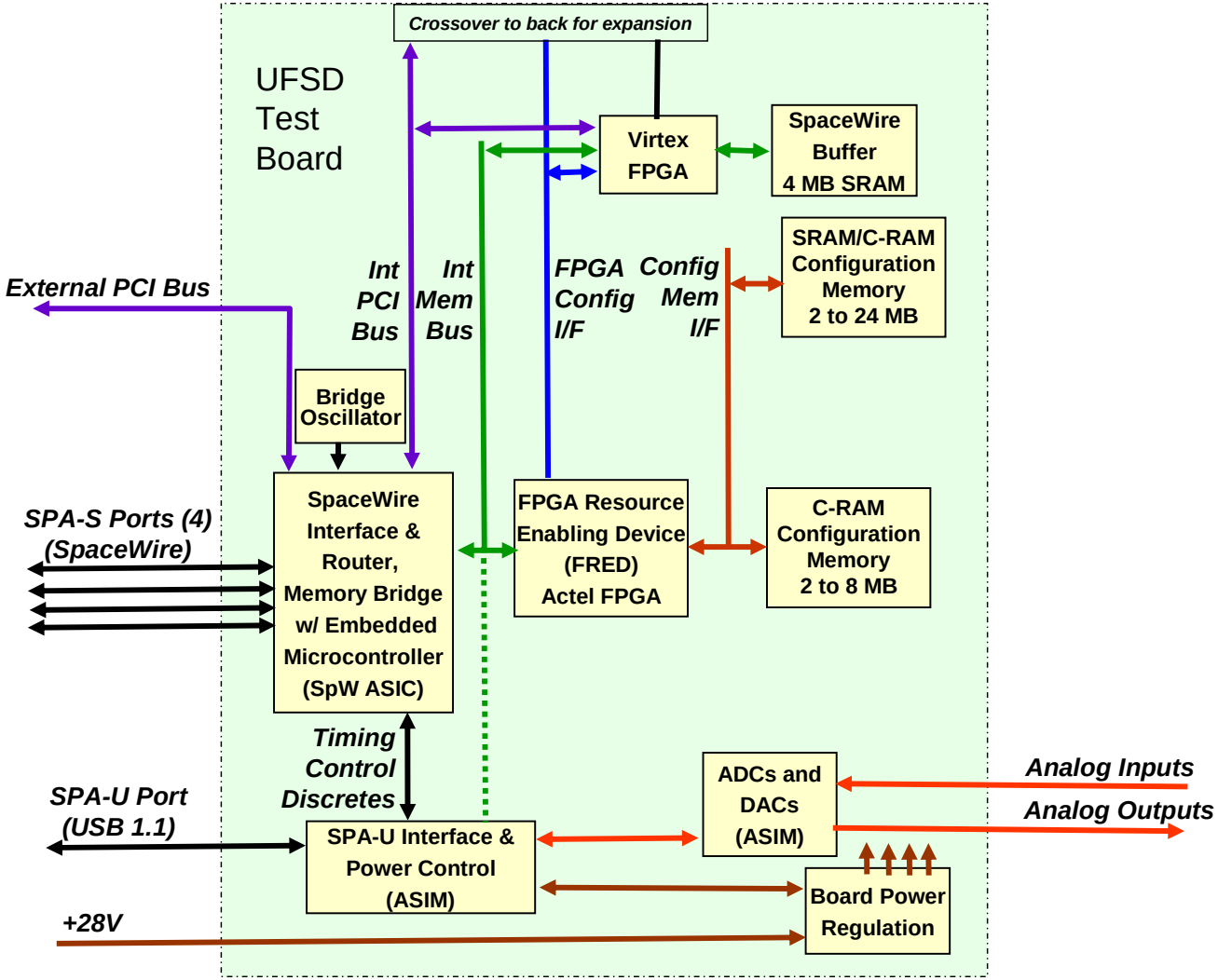
- Four SpaceWire Ports
  - with embedded Router and microcontroller
- Two Compact PCI Bus interfaces
  - Internal & External
- FPGA Resource Enabling Device (FRED) in Actel RTAX2000
- Virtex II Pro VP40 Target FPGA with 4 MB SRAM buffer
- Three Banks of FRED Memory with C-RAM/SRAM Footprint
- Memory, PCI and Configuration Interface Crossovers to Back
- Space PnP ASIM Device for SPA-U and SPA-S
- Voltage Conversion from 28V or 12V controlled by ASIM
- UART/JTAG on Test Connector
- 6U-220 Single Board with wedgelocks

Initial Board tests FRED and C-RAM Stacks



UFSD Current Test Board Photo

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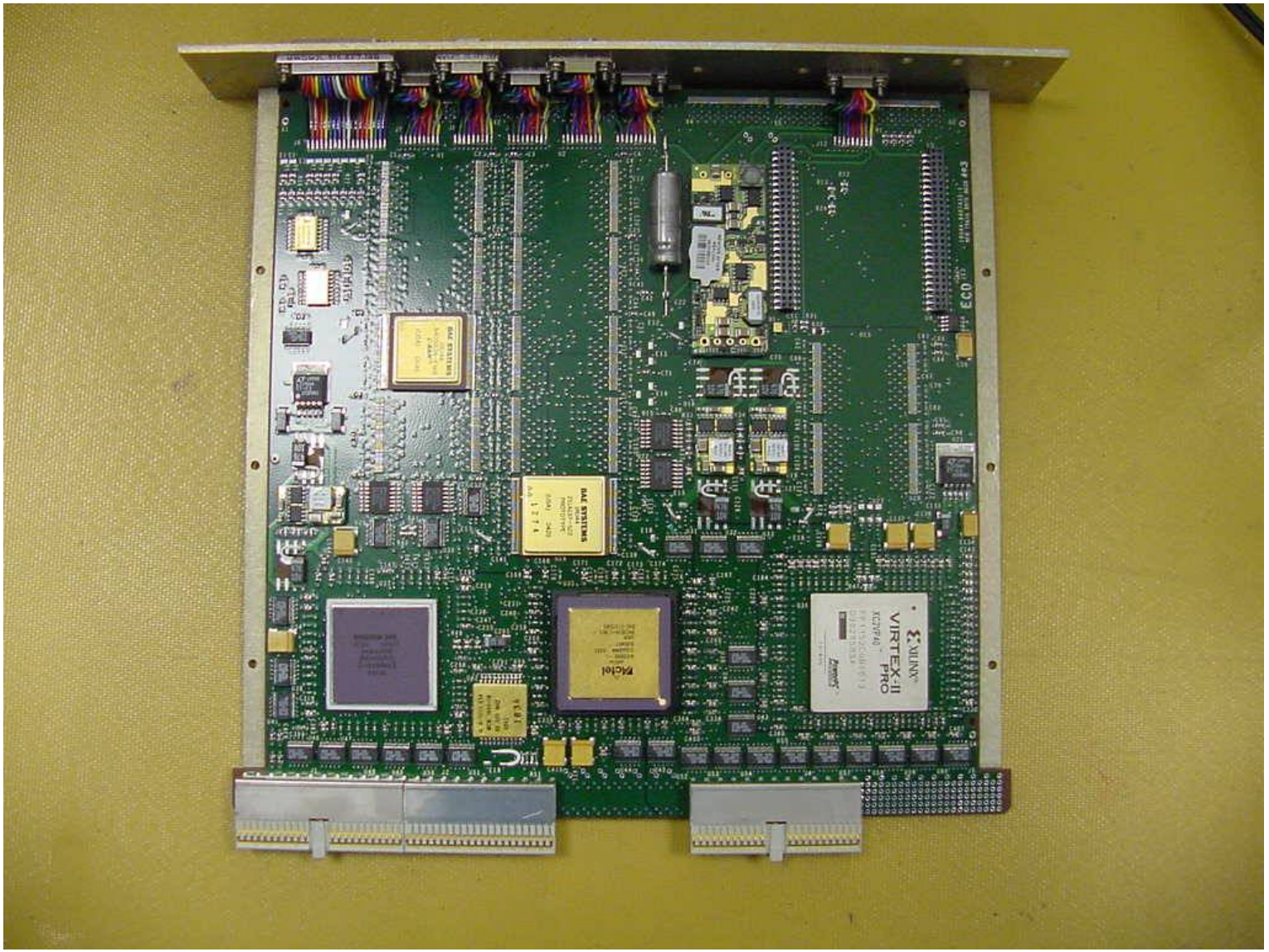

Board Currently Working in Lab

FRED ASIC Implementation Options

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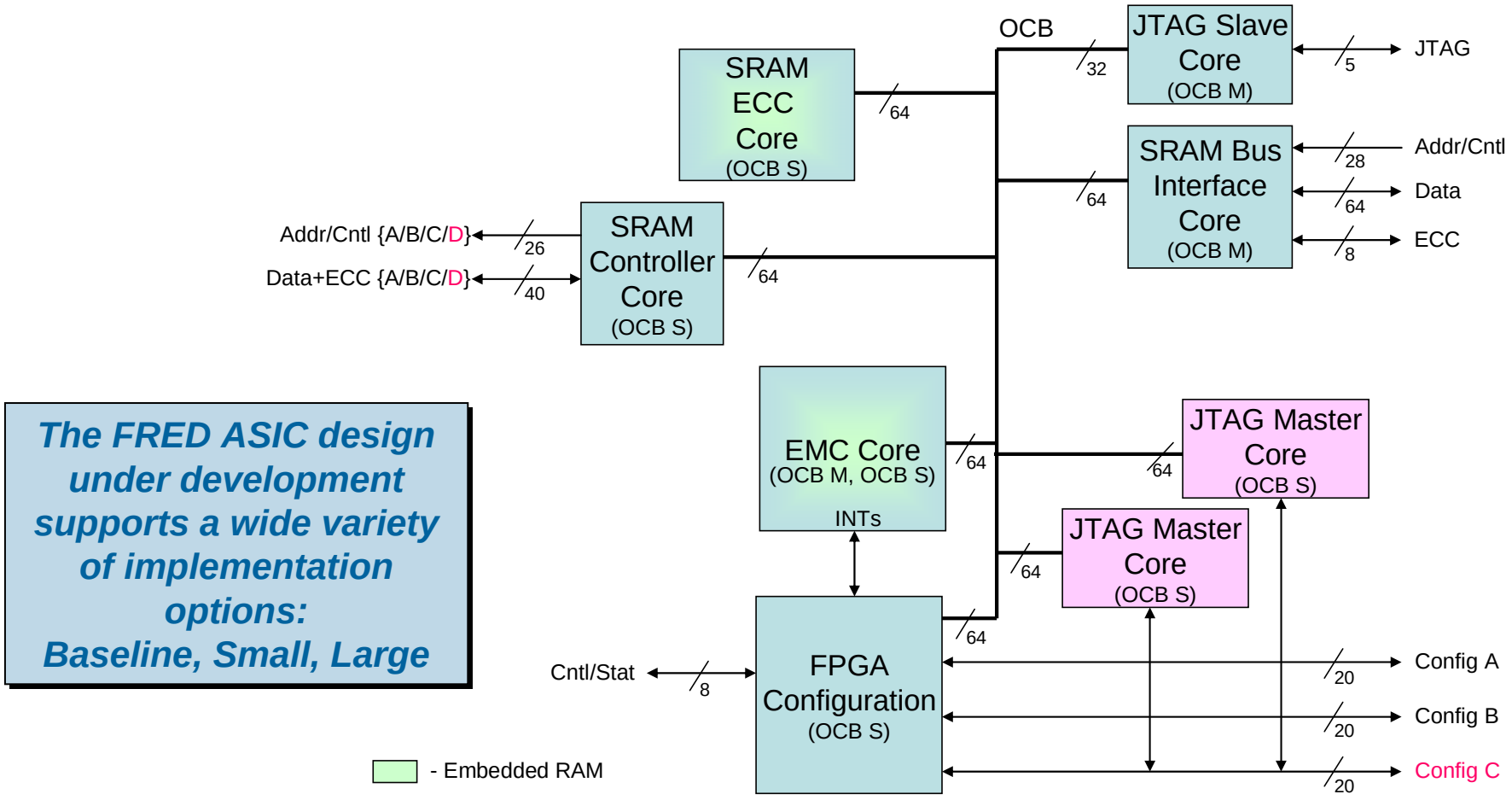

The FRED ASIC design under development supports a wide variety of implementation options: Baseline, Small, Large

Combined ASIC / C-RAM UFSD MCM

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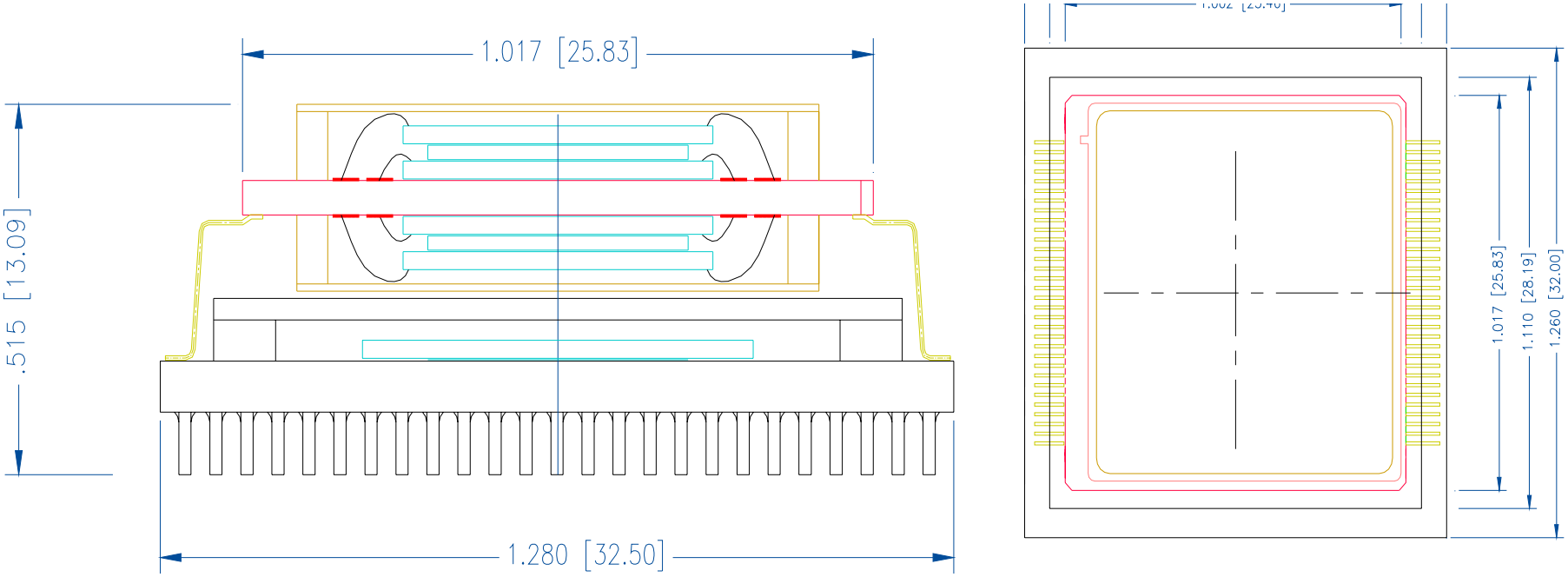
- Mount RH15 Structured ASIC in 32.5 mm 624 pin CGA Package
- Mount 4-High C-RAM Stack on top
- Analysis of resonance, displacement and thermal complete



UFSD Concept Modeling with latest FRED and C-RAM Stack viable for Space Systems

Summary

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- **Processing Systems will require Reconfigurable Elements throughout a Spacecraft today and in the future for performance, fault tolerance, responsiveness and flexibility as well as pathfinding prototypes**
- **Key to creating Reconfigurable Systems is the infrastructure.**
- **Our UFSD Program has created various FPGA support components and a test board**
- **We are continuing to develop the UFSD to provide the minimum SWAP and maximum flexibility in any FPGA support device**
- **Leveraging our UFSD Test Board and other Space Processing Boards and elements allows us to put together and deliver a variety of reconfigurable processors to match the many types that an application needs to complete its mission**

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