GAISLER RESEARCH

The Gaisler Research Roadmap for FPGA IP-Cores

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Military and Aerospace FPGA and Applications (MAFA) Meeting

Palm Beach

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Outline

- Introduction to Gaisler Research
- GRLIB IP core library
- Plug & Play on the chip-level
- LEON3 SPARC V8 processor
- Architecture and Fault Tolerance
- IP cores
- Latest IP cores
- Roadmap for future IP cores
- Conclusions

Gaisler Research

- Founded in 2001 by Jiri Gaisler
- Spin-off from European Space Agency (ESA)
- Independent and privately owned company
- Located in Gothenburg, Sweden
- New modern down-town offices, 500 m²

Gaisler Research – company profile

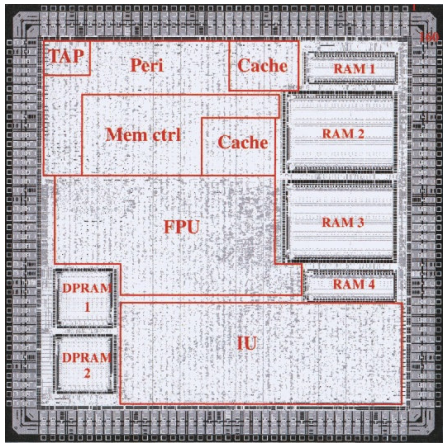
- Staff members:
  - 14 engineers
  - 2 marketing and sales
  - 2-4 in-house trainees
- Design engineers with expertise within electronics, ASIC and software design
- Complete design facilities in-house for ASIC and FPGA design
- Company active in ECSS SpaceWire standardization

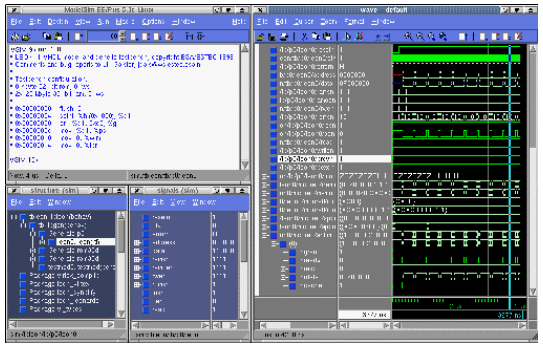
Gaisler Research - management

- Management team with 40 years combined experience in the space sector:
  - Per Danielsson: President and CEO
    - Radiance Innova AB, President and CEO
    - Saab Space, Division Manager
  - Jiri Gaisler: Chairman and CTO
    - European Space Agency, Systems Design
    - Saab Space, Computer Design
  - Sandi Habinc: Vice President of Products
    - European Space Agency, Microelectronics
    - Serco Space, Senior Design Engineer
    - Saab Ericsson Space, Digital Design

Gaisler Research – product portfolio

- LEON3 32-bit processor, STD/FT
- LEON3 compatible IP cores:
  - GRFPU, Floating Point Unit
  - SDRAM controller
  - PCI bridge
  - 10/100/1000 Mbit Ethernet MAC

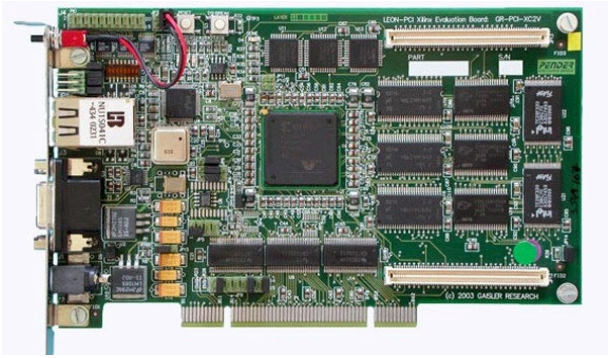




- TSIM, LEON simulator
- GRMON, LEON Debug monitor

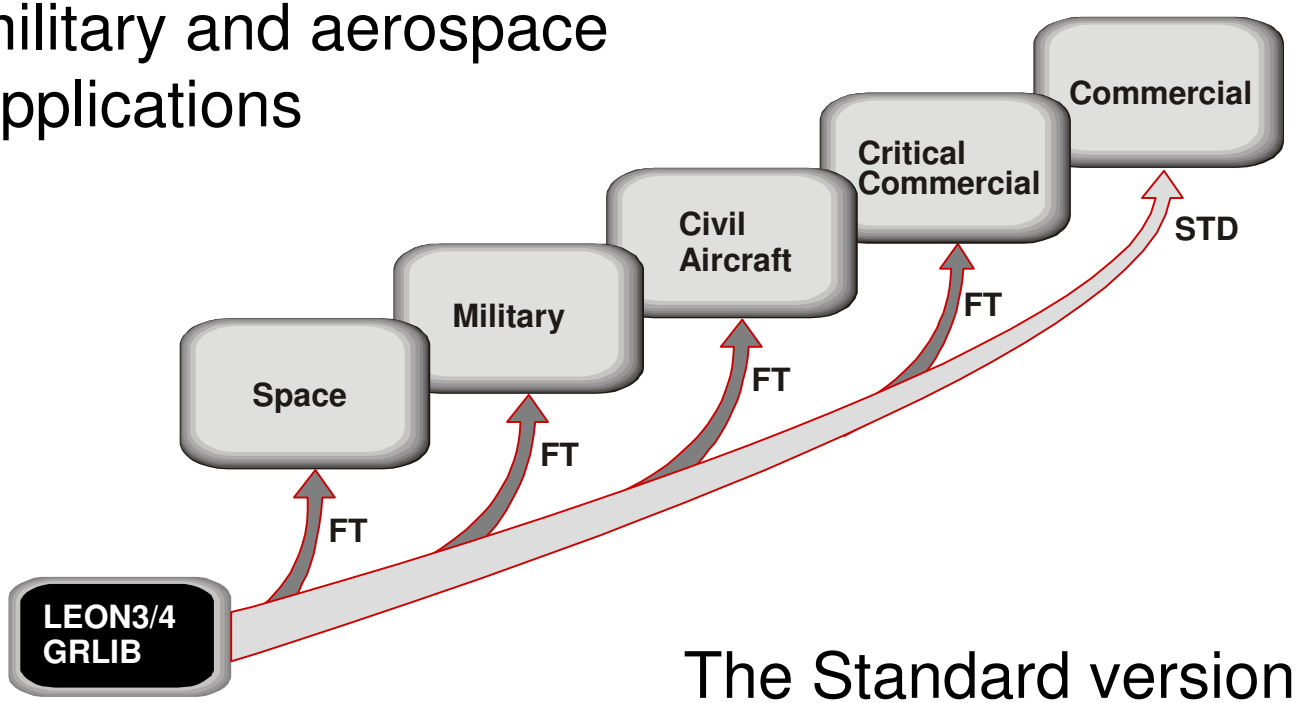
LEON development boards

- Technical support and adaptations
- Full software development environment based on open source tools



Gaisler Research – markets

The Fault Tolerant (FT) version is used for critical, military and aerospace applications



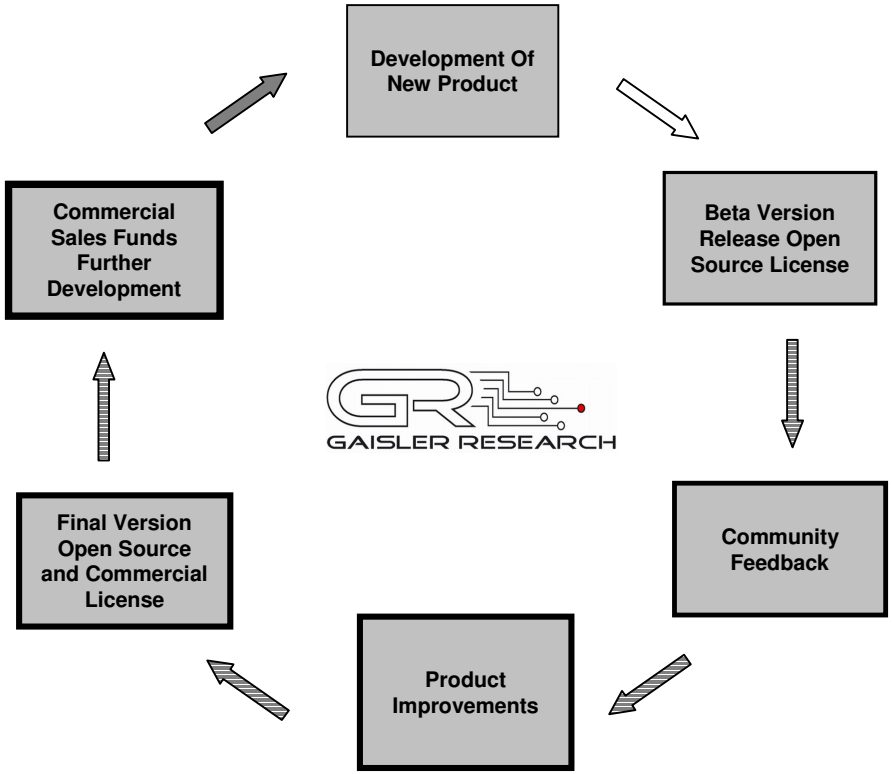
The Standard version (Non-FT) is used for commercial applications

Gaisler Research – applications

- Space
  - Satellites
    - Spacecraft controllers (parts, IP cores, tools)
    - Instruments (IP cores, tools)
  - Ground systems (tools)
  - Launchers (tools)
- Military (IP cores, tools)
  - Non-disclosed applications
- Commercial (IP cores, tools)
  - GPS/GLONAS receivers
  - Routers, MP3 players, Video codec, Set-top boxes
  - Automotive
  - Non-disclosed applications
- Research and Universities
  - Used by hundreds of institutes and research centres

Gaisler Research – business model

Gaisler Research uses an open source business model based on Dual Licensing. It allows to provide commercial licenses for a fee, and at the same time to offer source code under open source licenses.



IP Core issues

The integration of IP cores from multiple vendors into a single FPGA or ASIC design is a challenging task.

It involves the harmonization of:

- On-chip buses & Signal interfaces
- Merging of synthesis scripts and constraints
- Merging of constraints
- Mapping of technology specific macros cells:
  - Embedded memory
  - I/O ports
  - Clock generation (PLL, DCM, etc.)
- Protection against radiation effects

The rationale for the GRLIB IP core library is to offset these problems.

GRLIB IP Core library

GRLIB is a complete design environment:

- Large set of IP cores
- AMBA on-chip bus with Plug & Play support
- Bus-centric approach
- Strict VHDL coding methodology:
  - Two-process model
  - Extensive use of record types
- Support for portability between technologies:
  - Actel, Altera, Lattice, Xilinx, ASIC
- Support for many tools:
  - Synplify, Synopsys, Cadence, Mentor Precision, Xilinx, Quartus, Actel Designer, ModelSim, GHDL
- Support for many FPGA prototyping boards

AMBA

Advanced Microcontroller Bus Architecture (AMBA):

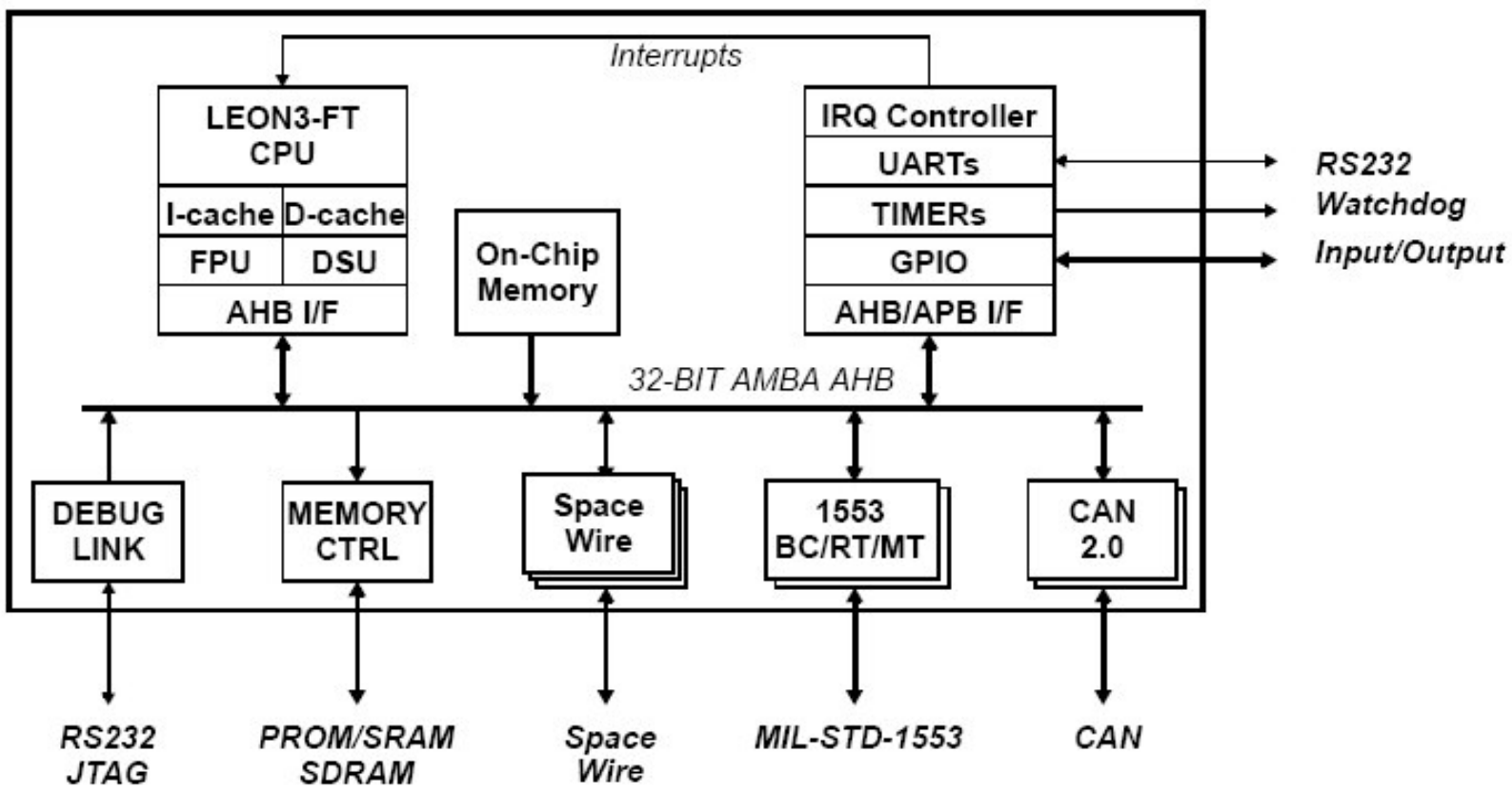
- Fully pipelined arbitration, address and data phases
- Multi-master, multi-slave
- Burst access: incremental or fixed size (up to 1024 bytes)
- Byte, half-word, word or larger data structures (up to 1024 bits)
- Separate high-performance and peripheral buses
- Open, non-licensed, standard

- The standardization has resulted in a multitude of synthesizable cores that are integrated in system-on-a-chip designs.

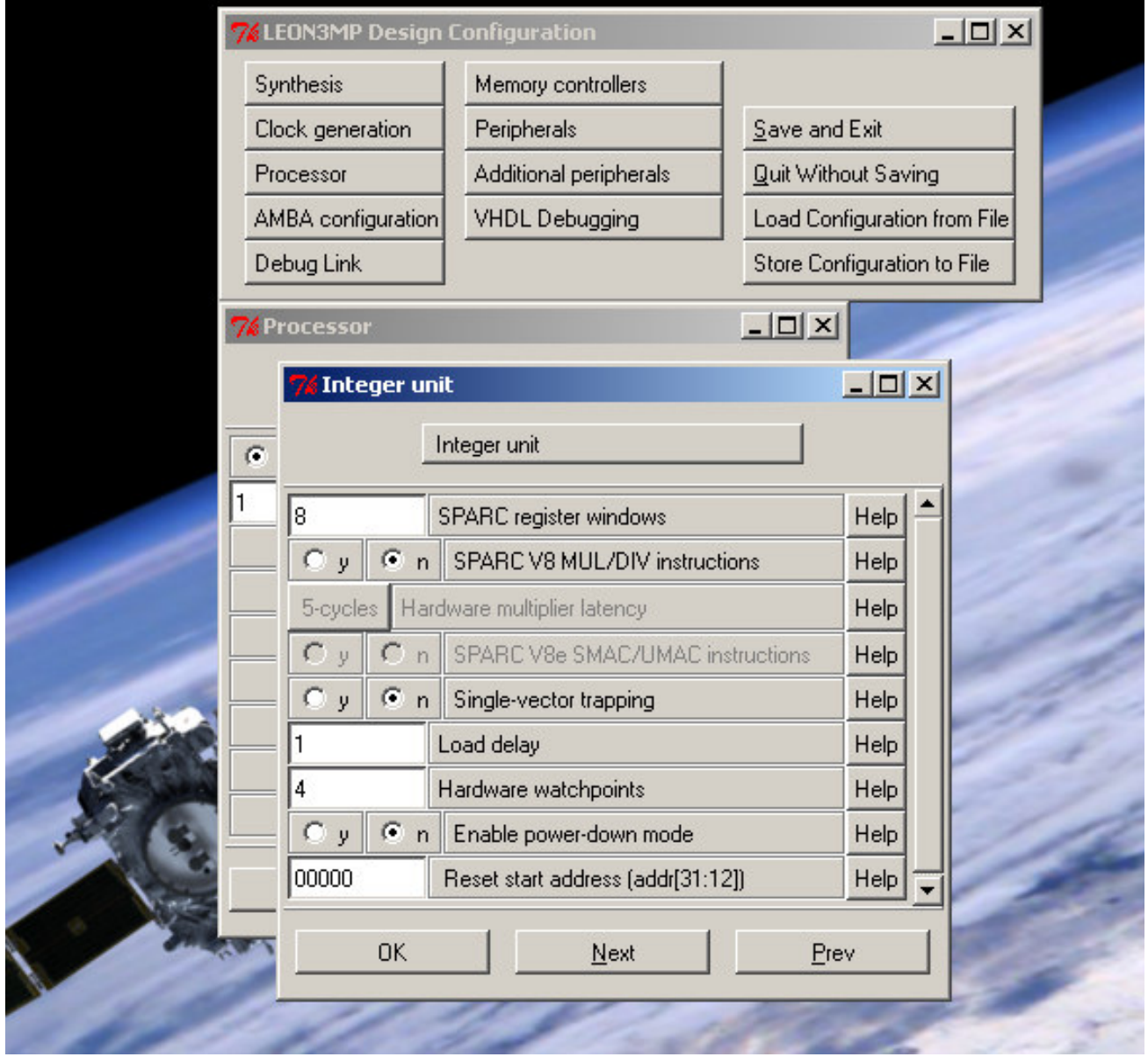
AMBA Plug & Play

- GRLIB extends AMBA with Plug&Play (PnP) capability
- PnP information allows for distributed address decoding, interrupt steering, cacheability information, etc.
- No modification of centralized resources, e.g. address decoder, arbiter or interrupt controller.
- Automatic generation of table including vendor and device identifier for each attached core, including version and interrupt information.
- Software can scan table and install the corresponding drivers etc.
- Hardware debuggers can use table for initializing the various IP cores etc.

Typical GRLIB based design



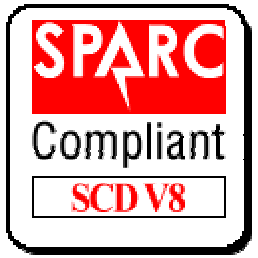
Configuration of a design



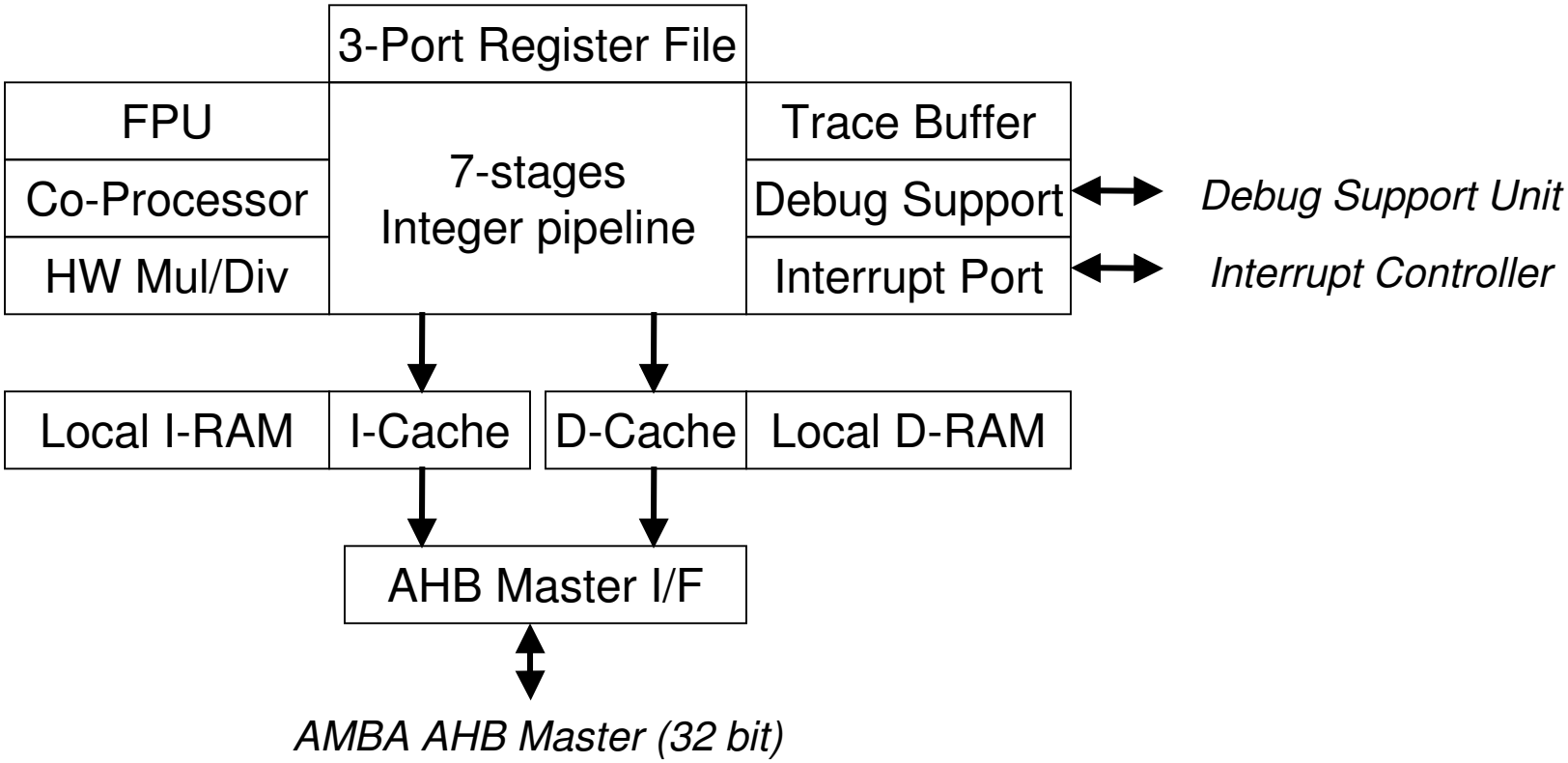
LEON3 32-bit processor

Advanced 32-bit processor IP core:

- implementing the SPARC V8 instruction set
- 7-stage pipeline, hardware mul/div
- Separate instruction and data multi-set caches (Harvard architecture, set-associative caches)
- Data cache snooping
- Fast branch address generation
- Optional Floating Point Unit
- Optional Memory Management Unit
- Optional Co-processor interface



LEON3 architecture



LEON3 features

High Performance

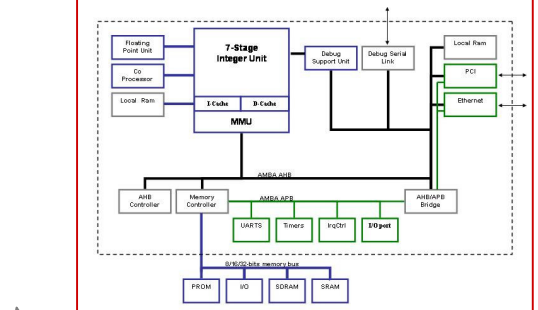
- 400 MHz on UMC 0.13 µm ASIC (std-cell)
- 125 MHz on Xilinx Virtex FPGA

Open Source Standard SW Environment

- GNU C/C++ compiler
- RTEMS real-time kernel
- eCos real-time kernel
- SnapGear Linux

Low Gate Count

- 25 kgates for ASIC
- 3,500 LUT for Xilinx FPGA
- 4,000 Cells for Actel FPGA



Full Simulator and Debug Monitor

- Simulator for developing and debugging SW
- Monitor for HW and SW validation

IP-Library of Cores for SOC Design

- Portable and Vendor independent
- Connection through standard AMBA bus

Customer Approval and Validation

- LEON is the standard processor of ESA
- Numerous commercial customers are using LEON

LEON3 fault tolerance

SEU tolerance by design for space applications

All on-chip memory protected against SEUs:

- Register file
- Cache memories
- No timing penalty
- Instruction re-scheduling on error

Flip-flops protected by technology specific cells (or by TMR)

Legacy IP cores

- Floating Point Unit (IEEE-754)
- SPARC Reference Memory Management Unit
- Ethernet MAC 10/100 Mbit/s
- CAN 2.0 Controller, simple interface
- MIL-STD-1553B BC/RT/M (Actel)
- PCI 32-bit, initiator & Target
- SpaceWire with RMAP
- Memory controllers
  - SRAM/PROM/EEPROM/FLASH
  - SDRAM & SDRAM DDR / DDR2
- Interrupt Controller, Timers, GPIO, UART
- CCSDS Time Management Unit
- VGA, IDE, DMA, security, etc.

Latest IP cores

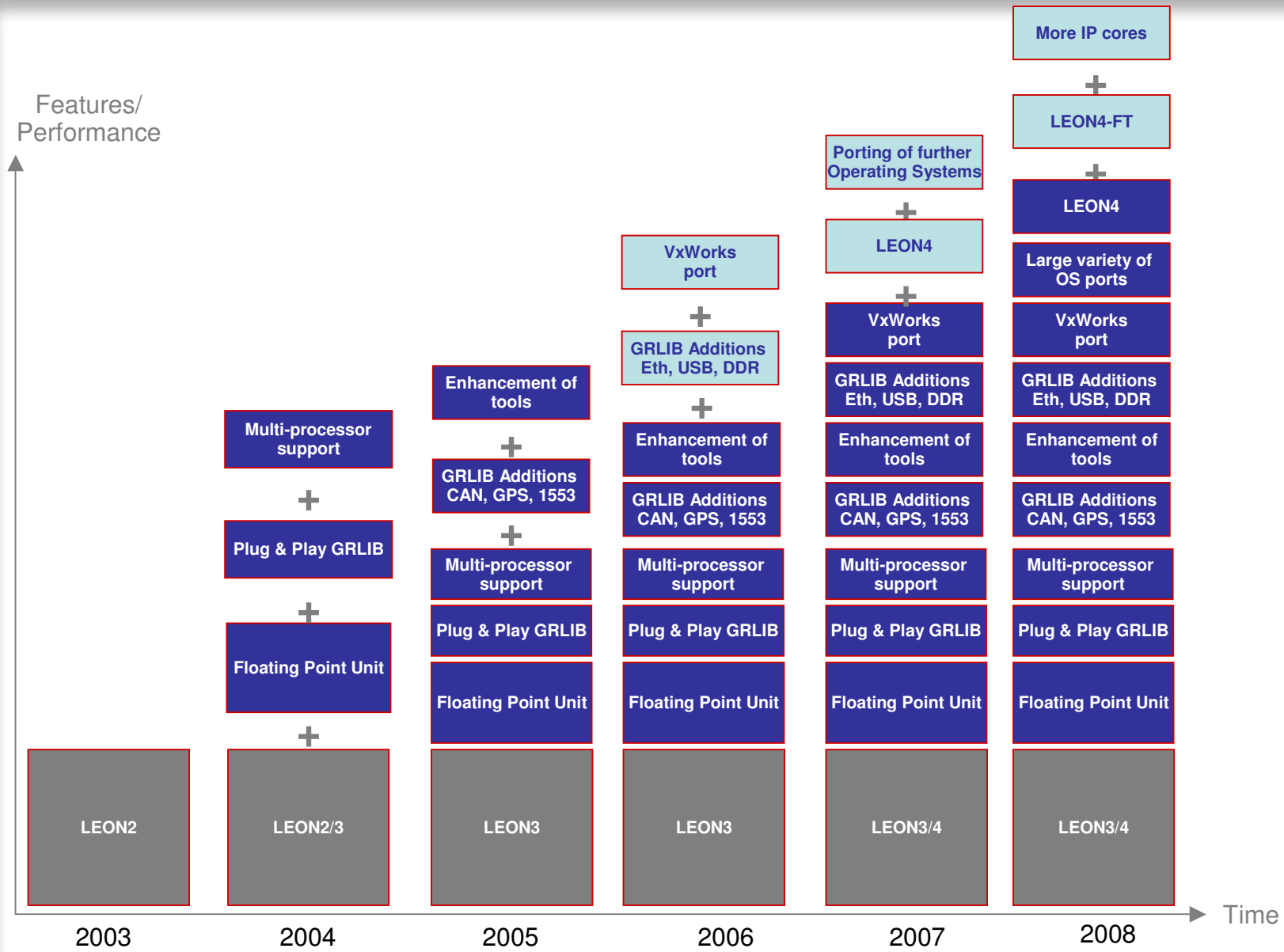
- USB 2.0 Host Controller
- CAN 2.0 Controller with DMA
- Gigabit Ethernet MAC with EDCL
- I^2C Master
- Serial Peripheral Interface (SPI) Controller

- Combined ADC / DAC Interface
- External FIFO Interface with DMA

Future IP cores

- New SpaceWire CODEC with increased performance (GRSPW2) (completed)
- 16 and 32-bit DDR Controller, with Reed-Solomon based memory protection
- 16 and 32-bit DDR2 Controller, with Reed-Solomon based memory protection
- SDRAM Controller, with Reed-Solomon based memory protection
- CCSDS Telemetry and Telecommand
- LEON4 processor, with Non-blocking pipeline, Instruction streaming buffer, 64-bit AMBA interface etc. (in progress, not targeting FPGA)

Roadmap


Features/
Performance
LEON2
Floating Point Unit
Plug & Play GRLIB
Multi-processor support
LEON2/3
Floating Point Unit
Plug & Play GRLIB
Multi-processor support
GRLIB Additions CAN, GPS, 1553
Enhancement of tools
LEON3
Floating Point Unit
Plug & Play GRLIB
Multi-processor support
GRLIB Additions CAN, GPS, 1553
Enhancement of tools
VxWorks port
LEON3
Floating Point Unit
Plug & Play GRLIB
Multi-processor support
GRLIB Additions CAN, GPS, 1553
Enhancement of tools
VxWorks port
LEON4
Porting of further Operating Systems
LEON3/4
Floating Point Unit
Plug & Play GRLIB
Multi-processor support
GRLIB Additions CAN, GPS, 1553
Enhancement of tools
VxWorks port
LEON4
Large variety of OS ports
LEON4-FT
More IP cores
LEON3/4
2003
2004
2005
2006
2007
2008
Time

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Conclusions

- GRLIB library provides a large set of harmonized IP cores suitable for the space market, targeting both FPGA and ASIC
- The library is being continuously extended with new IP cores and support for new FPGA development boards
- The GRLIB IP core concept widely used in space community
- Applications based on the GRLIB IP core library will be presented during the Applications Day