

Overview of FPGA activities in ESA

European Space Agency

David Merodio Codinachs
ESTEC/TEC-EDM
david.merodio.codinachs@esa.int

Presentation Overview

- **Past- Current FPGA activities**
 - Radiation tests
 - Standards
 - Information on ESCIES
 - Atmel, Actel and Xilinx related activities
- **Summary of Future FPGA activities**
- **FPGA usage in ESA missions**
- **Conclusion**

Radiation tests

Several FPGA vendor and technologies tested under radiation in the past:

- Actel: A1020, A1280, A1425A, A141000A, A32140DX, RH1280, RT54SX32/72
 - Lattice
 - Lucent
 - Quicklogic
 - Xilinx: XQVR300, XQR2V3000 (presented MAPLD`06)
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- **Complexity is growing (capacity, packages, architectures); radiation tests are more complex**

Past FPGA activities: Standards

- **ECSS-Q60-02: ASIC and FPGA development**
 - European Cooperation for Space Standardization (ECSS) Standard
 - Released on: **17-July-2007**
 - Standardize design methods (design, verification, reviews, documentation, prototype validation and post-programming screening) to allow quality control
 - Enforce an ASIC-like design methodology for FPGA developments. Required as too heterogeneous approaches were used (as evidenced for instance by the Rosetta experience):
 - Available at:
 - <http://www.ecss.nl/>
 - <https://escies.org/ReadArticle?docId=167>



European Space Components Information

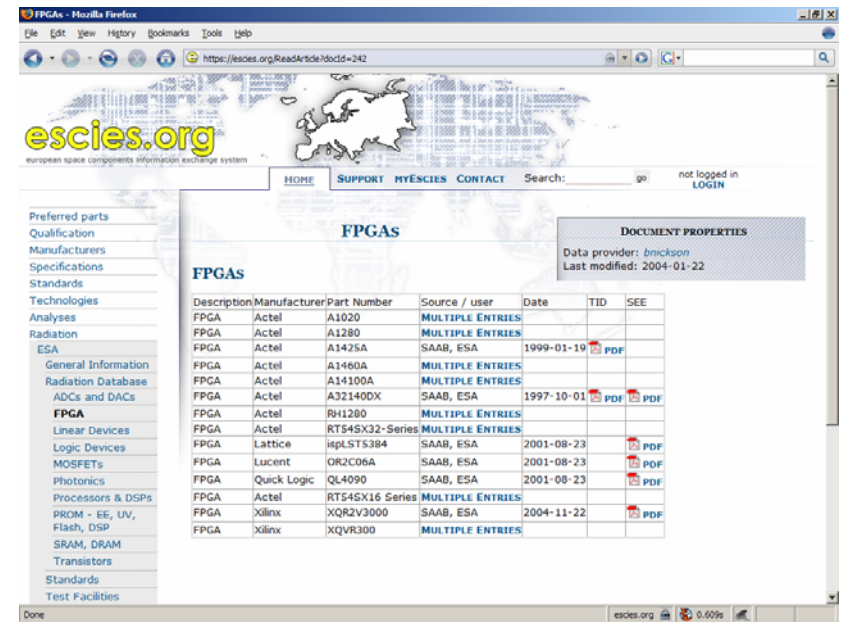
ESCIES: <https://escies.org/>

ESCIES is the European Space Components Information Exchange System and is an online library contributed to, and used by, European space industries and agencies.

Most of the information is available also for non registered users

For instance:

- Radiation test reports on FPGAs
- Radiation test standards and European test facilities



The screenshot shows the ESCIES website interface in a Mozilla Firefox browser window. The page title is "FPGAs - Mozilla Firefox" and the URL is "https://escies.org/ReadArticle.html?id=242". The website logo "escies.org" is visible, along with navigation links: HOME, SUPPORT, MYESCIES, CONTACT, and a search bar. A "not logged in LOGIN" link is also present. The main content area displays a table titled "FPGAS" with columns: Description, Manufacturer, Part Number, Source / user, Date, TID, and SEE. A "DOCUMENT PROPERTIES" box on the right indicates the data provider is "brinkoon" and the last modified date is "2004-01-22".

| Description | Manufacturer | Part Number | Source / user | Date | TID | SEE |
|-------------|--------------|-----------------|------------------|------------|-----|---------|
| FPGA | Actel | A1020 | MULTIPLE ENTRIES | | | |
| FPGA | Actel | A1280 | MULTIPLE ENTRIES | | | |
| FPGA | Actel | A1425A | SAAB, ESA | 1999-01-19 | | PDF |
| FPGA | Actel | A1460A | MULTIPLE ENTRIES | | | |
| FPGA | Actel | A14100A | MULTIPLE ENTRIES | | | |
| FPGA | Actel | A321400X | SAAB, ESA | 1997-10-01 | | PDF PDF |
| FPGA | Actel | RH1280 | MULTIPLE ENTRIES | | | |
| FPGA | Actel | RT545X32-Series | MULTIPLE ENTRIES | | | |
| FPGA | Lattice | ispLST5384 | SAAB, ESA | 2001-08-23 | | PDF |
| FPGA | Lucent | OR2C06A | SAAB, ESA | 2001-08-23 | | PDF |
| FPGA | Quick Logic | QL4090 | SAAB, ESA | 2001-08-23 | | PDF |
| FPGA | Actel | RT545X16 Series | MULTIPLE ENTRIES | | | |
| FPGA | Xilinx | XQR2V3000 | SAAB, ESA | 2004-11-22 | | PDF |
| FPGA | Xilinx | XQVR300 | MULTIPLE ENTRIES | | | |

Past-Current FPGA activities: Atmel

- Recognizing the value of FPGA technology for space systems and aware that final product confidence depends on a close partnership with the manufacturer, CNES and ESA are supporting the development and ESCC (European Space Components Coordination) qualification of European SRAM based FPGA types
- AT40K reprogrammable rad-hard FPGA available since 2004.
- Used in a few ESA and European space industry developments.
- ESA was also first user, helping to debug/improve the Design Kit.

Past-Current FPGA activities: Xilinx

- **Radiation tests on XQR2V3000; conclusions for designs:**
 - May be usable for “non-critical” designs
 - XTMR and continuous scrubbing required
 - SEFI Detection and/or Watch Dog Circuitry
 - Clocking of TCK input + ground TRST (avoid JTAG SEFI)

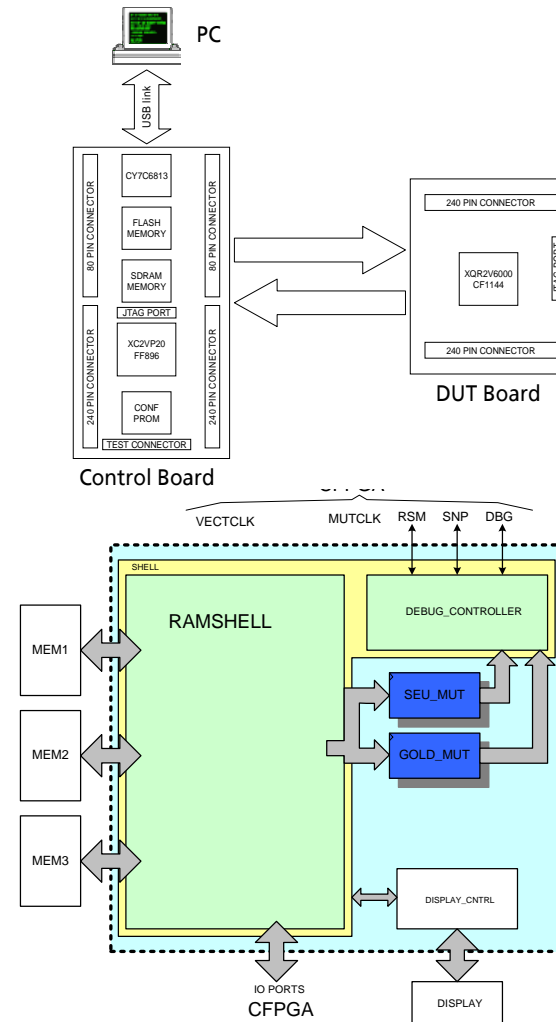
- **ESA is member of the European Xilinx SEE Consortium,**
 - Periodic multiparty teleconferences
 - Info exchange on rad tests, fault injection & mitigation techniques R&D across various institutes/Agencies.

Past-Current FPGA activities: Xilinx (II)

- Further investigations on the test results of *XQR2V3000* (ongoing):
 - Configuration memory SEUs:
 - Can it be improved by the user? Can STAR and RoRA improve the situation?
 - *STAR/RoRA* tools (from Politecnico di Torino):
 - **STAR**: analyzes the placed and routed circuit to check whether critical areas exist in the configuration memory that may corrupt the correct operations of the TMR architecture when affected by SEUs
 - preliminary assessment of STAR (paper at NSREC'07)
 - **RoRA**: routing with extra constraints to overcome potential critical areas revealed by STAR

Past-Current FPGA activities: Xilinx (III)

- FLIPPER fault injection system (from IASF Milano) addressing the **Xilinx configuration memory** being used to investigate the results of STAR/RoRA, and XTMR
- FT-UNSHADES fault injection system (from University of Seville) used to validate effectiveness against SEU of the XTMR and other hard-by-design implementations of **the user's design**



Past-Current FPGA activities: Actel

- A **European independent evaluation** of FPGAs subject to **ITAR**+vendor know-how restrictions (technology details not shared) **appears impractical** and efforts outbalance the expected results.
- European users appreciate very much the very open information policy of the US teams
- **ESA Policy for one-time-programmable FPGAs (ongoing):**
 - **Post-Programming screening (incl. dynamic burn-in):**
 - **Motivation:** Antifuse-based FPGAs do suffer a physical change at their programming stage, which can therefore be considered as the last fabrication stage. There is therefore need to have a screening to ensure high reliability of final programmed device
 - **associated difficulties and limitations duly noted (sockets, inducing unwanted failure mechanism/s, high costs...)**
 - **Several European test-houses have been contacted for a possible generic PPBI set-up for Actel**

Future activities: summary (I)

- **European reprogrammable rad hard FPGA**
 - ESA is involved in European reprogrammable FPGA developments with CNES and Atmel for the AT280 devices and beyond
 - On-going efforts to define and raise funding for a future large (1-2Mgates) European reprogrammable rad hard FPGA
- **Radiation Testing of Reprogrammable Flash-based technologies: ACTEL ProASIC3 family**
 - Motivation: the current good radiation results recently shown, power consumption and the re-programmability capabilities
 - Test setup and test vehicle are currently under definition
 - Collaboration at different levels is expected and very welcome from other groups

Future activities: summary (II)

- **Evaluation of new FPGA technologies (hardened-SRAM, Flash, mixed-signal).**
 - Functional and performance evaluation of new FPGA technologies and design kits (benchmarking)
 - Main first target: AT280E European FPGA.
 - Setup and test vehicles under definition:
 - basic structures and application- representative designs based on mapping typical space IP functions
 - easy porting to a radiation test environment will be pursued
- **Xilinx Radiation Test results & mitigation**
 - Investigation with the tools for rad protection/analysis (XTMR; STAR/RoRA; FLIPPER; FT-UNSHADES) will continue (based on Virtex-II)
 - ESA will continue being a member of the European SEE Consortium

Future activities: summary (III)

- **TID characterization of power-up behaviour for FPGAs.**
 - Characterize Atmel's AT40KE and AT280 FPGAs and Actel AX2000 (RT or non-RT) power-up behaviour as a function of cumulated dose
- **Development of standard test methods for Single Event Transient characterisation in CMOS using FPGA as test vehicle**
 - Development and verification of a standard test method (based on FPGA) for characterization of Single Event Transients (SET) in CMOS ASICs and FPGAs
- **Reliability assessment of reconfigurable FPGAs in Space Projects**
 - evaluate the susceptibility and impact of the different reliability failure mechanisms on a variety of commercially available, state-of-the-art reprogrammable FPGAs. At the completion of the activity the European space community shall be provided with sufficient data to perform a profound risk assessment when using reprogrammable FPGAs in their projects.
- **Reconfigurable payload demonstrators based on SRAM-FPGA**
 - Pursuing on-board reconfiguration to satisfy different needs: error correction and processing algorithm upgrades to extend mission life and mission services. Focus on SW-defined radio telecom applications.

FPGA usage in European Missions

- **Short recent history**

- **2001-02: the first extensive FPGA audits on ESA missions were done (e.g. Rosetta, SMART-1, Mars Express) => design and verification methods were to be improved, go ASIC-like. Tens of FPGAs used in payloads and platform. Mostly ACTEL.**
- **2004/5: Actel anti-fuse problems triggered a thorough FPGA recount and reliability assessment in all ESA projects (Herschell-Planck, VenusX, Aeolus, Cryosat, Galileo, GOCE, SMOS) . Up to hundreds of FPGAs found in platform and payloads. Case-by-case decisions on replacing MEC by UMC. Additional in-system test hours to minimize early-life failures.**

FPGA usage in European Missions

- **The use of FPGAs in European Missions is growing**
 - **New missions like ATV, Proba2, GAIA, BepiColombo, GMES Sentinels will use large amount of FPGAs, mostly ACTEL.**
 - **Proba2 will be the first ESA mission to fly RTAX**
 - **The fairly new Actel RTAX is extensively used or considered for all new missions under development:**
 - **Different approaches have been adopted to address the Post-Programming screening; ranging from no- screening to pseudo-dynamic PPBI**

FPGA usage in European Missions

- **The use of FPGAs in European Missions is growing (cont.)**
 - **Re-programmable FPGAs (Xilinx, Lattice) are used in very small quantities, normally in non-critical payload instruments (cameras, star-trackers).**
 - **Venus Express is flying a camera with LEON2 in Xilinx, applying all known mitigation techniques. SMART-1 and Proba1 are flying StarTrackers which use Lattice.**
 - **Other ESA missions which will fly reprogrammable FPGAs are Proba2, ATV, GOCE. None of them is actually exploiting the re-configurability capabilities to do on-board ground-controlled functional upgrades.**

Conclusions

- **A European independent evaluation of FPGAs subject to ITAR+vendor know-how restrictions (technology details not shared) appears impractical and efforts outbalance the expected results.**
- **CNES and ESA are supporting the development and ESCC qualification of European SRAM based FPGA types**
- **ESA has a planning of activities to assess new FPGA technologies in order to anticipate policies / recommendations on their usage**
- **Feedback and cooperation from FPGA users is important: ESA is setting the bases for a space FPGA users' Working Group, to centralise experience, find solutions and have lessons learned.**