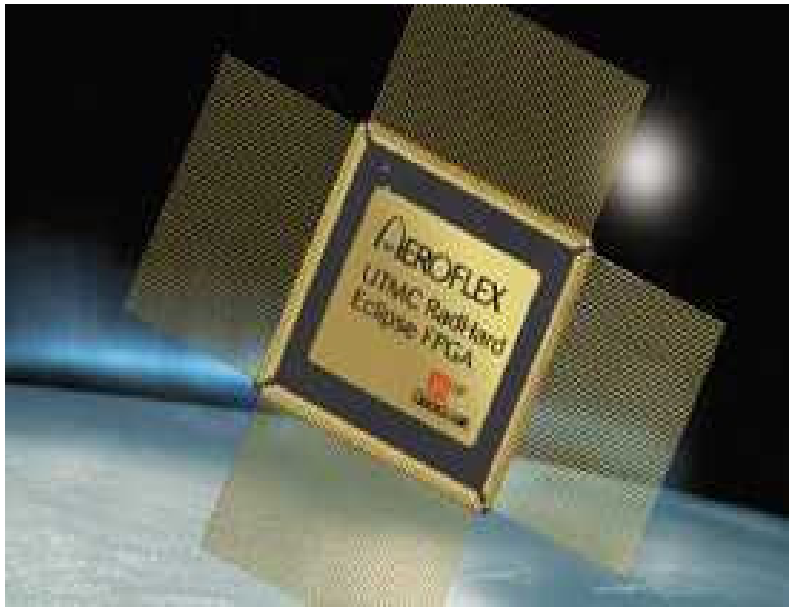
RadHard Eclipse Reliability Update

Aeroflex – Colorado Springs

Agenda

- HTOL / LTOL AC Trends
- Reliability Characterization Vehicles (REL4 and REL5)
- Improved ViaLink Perceptivity
- ViaLink Programming Distribution
- Programming Pulse Experiment
- ViaLink Trends with Hi-Rel Algorithm
- Summary / Conclusions

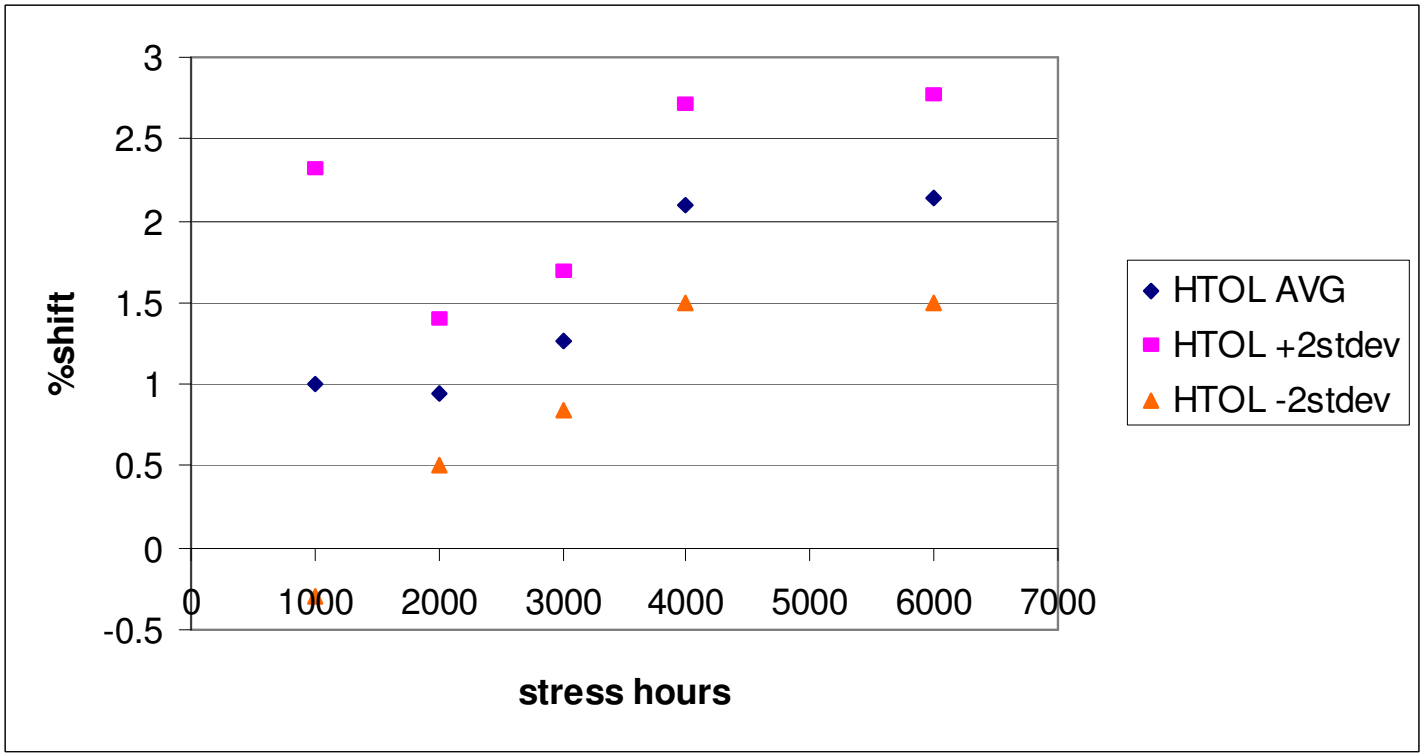


HTOL \ LTOL AC Trends

- Previous Reliability Work: AC Delay Deltas
  - Extended life stress has been used by Aeroflex to evaluate device and ViaLink behavior over time
  - Review of AC delay shifts on long inverter chains through 6000h show less than 5% delay deltas on HTOL, and less than 1% delay deltas on LTOL
  - This supports the position that standard CMOS mechanisms (charge trapping, oxide leakage) are the major cause of AC delay change, not ViaLink aging

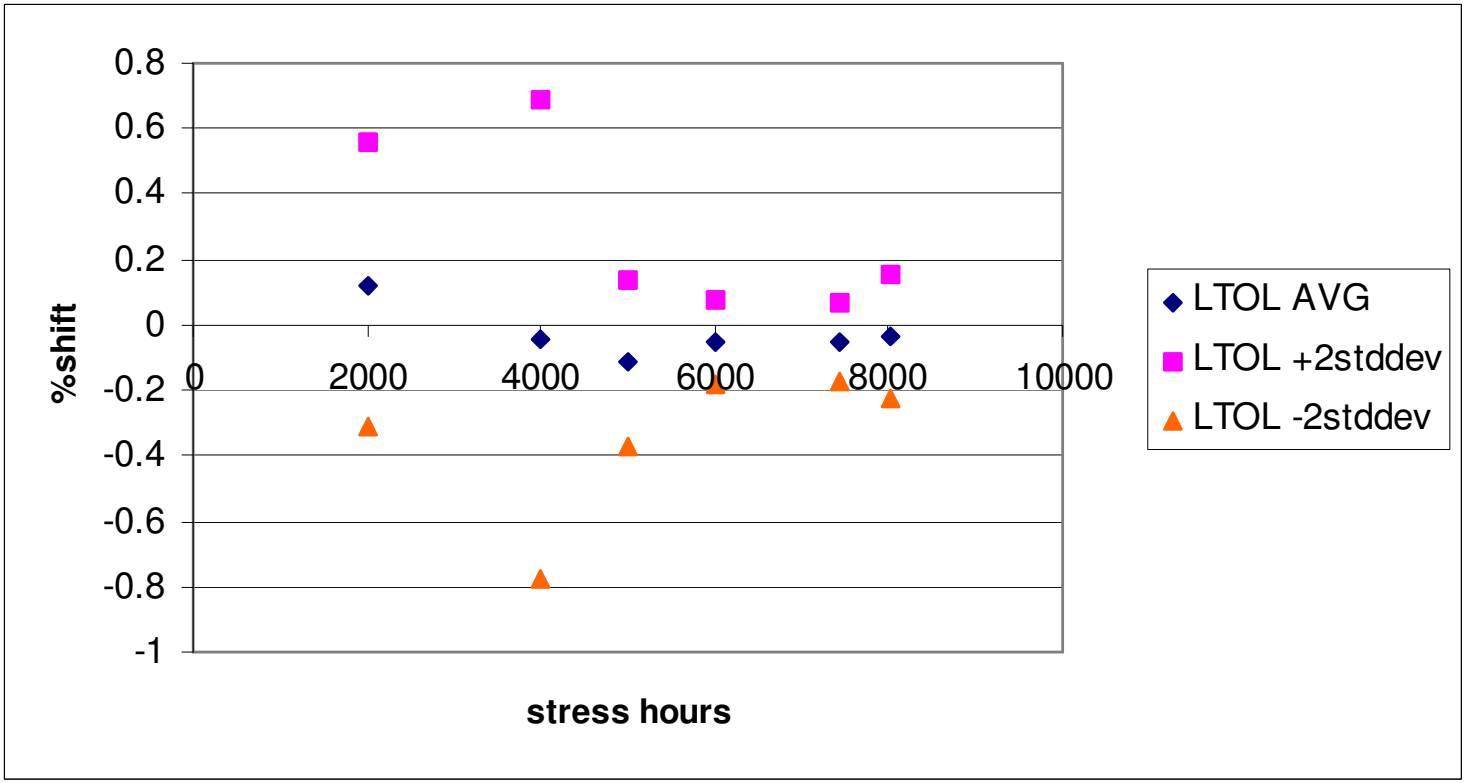
HTOL \ LTOL Trends

- Lot QL0882 inverter chain delay through HTOL stress
  - 50 units, 251 gate NAND inverter, time 0 absolute delay 150ns



HTOL \ LTOL Trends

- Lot QL0882 inverter chain delay through LTOL stress
  - 48 units, 251 gate NAND inverter time 0 absolute delay 150ns



Aeroflex Enhanced Reliability Analysis

- **Previous reliability work emphasized catastrophic failure mechanisms**
  - **Maximum use of ViaLinks**
  - **Long, heavily loaded delay chains**
  - **Testing looked for significant AC delay shifts or current consumption**
- **Current work focuses on individual ViaLinks**
  - **New reliability vehicle (REL4) created to allow perceptivity into small groups of ViaLinks**
  - **Second reliability vehicle (REL5) created to maximize ac current flow through ViaLinks**
  - **Techniques developed to measure current flow through individual ViaLink networks (ReadLink)**
  - **Individual ViaLinks analyzed for out-of-family behavior after baseline programming and after HTOL / LTOL stress cycles**

AC Test Comparison: REL3 vs REL4

REL3 Delay Measurements

Path Type	# Tests
Clock to Q (shift registers, SRAM blocks)	76
Combinatorial measurements (11 logic elements)	30
Combinatorial measurements (251 logic elements)	6
Total	112

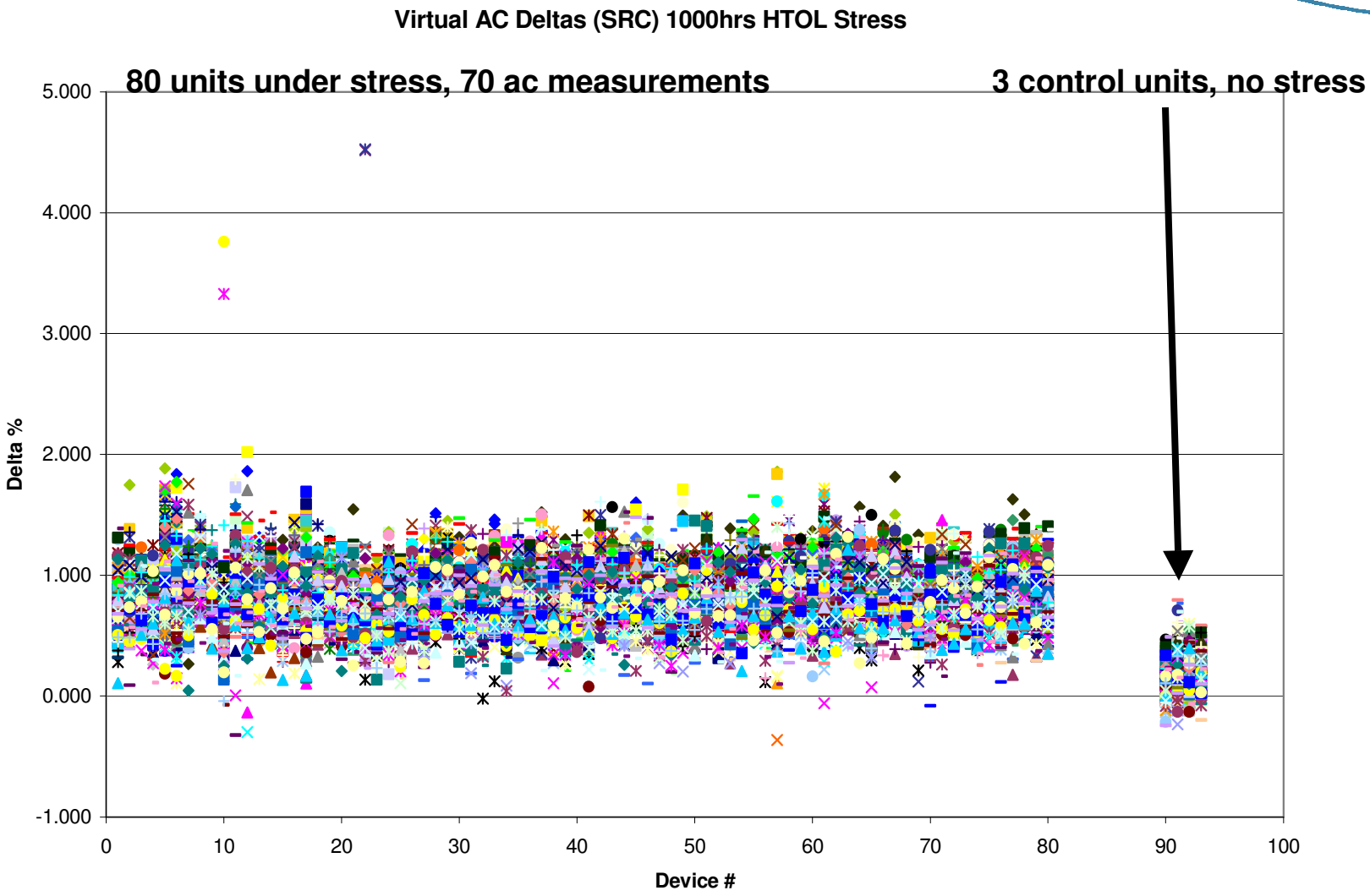
REL4 Delay Measurements

Path Type	# Tests
Clock to Q (shift registers, cascading registers, SRAM blocks)	104
Input to Output (combinatorial blocks, cascading registers)	84
Redundant Input to Output (multiplexor outputs)	78
Combinatorial sub-path measurements (10 logic elements) (combo, cascade reg.)	290
Combinatorial sub-path measurements (50 logic elements) (combinatorial)	22
Combinatorial path measurements (100 logic elements) (combinatorial)	4
Frequency measurements (oscillator, counters, shift registers)	11
Total	593

Improved Perceptivity w/ REL4 Structures

Path Structure	# Elements	Typical Value	Path Perceptivity (ps per % Delta)
"A" Mux Chain	100	180.0 ns	1800
"B" Mux Chain	100	225.0 ns	2250
"C" Mux Chain	100	305.0 ns	3050
"D" Mux Chain	100	370.0 ns	3700
XOR Chain	550	475.0 ns	4750
NAND Tree	100	75.0 ns	750
Cascading SR Chain	100	185.0 ns	1850
"A" Mux Sub-Chain	10	15.0 ns	150
"B" Mux Sub-Chain	10	20.0 ns	200
"C" Mux Sub-Chain	10	30.0 ns	300
"D" Mux Sub-Chain	10	35.0 ns	350
XOR Sub-Chain	50	85.0 ns	850
Cascading SR Sub-Chain	10	18.0 ns	180
Counter Frequency	8	140 MHz	72
"A" Shift Register	100	195 MHz	52
"B" Shift Register	100	180 MHz	56

REL4 HTOL % Shift from Baseline : Original Programming Algorithm

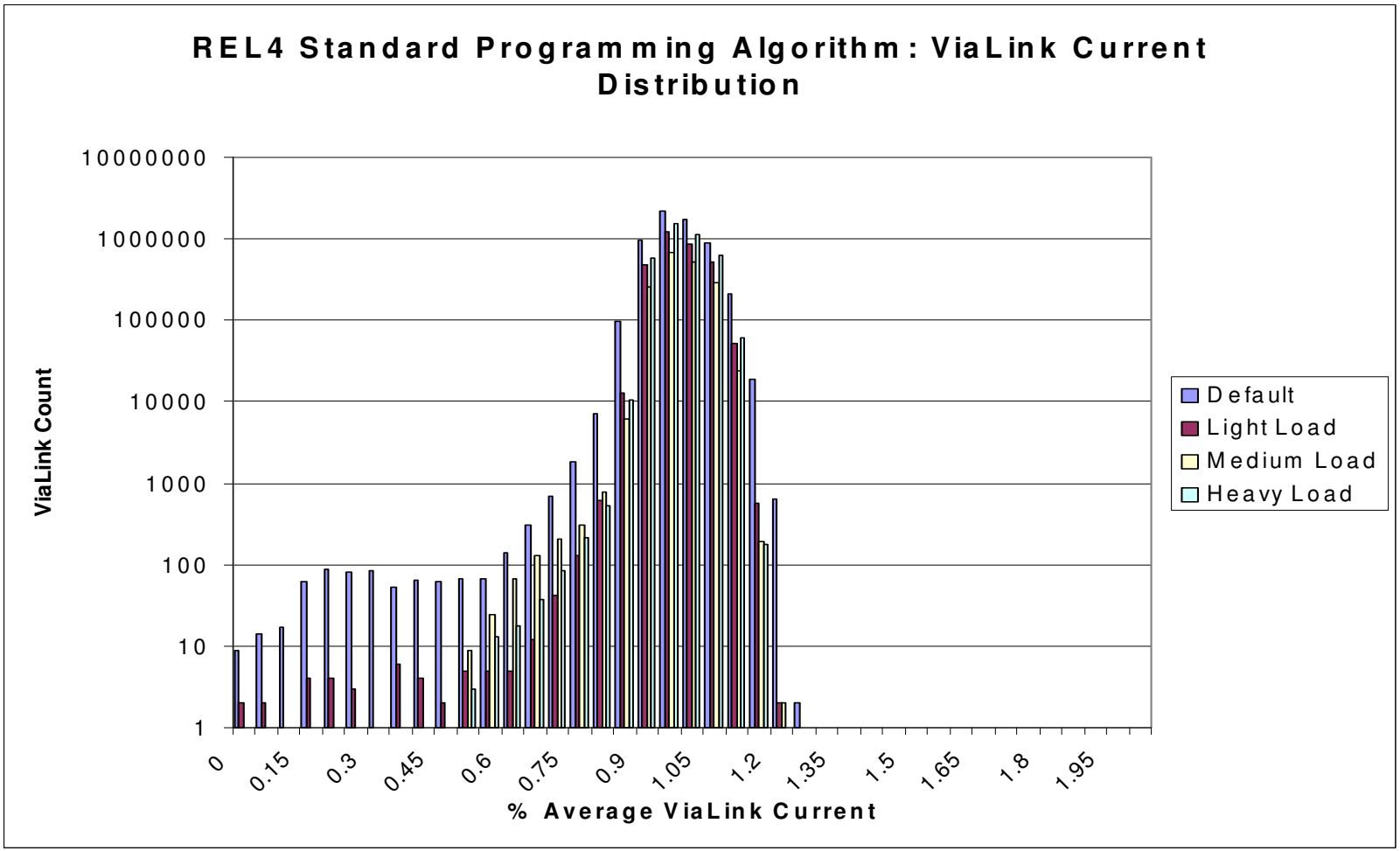


ViaLink Resistivity Analysis

- Aeroflex has developed techniques to monitor current flow through individual ViaLink networks (ReadLink)
  - Currently use System General Programmer
  - Tester provides improved accuracy & repeatability
- Current techniques look for “out of family” characteristics when evaluated across group of devices
  - Compare individual ViaLink behavior across family of devices during programming baseline
  - Compare ViaLink delta behavior after HTOL / LTOL stress cycles
- Results used to improve ViaLink consistency

ViaLink Current Distributions

- Standard commercial programming algorithm allows multiple programming pulse options
- Programming pulse polarity and count determined by capacitive load on net

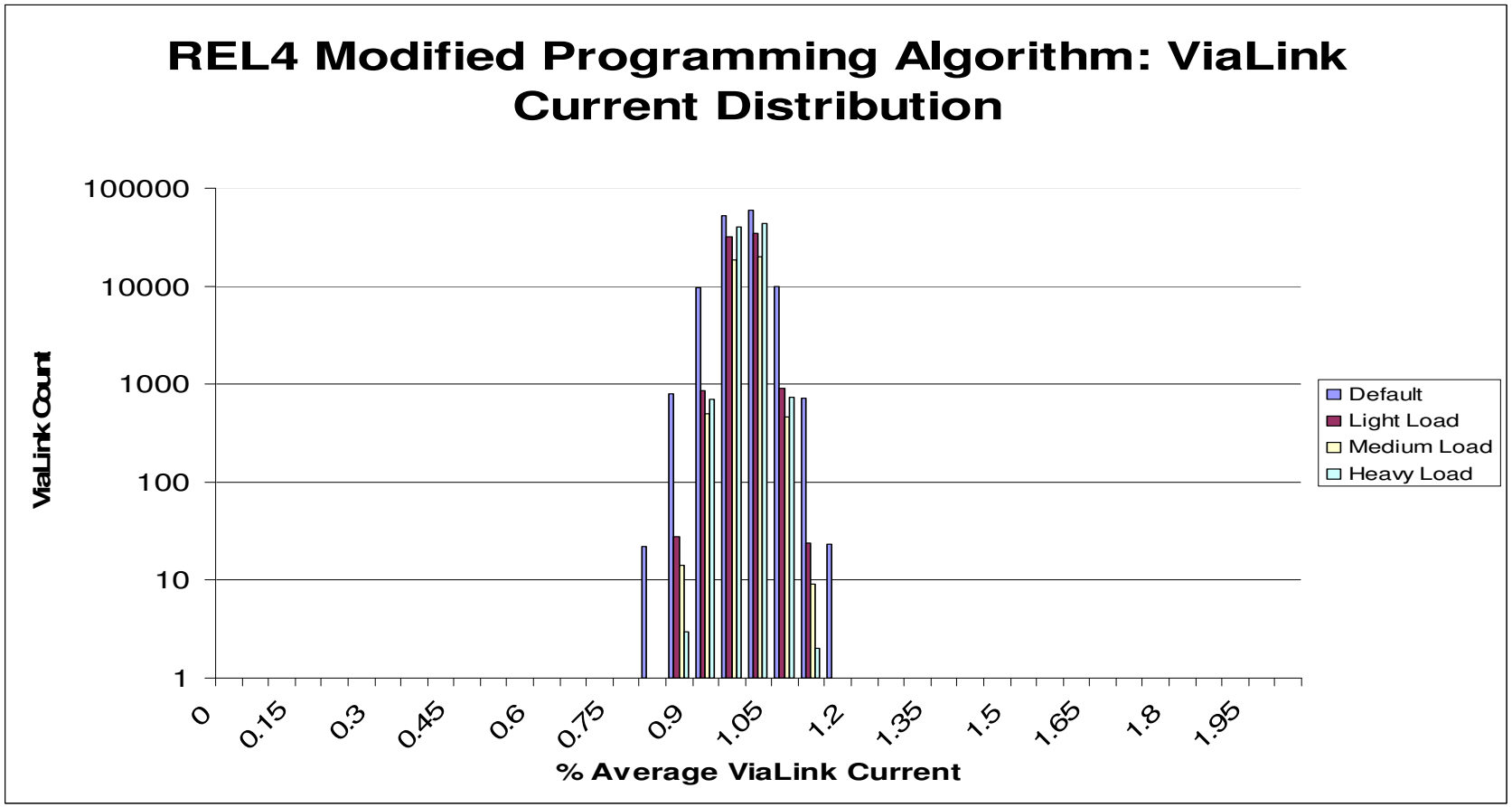


Programming Pulse Experiment

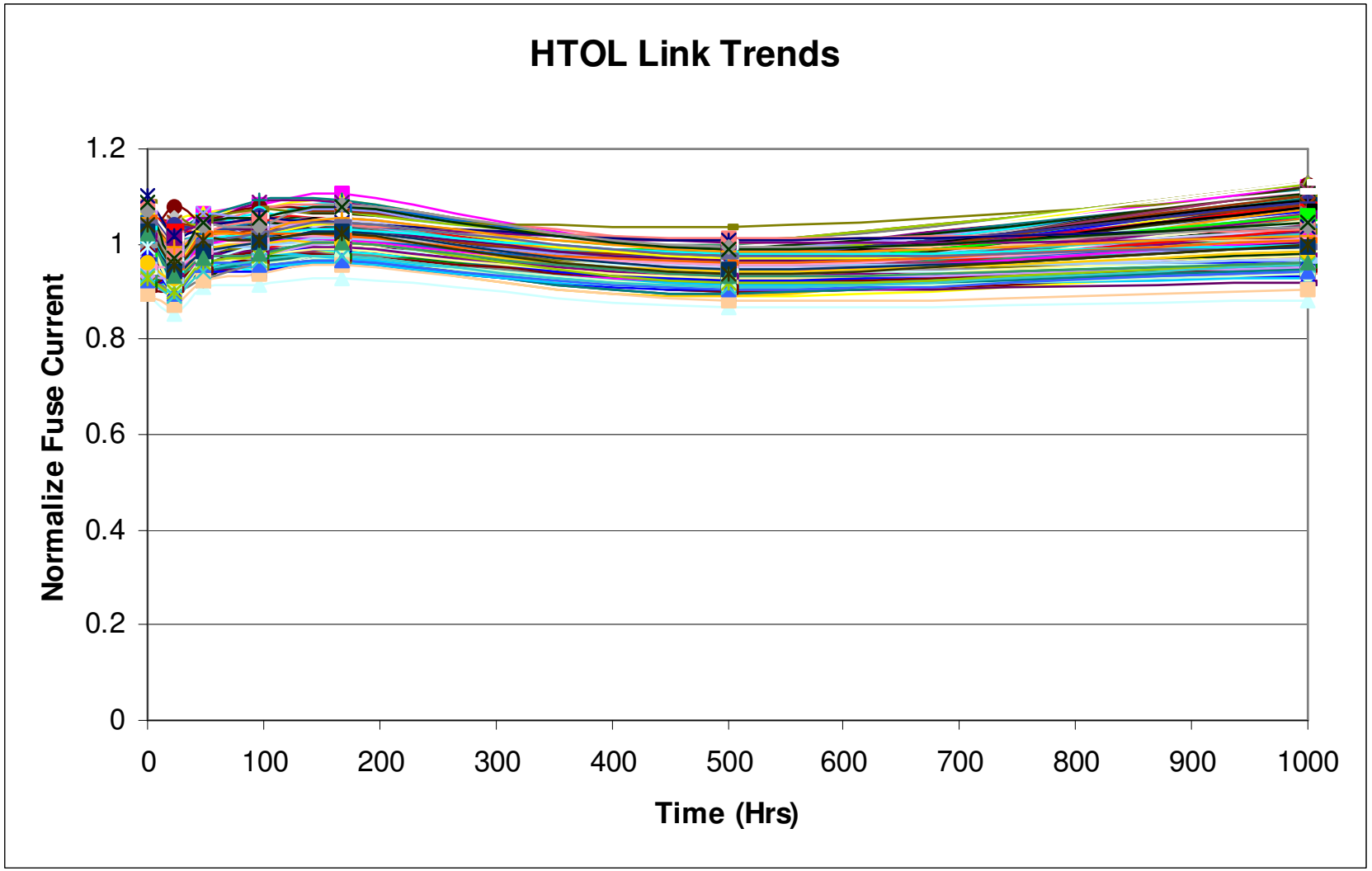
- Analysis of individual ViaLinks identified opportunity to improve consistency in ViaLink programming
- Reliability devices programmed with “lightly” programmed ViaLink on global clock shift register
- Baseline ReadLink measurement 0.96mA (vs lot average 1.83mA)
- Maximum frequency baseline for global clock shift register > 200MHz
- 1000 hr HTOL stress applied to lot including weakly programmed unit
- “Normal” devices in lot experience minimal change
- “Lightly” programmed device experiences significant shift
  - ReadLink current measurement 0.36mA
  - Maximum frequency measurement on global clock shift register = 171MHz
- Single ViaLink “healed” by single additional programming pulse
  - ReadLink current measurement 1.65mA
  - Maximum frequency measurement on global clock shift register > 200MHz

ViaLink Current Distributions

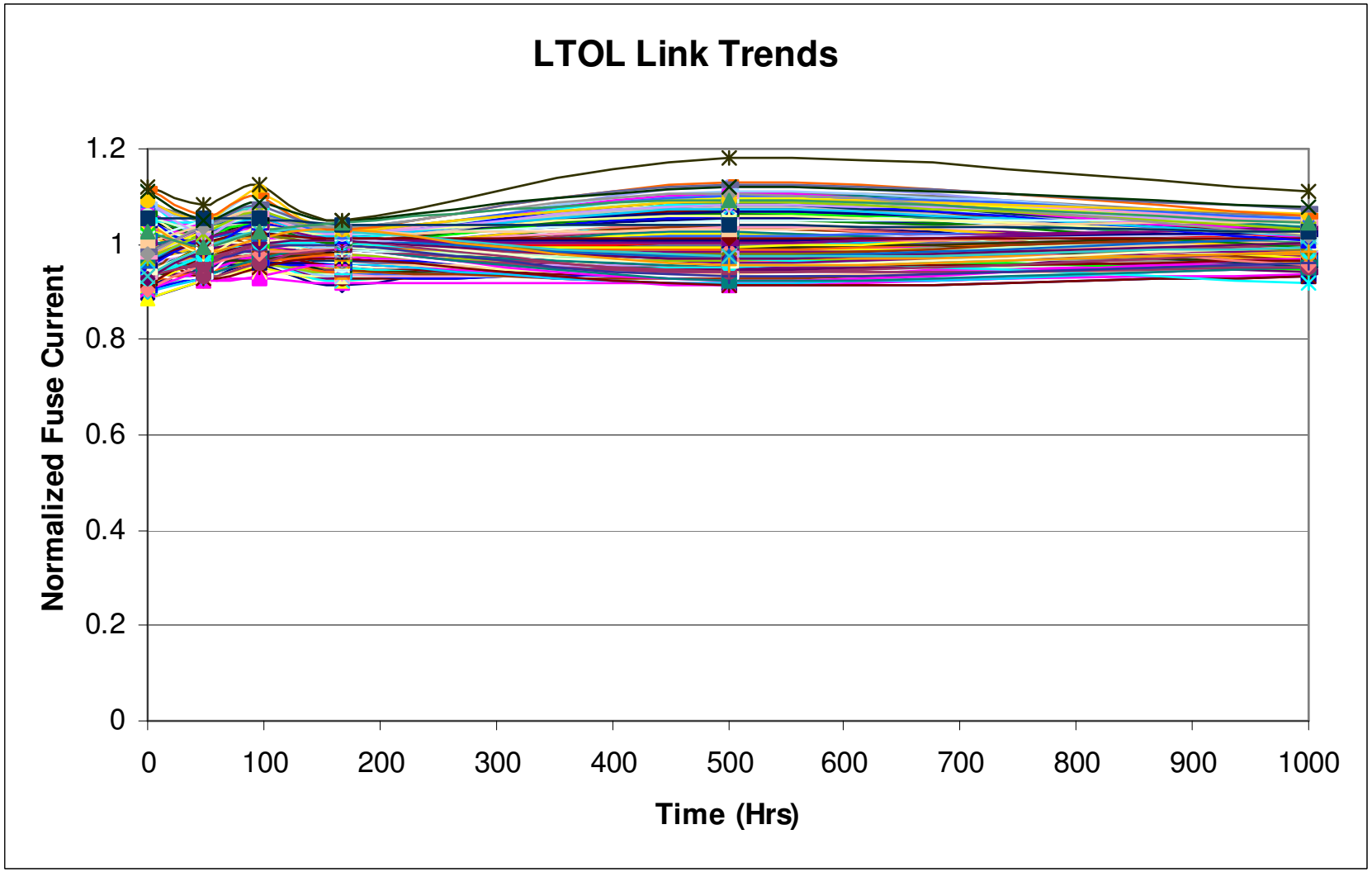
- Hi-Rel algorithm reduces programming pulse options
- Programming pulse waveform, amplitude and duration are unchanged
- Programming pulse count increased



REL4 HTOL ViaLink Trends w/ Hi-Rel Algorithm



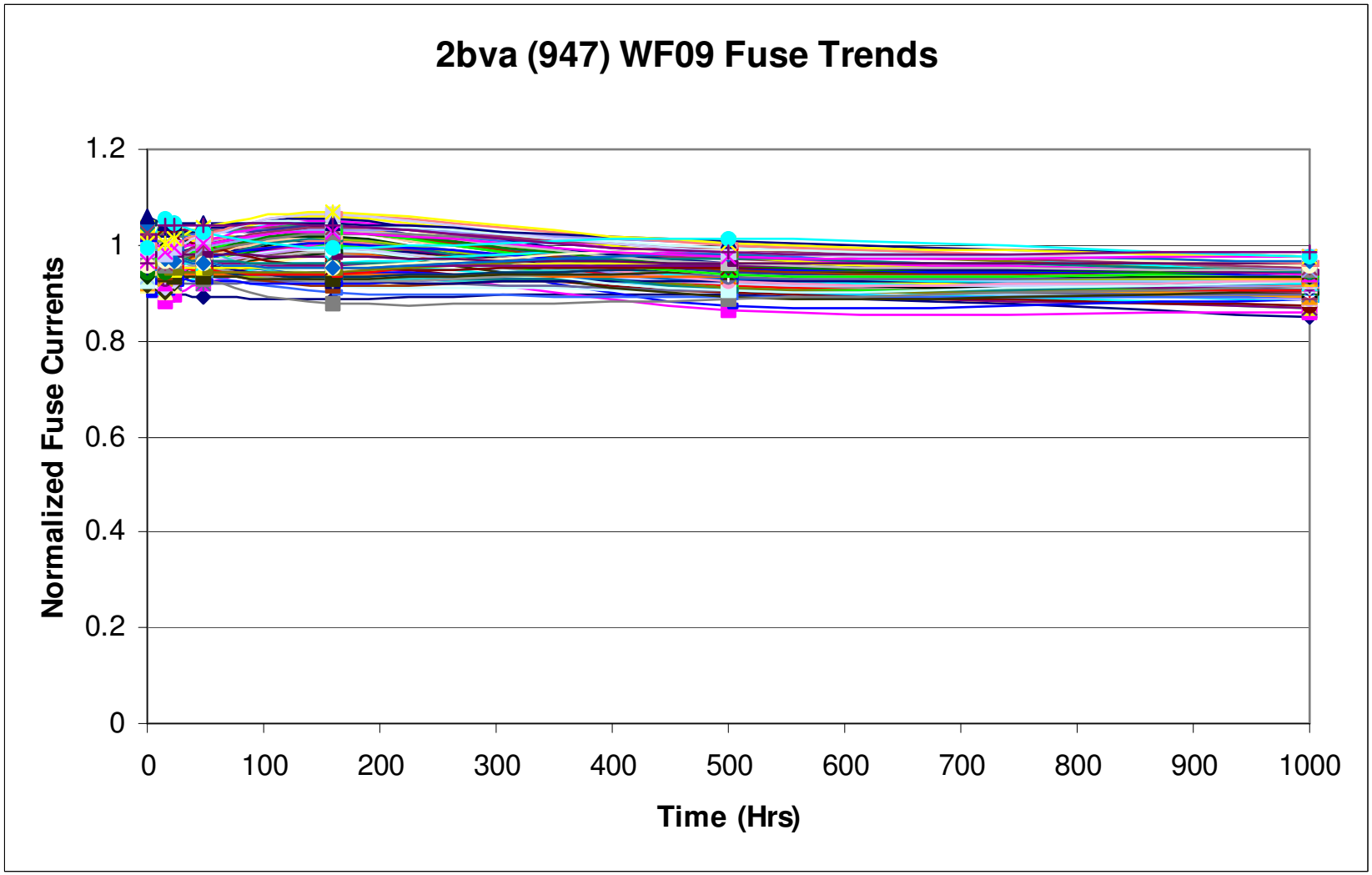
REL4 LTOL ViaLink Trends w/ Hi-Rel Algorithm



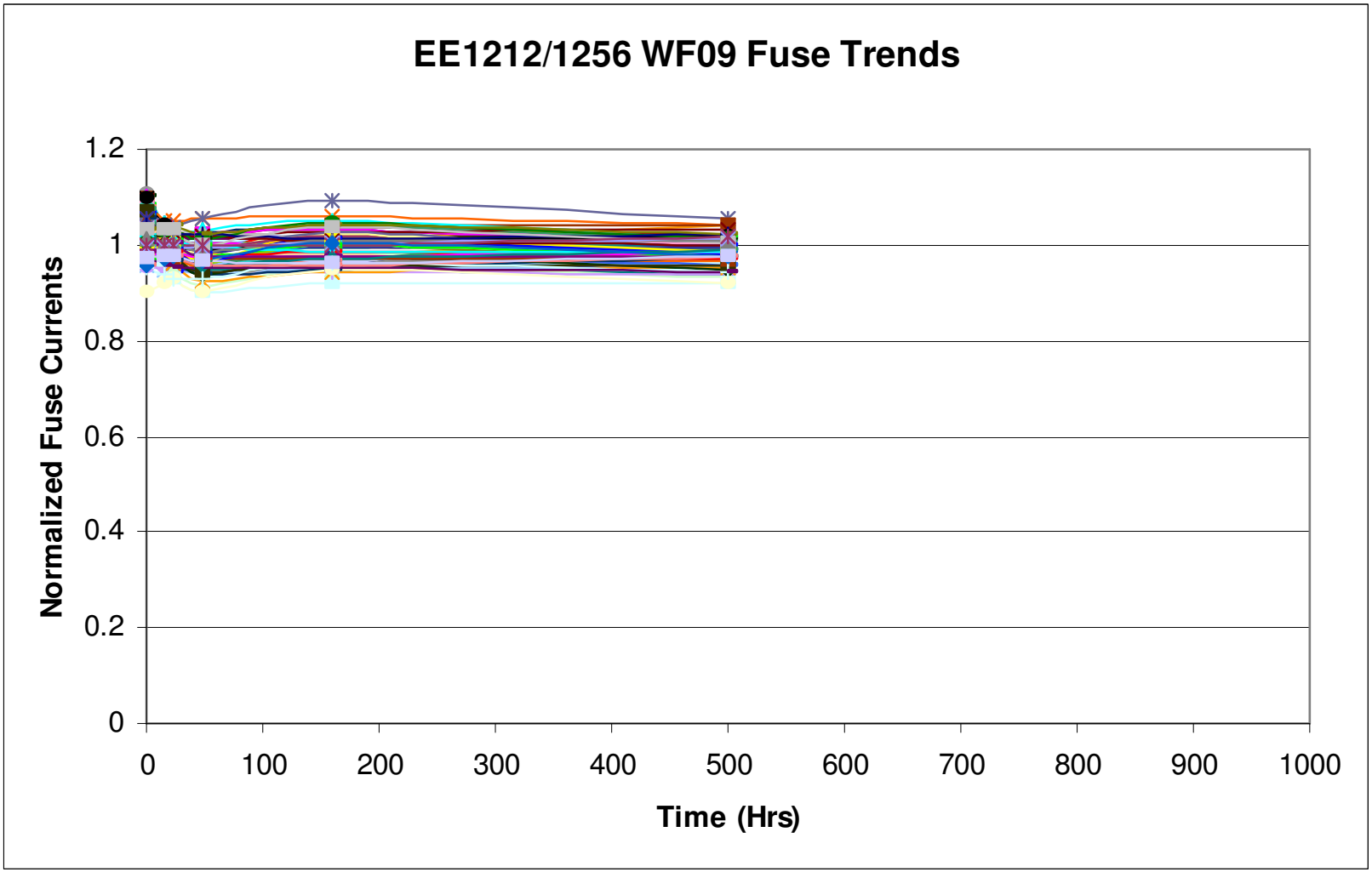
High Current Flow Reliability Analysis

- **Second reliability vehicle created to maximize current flow through ViaLinks**
  - Six, free running oscillators created
  - Three “fast oscillators” run at 200 – 270MHz
  - Three “slow oscillators” run at 100 – 150MHz
  - Loading on oscillator stages varies from 1 to 20 input loads
- **Oscillator design run at frequency in HTOL / LTOL stress chambers**
  - Material from 2 separate wafer lots used
  - Hi-Rel programming algorithm used
  - ViaLink resistivity (current flow) analyzed at multiple read points: baseline, 24hr, 50hr, 168hr, 500hr and 1000hr
  - No evidence of ViaLink degradation seen

REL5 HTOL ViaLink Trends with New Algorithm



REL5 HTOL ViaLink Trends with New Algorithm



Summary

- Material from four separate wafer lots currently undergoing long term stress
  - Three lots programmed with REL3
  - One lot programmed with REL4 and REL5
- Improved designs and enhanced analysis techniques improve perceptivity into ViaLink behavior
- Programming algorithm modified to reduce ViaLink standard deviation
  - Reduces programming options
  - Increases programming pulses to lightly loaded ViaLinks
  - Improves ViaLink programming consistency
  - Fifth wafer lot programmed with REL4 using HiRel programming algorithm
- With new programming algorithm, AC delay is driven by standard CMOS mechanisms not ViaLink