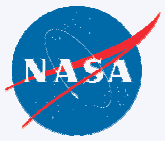

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Monitoring Temperature in SRAM-based FPGAs using a Ring-Oscillator Design

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Overview

- This presentation describes a new method of monitoring and reporting the junction temperature of SRAM-based FPGA.
- The method is based on seven stages ring oscillator programmed in the FPGA.
- The linearity of the ring oscillator combined with the compactness and very small FPGA resource utilization allows the integration of this “thermometer” into the main design.
- Several of these ring oscillators can be placed on the FPGA die to provide the dynamic thermo profile of the entire chip.

FPGAs and Temperature

- Modern FPGAs are very large VLSI devices with millions and millions of transistors. The junction temperatures of these devices can increase to the point of almost instant circuit failure.
- As a result manufacturers are continuing to lower the temperature at which these devices can be operated at.
- This reduction in margin directly reduces the safety margin NASA Missions have.
- The higher the temperature, the quicker the reliability degradation of the FPGA is.
- Almost all degradations mechanisms are enhanced (usually exponentially) with increasing temperature.
- The rise in the temperature of each FPGA is unique, depending upon how many resources are used, what the operating frequency is, etc.

On Board Temperature Measurement

- Our solution is to use a LUT (Look Up Table) based ring oscillator style design.
- Separate logic waveform inversion circuit elements, similar to individual inverters in a normal ring oscillator have been logically defined in VHDL code.
- We then logically connect these separate elements to be able to produce stable reference oscillation frequency.
- This frequency of oscillation is a function of the number of FPGA resources that are consumed and hence it allows us to custom tailor the sensitivity of frequency change to temperature change.

Test Setup

- The test setup consisted of a 12 layers FR4 PCB with two ground planes and two power planes. The socket holding the Virtex-II XC2V3000 UUT positioned in the center of the PCB. All FPGA I/O pins are fanned out.
- The oscillating frequency was measured by a frequency counter and observed on an oscilloscope connected to the corresponding I/O that was assigned to a given ring oscillator and configured as LVTTL. All the transmission lines were made using 3 feet, 50 Ohm Teflon cables.
- The oscillator was manually triggered and timed out (stopped) within a few seconds allowing just enough time to take the reading and minimize self heating of the elements of the oscillator.
- During most of the test the FPGA remained in static operating mode (powered up and idle) for thermal equilibrium conditions for the test.

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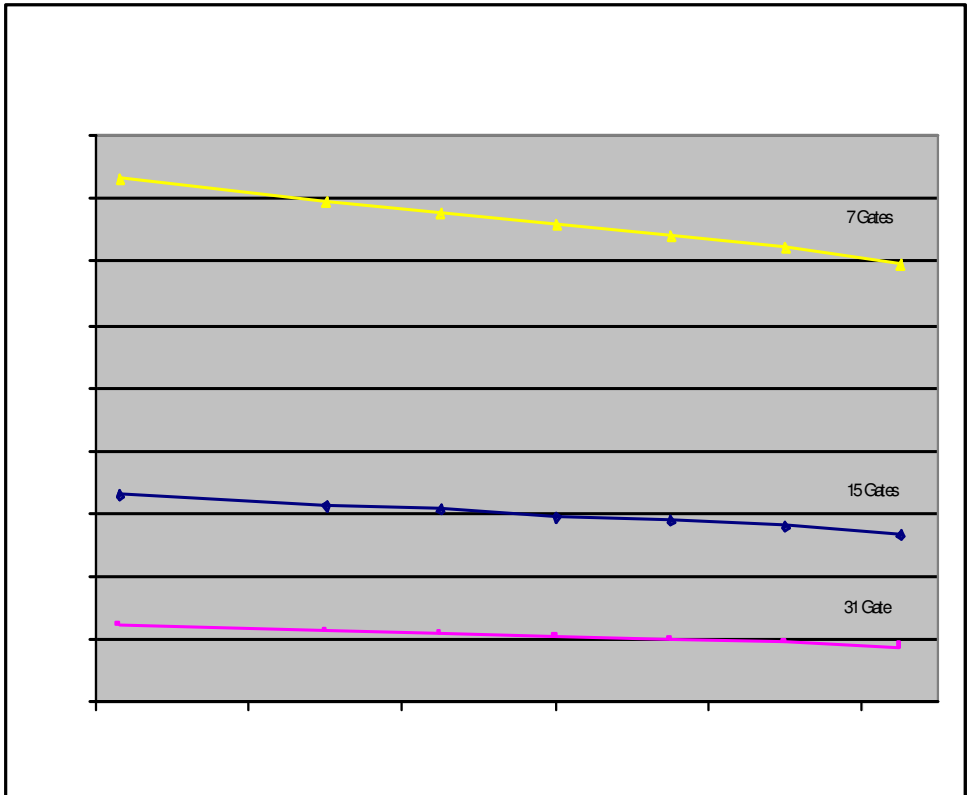
Ring Oscillator Frequency Dependency

- Various length ring oscillators were developed.
- 31, 15, and 7 gate ring oscillators were tested.
- There is a linear dependency between the frequency and the temperature of the junctions for each oscillator.
- There is also linear dependency between frequency and number of gates used in the oscillators.
- The 7 gate design was chosen for further experimentation.



Number of Gates	31	15	7
Slope, kHz/¼C	16.267	31.56	66.667

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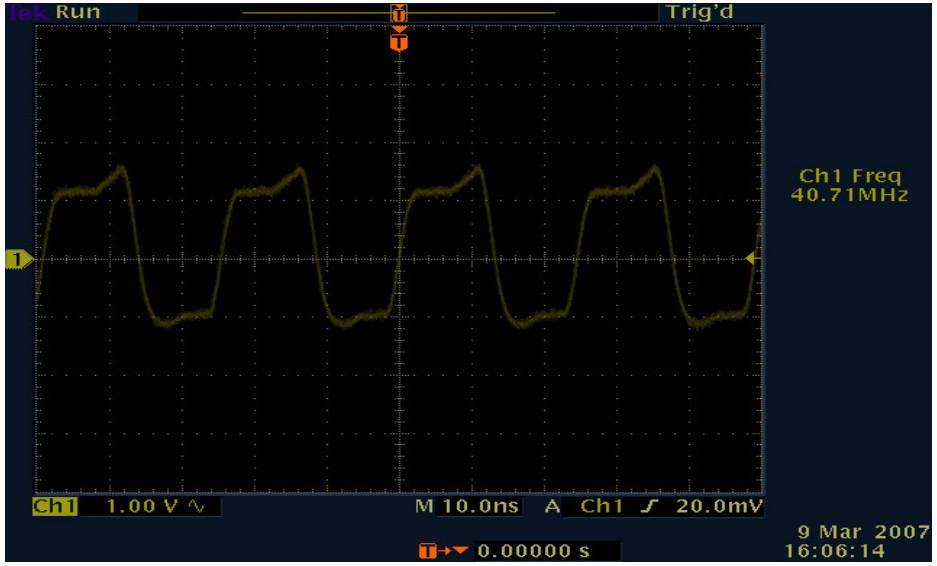
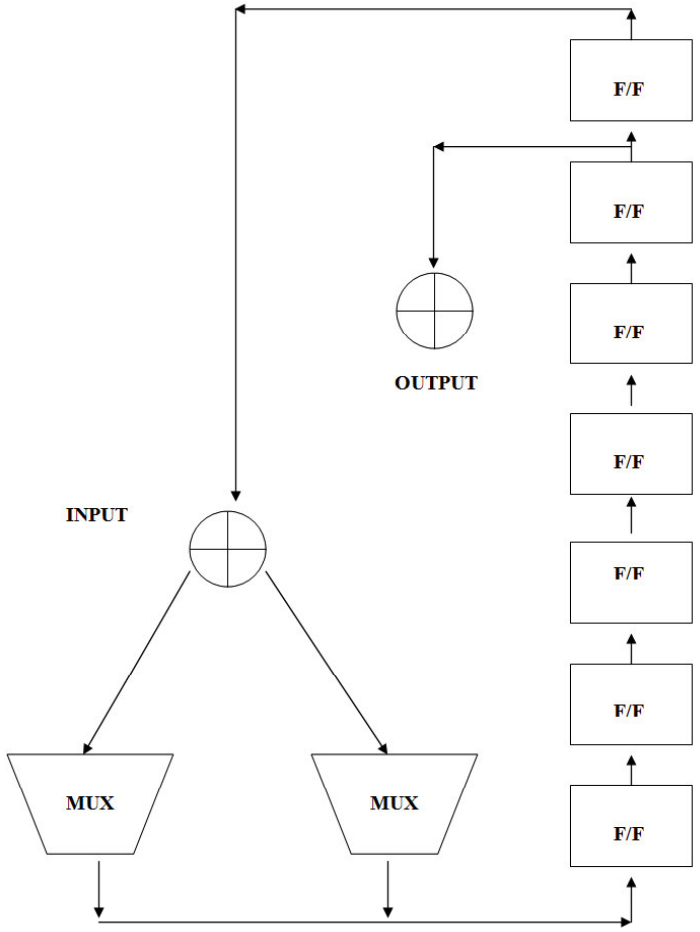
7 Stage Design

- The implementation of 7-stages ring oscillator as it is reported by Xilinx® Integrated Software Environment (ISE™) software





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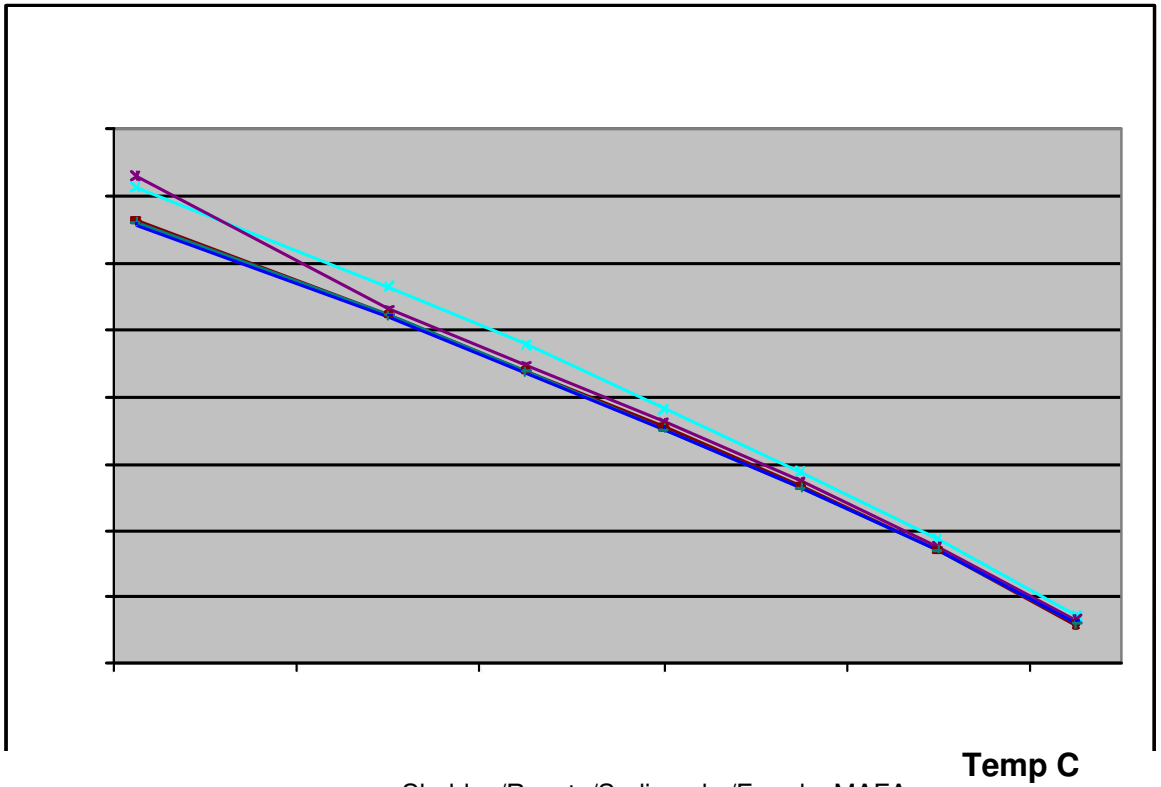
Repeatability

Run #	1	2	3	4	5
Delta Frequency (MHz)	4.93	4.65	4.65	4.62	4.58
Delta Temperature range (125¼C-50¼C=75¼C)	75	75	75	75	75
Slope, kHz/¼C	65.733	62.0	62.0	61.6	61.067



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Repeatability

- The difference between the maximum and minimum slope values is about 4.7 KHz/ºC which represents approximately 7% run-to-run error.
- The behavior of the UUT resembles the process of bake-in, or stabilization i.e. the difference in frequency values for adjacent runs decreases as the number of runs increases.
- Considering the fact that UUT was in a plastic commercial package, the drift seems reasonable.

Temperature, ¼C	Frequency, MHz				
	Run 1	Run 2	Run 3	Run 4	Run 5
50	44.65	44.31	44.23	44.23	44.21
65	43.78	43.47	43.39	43.38	43.34
80	42.82	42.61	42.53	42.51	42.52
95	41.88	41.73	41.65	41.63	41.62
110	40.86	40.75	40.68	40.71	40.69
125	39.72	39.66	39.58	39.61	39.62

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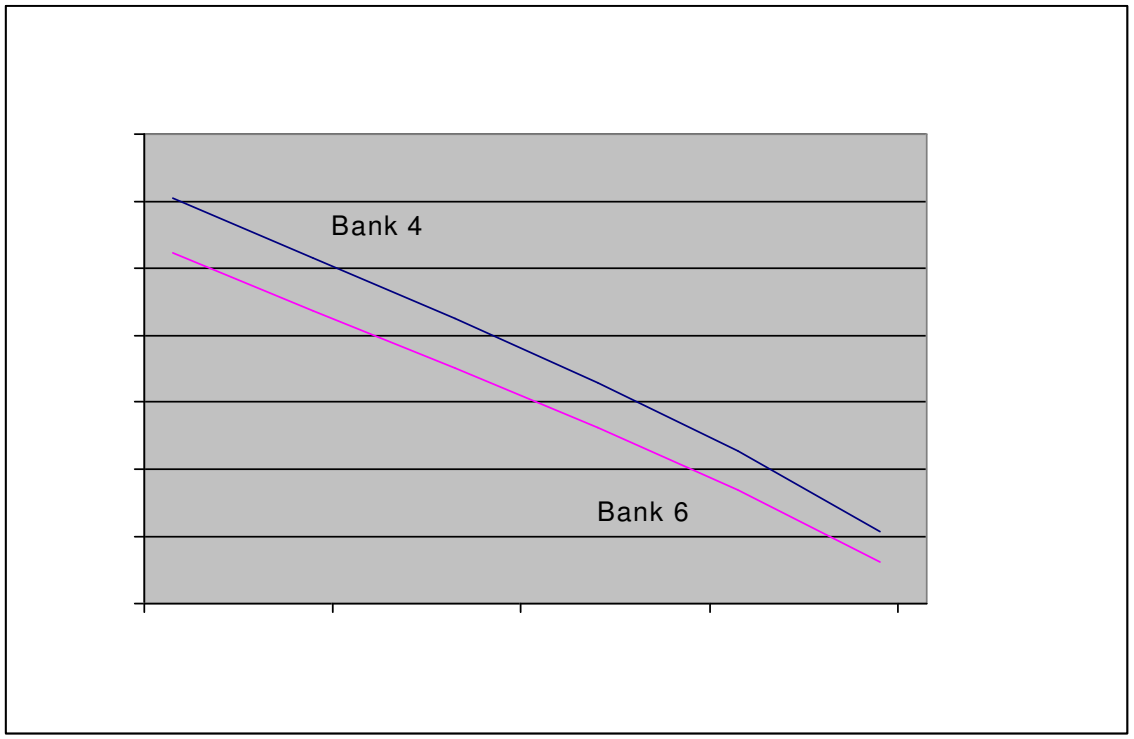
Bank to Bank Variation

- In a practical implementation, it will be desirable to place several ring oscillators/ temperature sensors in different areas of the die
- Graph illustrates the difference in frequency for the same temperature profile with oscillators placed in Banks 4 and 6.
- The difference between corresponding frequencies for banks 4 and 6 starts at 800 KHz for lower temperatures and drops to 400 KHz toward 125ºC.
- Bank-to-bank variations dictate the necessity to calibrate prior to actual temperature readings.



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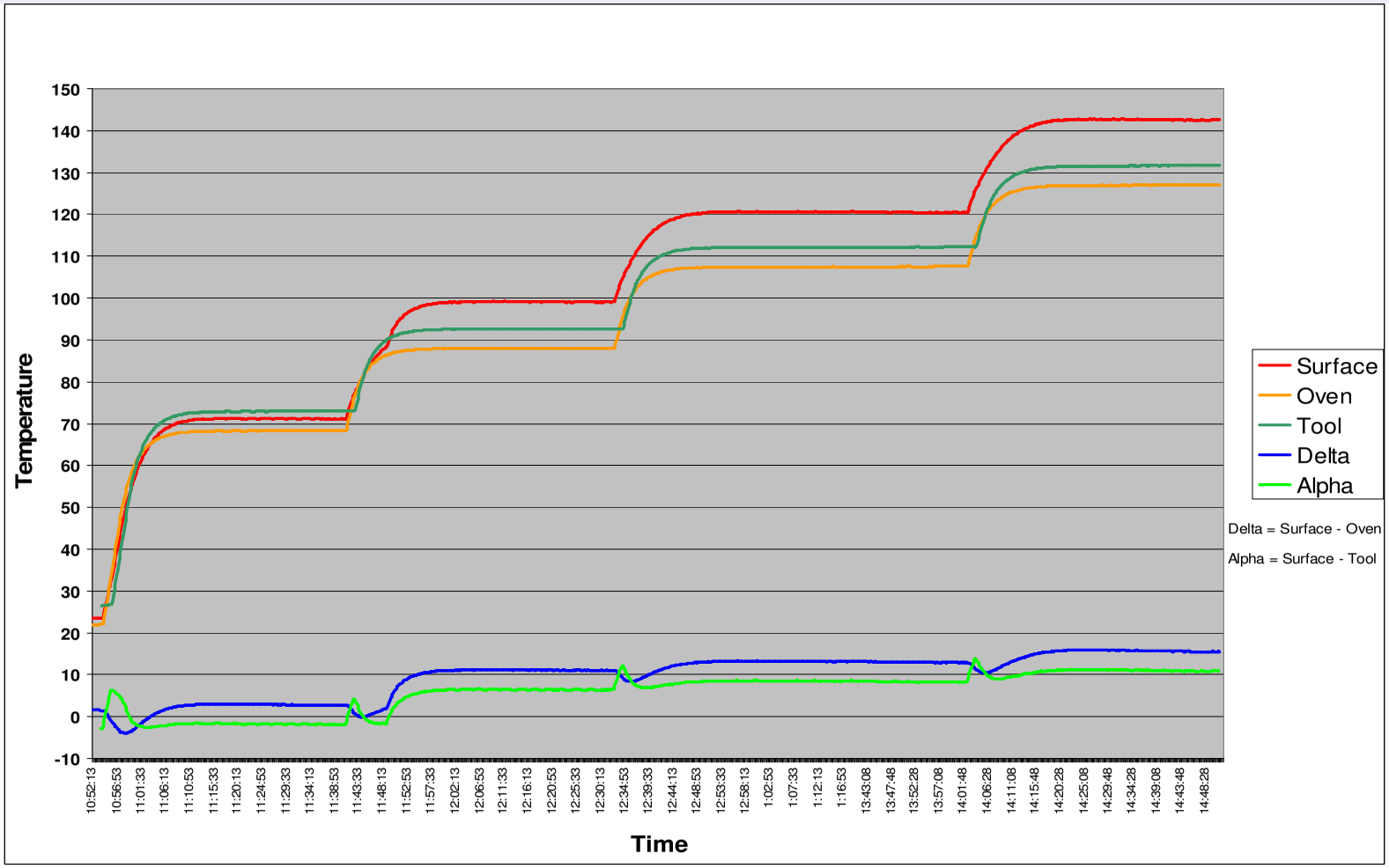
Sample - CRC design as a function of increasing bake temperature



CRC design Temperature Measurements vs. XPower Predictions

Experimental Results

- As the ambient temperature goes up, Delta ($T_{amb} - T_{surf}$) and Alpha ($T_{amb} - T_{tool}$) both increase; However, Xilinx XPower tool predicts Alpha and Delta to have constant values.
- As the ambient temperature (the oven temperature) goes higher than 90 ℃, the Xilinx XPower tool begins under-estimating the case temperature by 6 ℃ (T_{amb} = 90 ℃) to 11 ℃ (T_{amb} = 125 ℃) on the CRC design.
- The ring oscillator design accurately changes frequency from 41.3 to 39.6 kHz.
- The need for accurate on board temperature measurement is critical to accurate FPGA implementation.