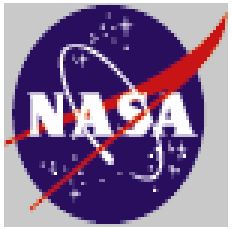

Reliability of FPGA Assemblies Pb/Sn & Pb-free Solders Tested per IPC 9701A

by

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Military and Aerospace FPGA Applications (MAFA) Meeting

November 2007

Outline

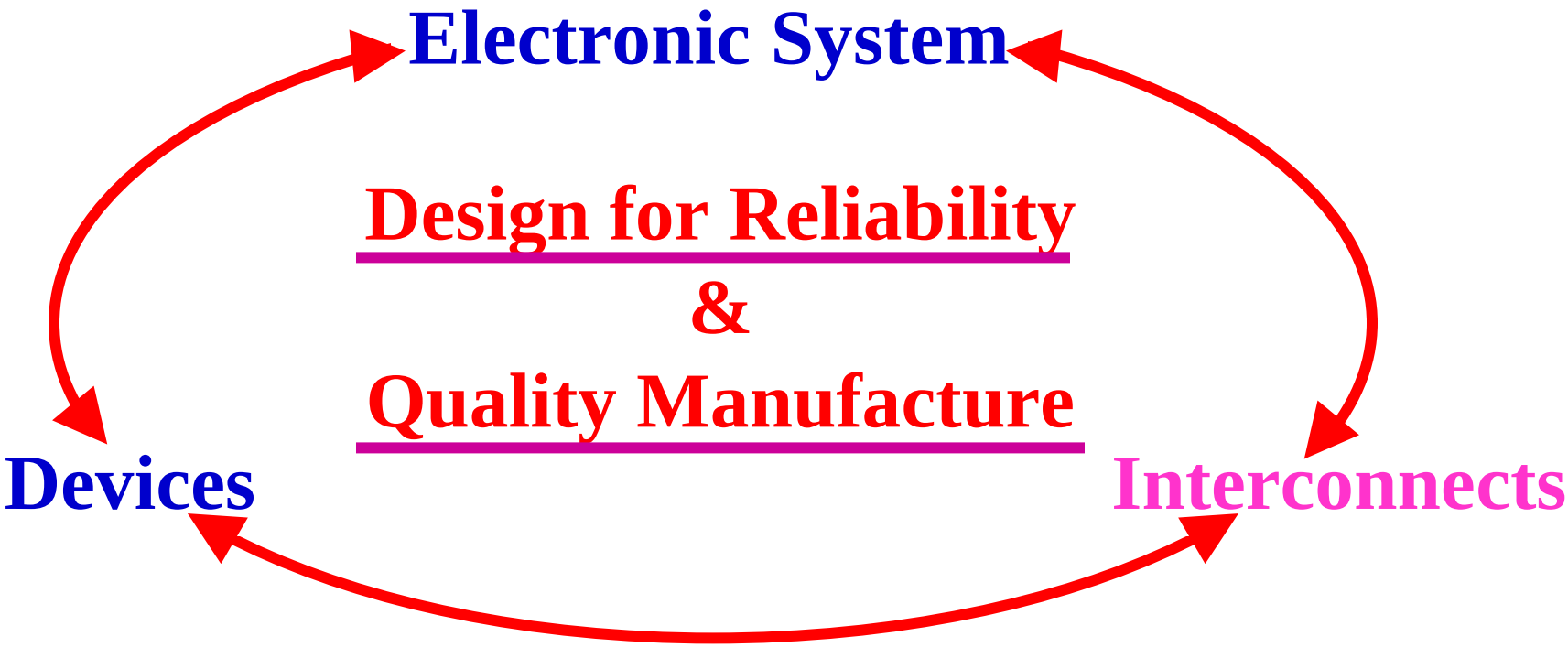
- Reliability
  - Reliability definition
  - IPC 9701A SMT Attachment Reliability
  - Relative thermal cycle data Pb-free/SnPb
- Thermal Cycle Data for PBGA 676 I/O
  - Celestica's test data using RIA3
  - Solectron/industry- effect of dwell time
  - Xilinx
- Why different results using IPC 9701A?
- JPL preliminary data using RIA3 TVs & Future Joint Activities
- Other Current Activities

What is Reliability

JPL

"Reliability is the ability to function as expected
under the expected operating conditions
for an expected time period
without exceeding expected failure levels"

Reliability Threats



Qualification- IPC 9701

- IPC 9701, Released Jan 2002
  - IPC SM785- Guideline
    - No answer to the question of data for product application
    - Data comparison
  - IPC 9701
    - Details on thermal cycle test and acceptance
- Key Controls
  - Surface finish (OSP, HASL), thickness, 93 mil, NSMD, continuous monitoring, etc.
- Five Cycle Conditions
  - Preference 0/100°C
- Five number of thermal cycles
  - Preference 6,000 cycles

IPC 9701- "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments"

IPC 9701 Temp Cycle Req

Table 1 Temperature cycling requirements specified in Table 4.1 of IPC 9701

Test Condition	Mandated Condition
Temperature Cycle (TC) Condition: ***TC1***	***0℃ ↔ +100℃ (Preferred Reference)***
TC2	−25℃ ↔ +100℃
TC3	−40℃ ↔ +125℃
TC4	−55℃ ↔ +125℃
TC 5	-55 ℃<-> 100℃
Test Duration	Whichever condition occurs FIRST: 50% ***(preferred 63.2%)*** cumulative failure (Preferred Reference Test Duration) or
Number of Thermal Cycle (NTC) Requirement: NTC-A	200 cycles
NTC-B	500 cycles
NTC-C	1,000 cycles (Preferred for TC2, TC3,and TC4)
NTC-D	3,000 cycles
NTC-E	***6,000 cycles (Preferred Reference TC1***)
Low Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+0/−10℃ (+0/ −5℃) [+0 /−18℉ (+0/ −9℉)]
High Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+10/−0°C (+5/−0°C) [+18/−0℉(+9/ −0℉)]

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Pb-free Guideline- IPC 9701A-Appendix B

- IPC 9701A, Pb-free guideline- Released 2006
- Appendix B, “Guideline for Thermal Cycle Requirements for Lead-free Solder Joints”
  - Moisture sensitivity, use J-STD-020
  - Reference to several models
    - Details to be covered in IPC 9706
- Release delayed due to lack of data on dwell- 2 dwells
  - D10 (10 minute dwell)

    - Most efficient

    - Use as “stand-alone”, only when modeling understood could be theoretically compared to tin-lead
  - D30+ (30 minutes or higher)- To experimentally induce damage somewhat comparable to tin-lead
- Surface finish
  - Only OSP, IAg
- Requalification is required when
  - Solder paste change
  - Lead terminal change

Pb-free Guideline- IPC 9701A-Appendix B

Effect of Area Array Package Types on Assembly Reliability and Comments on IPC-9701A

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Back-up information for IPC-9701A
Discussion on Key Thermal Cycle Parameters and Projection for Lead-Free Vs Lead-Based Solder Joints

The appendix B of IPC-9701A establishes guidelines for modifications required to IPC-9701 for lead-free solder joints. Currently, there are only limited data and insight to determine acceleration factors and acceleration models for lead-free solders [1-13]. Data on the impact of various thermal cycle profiles on the results of accelerated testing in comparison to eutectic tin-lead solder are still being gathered by industry.

Acceleration thermal cycle test results especially when are compared to lead-free solder alloys are sometimes inaccurately assumed to be the same as product reliability. Correlations between acceleration test and product reliability for tin-lead are somewhat have been established during many years of investigation and product use whereas that is not true for less understood lead-free solder attachment. Reliability is the ability of a product, here surface mount solder attachments, to function under given conditions and for a specified period of time without exceeding acceptable failure levels. Therefore, comments such as a lead-free solder joint is more or less reliable than standard tin-lead solder joint based on only laboratory test results are unsubstantiated. Such general statements are incomplete when the lead-free alloy composition or/and when product information and use conditions are not specified. Product reliability needs to be estimated for solder joint under relevant use conditions.

Ref: APEX 2006

Examples of Ref to IPC 9701- SMTA 2007

QUALIFICATION OF A LEAD-FREE CARD ASSEMBLY AND TEST PROCESS FOR A SERVER COMPLEXITY PCBA

Matthew Kelly[1], Marie Cole[2], Jim Wilcox[3], Jim Bielick[4], Timothy Younger[4], David Braun[4]
IBM Corporation
[1]Toronto, Canada; [2]Hopewell Junction, NY, USA; [3] Endicott, NY, USA; [4]Rochester, MN, USA

ATC: Accelerated Thermal Cycling. 0-100C. Visual inspection and functional test conducted every 250 cycles. Following IPC 9701 thermal profile protocol.

IMPACT OF AGING AND STORAGE CONDITIONS OF OSP PCBs ON BGA SOLDER JOINT RELIABILITY

Bala Nandagopal, Sue Teng and Mason Hu
Manufacturing Technology Group
Cisco Systems, Inc.
San Jose, CA, USA

The boards were subjected to Accelerated Thermal Cycling (ATC) of -40/125°C with 20 minute ramps and 10 minute dwells per IPC9701. The characteristic life (η) results

EFFECT OF TEMPERATURE CYCLING PARAMETERS ON THE SOLDER JOINT RELIABILITY OF A Pb-FREE PBGA PACKAGE

John Manock[1], Richard Coyle[1], Brian Vaccaro[2], Heather McCormick[3], Richard Popowich[1], Debra Fleming[1], Peter Read[1], John Osenbach[2], and Dan Gerlach[2]
[1]Alcatel-Lucent, Murray Hill, NJ, USA; [2]LSI Corp., Allentown, PA, USA;
[3]Celestica Inc., Toronto, ON, Canada
jmanock@alcatel-lucent.com and rcoyle1@alcatel-lucent.com

of SnAgCu (SAC) and SnPb solder assemblies using typical IPC-9701 test conditions for accelerated temperature cycling (ATC) [1]. In the previous study, a temperature range of 0°C to 100°C with 10 minute dwell times was used.

MAFA 2007

COMPARISON OF THE LEVEL 2 CHARACTERISTICS OF HITCE™ SUBSTRATE ASSEMBLED WITH SAC AND HIGH LEAD BALLS

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For IPC9701, forty two assemblies for each leg were thermally cycled between 0°C and 100°C per IPC 9701.

SECOND LEVEL SOLDER JOINT RELIABILITY OF QUAD FLAT NO-LEAD (QFN) PACKAGES FOR USE IN IPC CLASS-2 ASSEMBLIES

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Robert Kinyanjui, Ph.D.
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Sanmina-SCI Corporation
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robert.kinyanjui@sanmina-sci.com

limited data is available that addresses the telecommunication application requirements per the IPC9701 specification under the TC1 test condition.

BOARD LEVEL RELIABILITY OF LEAD-FREE SOLDERED INTERCONNECTS - TEST METHODS

H.-J. Albrecht, M. Heimann, Ch. Götze, and M. Löffler
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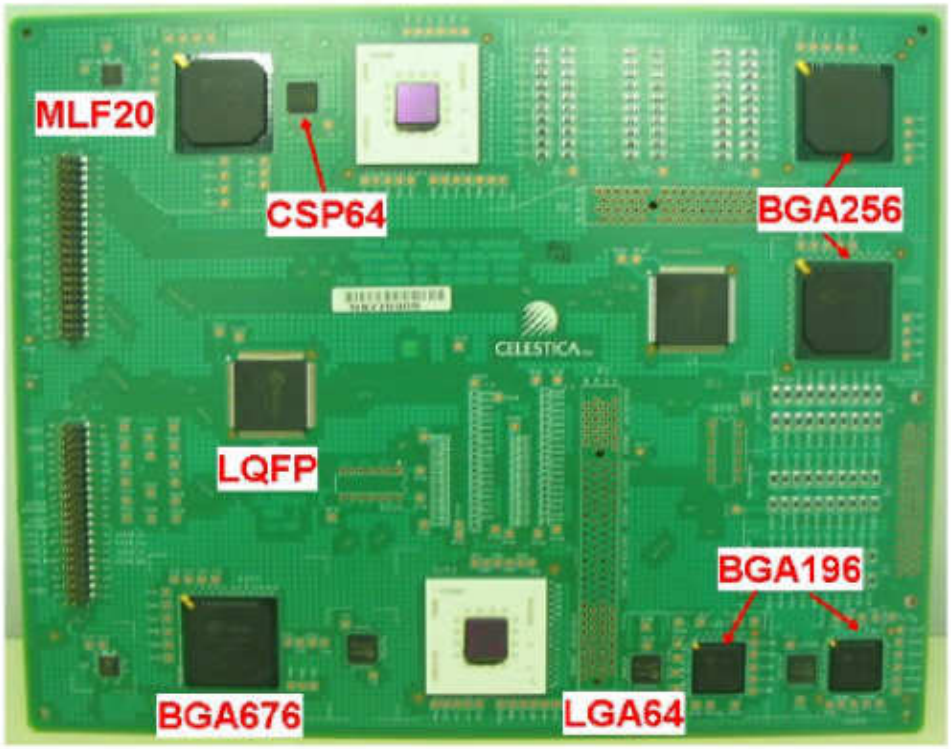
Berlin, Germany
hans-juergen.albrecht@siemens.com

Temperature cycling test conditions should be consistent with the IPC 9701 specification. Here are different test conditions applied to study the performance of lead-free

Comparison of TC Data per IPC 9701 for PBGA 676

- Celestica International Inc, Toronto, Canada
- Solectron/Sun Microsystems
- Xilinx, Inc
- NASA-JPL

Thermal Cycle Test- Celestica RIA3



- 12 layer boards
- 203 mm x 253 mm x 2.36 mm
- Lead-free compatible laminate material
- Board finish – ENIG (Electroless Ni / Immersion Au)

305 & 405 SAC Composition

Table 3. Solder composition

SAC 305 paste			SAC 405 paste		
	Requirements	Composition, %		Requirements	Composition, %
Ag	3.0±0.2%	3.0	Ag	3.9±0.2%	4.0
Cu	0.5±0.1%	0.5	Cu	0.6 ± 0.2	0.6
Zn	<0.002%	0.001	Zn	<0.002%	0.001
Al	<0.002%	0.000	Al	<0.002%	0.000
Sb	<0.12%	0.00	Sb	<0.12%	0.00
Fe	<0.02%	0.00	Fe	<0.02%	0.00
As	<0.03%	0.00	As	<0.03%	0.00
Cd	0.002%	0.000	Cd	0.002%	0.000
Pb	<0.050%	0.006	Pb	<0.050%	0.004
Bi	<0.10%	0.01	Bi	<0.10%	0.01
Sn	Remainder	Remain	Sn	Remainder	Remain

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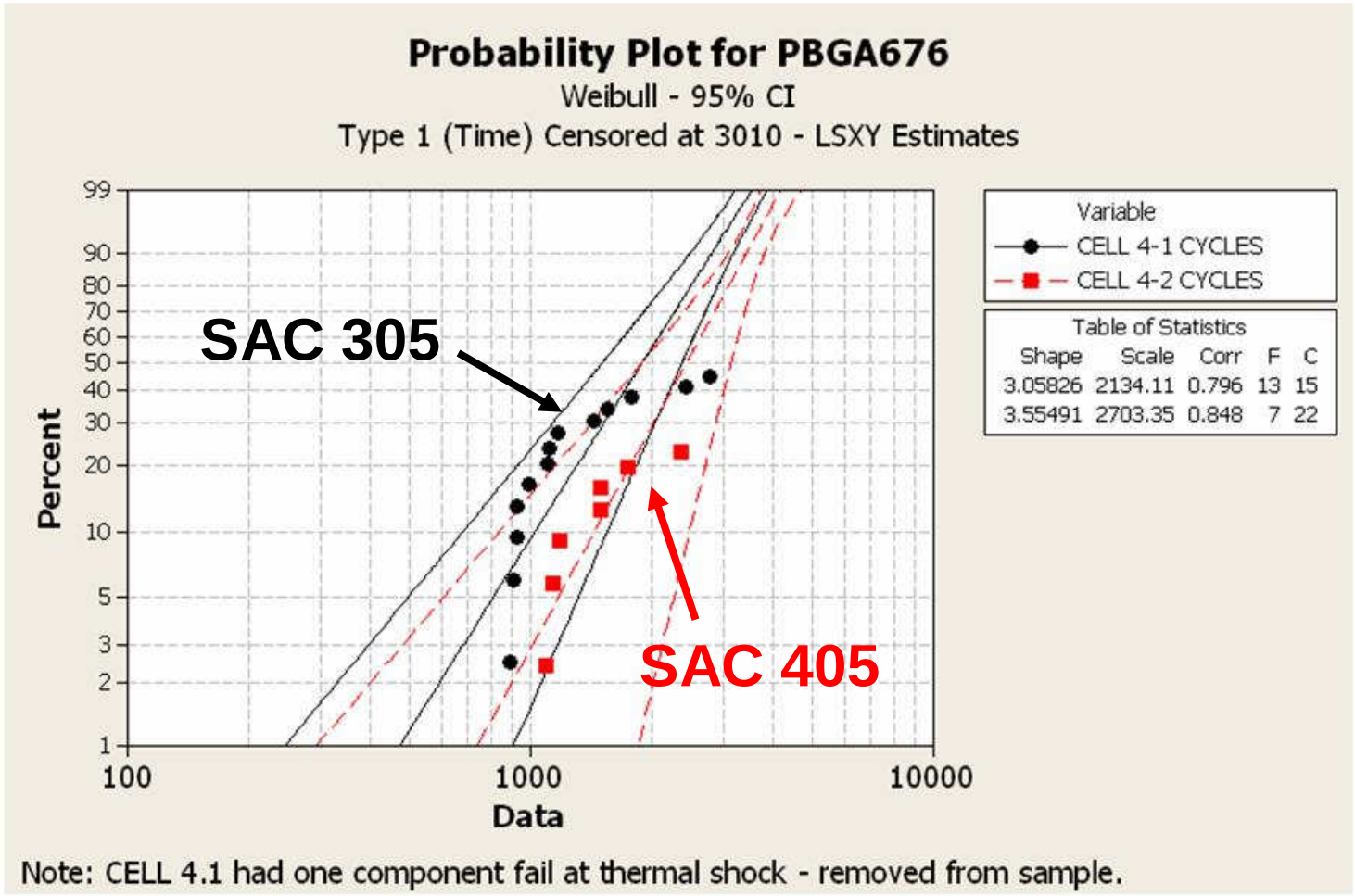
TC for PBGA 676- Celestica RIA3

- 405 balls/405 Paste, 305 balls/305 Paste
- Two thermal cycles
  - 0-100C 60 min, 15 min dwells, 15 min ramp/cool
  - -55 -100C, 60 min, 15 min dwells, 15 min ramp/cool
- Failure- 5 consecutive with $\geq$ 20% relative to its hot as-built resistance

Thermal Cycle Data for PBGA676 (-55/125C)



0-100C, SAC 305, 7 failures <2,500, 5400, 5800 cycles

0-100C, SAC 405, 7 failures <1,500, No failures to 6,000

Ref: Celestica SMTA 2006

Check @ 3010 - Electrical Failure @1778 (-55/125C)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A			6	5		4		4			4	5	4	4	5	4	5		6	5	6	5	5	3	6	4	A
B			5	5	5	4	5					4		5	5	4		5	6	4	4	5	5	4	5	5	B
C			5	5	6	3	5	4		4	5	5	5	5	6	5		6			6	6	6	6	6	3	C
D	6	5				4	5			5	5	4	4	5		5	5						6	6	6	4	D
E	6	6		4	6		5	5		5					4		4	3		5	4			6	6	4	E
F	6		6	4	4			4			5	5	5		5	4	5						5			5	F
G			4	5								3	5	4	5			4			5	4	5	6	4		G
H									3		4	5		4				6							6	4	H
J											4			4													J
K												5			4										6		K
L	6										3	4	4	4		3	4	3									L
M	4	5	6								5	3	3			3				5				4	4		M
N	4		4	3	5		6			4	4													3			N
P	4		5	4				6	4		5	5	5	6	5	5		4		4	6	3	5	5	6		P
R	5	6	5	6	6		4				2	4		5	6	5	4	5	5	5		5				4	R
T	6	5	4	5		6	6			5	3	4		5	3	4		4		6	4				5	4	T
U	5	6	5	5	5	5		4	4	4	4			4	4	4		4	5	6							U
V	5		5	6		5	4			4	5	4		5			4	4		3	4	4	6	5		4	V
W					5	3		5	4	6	6		5	6	5	5	5	5	5		5			4			W
Y	5	6			4	4	6		5	5	5	4	4		5		5	5	5	5	4		6	5	5	3	Y
AA	4	6	5	5	3			5									5	5		5		4		4	4	3	AA
AB	5	6			4	4	6	5	5	5	5	4	5	3	5				5			5	5	4	5	5	AB
AC		6		5	4		6		5			5	5	5	5			6		4		6	4	4	5	3	AC
AD		6		5		6		6		5	6	4							6			5			5	4	AD
AE	4	6	6	5	6	4				5	4	6	5	6			6	4								5	AE
AF	5	6	6	6		6		5																	3	4	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

EGA I/O = 196

Failure Mode	# of Sites	% of Sites	% Fractured - Eye Present
1	0	0%	1 = Open
2	2	1%	2 = 71-90%
3	0	0%	3 = 51-70%
4	0	0%	4 = 31-50%
5	0	0%	5 = 11-30%
6	2	1%	6 = 1-10%

No Mechanical Failures @ 3010?

Ref: Celestica SMTAI 2006

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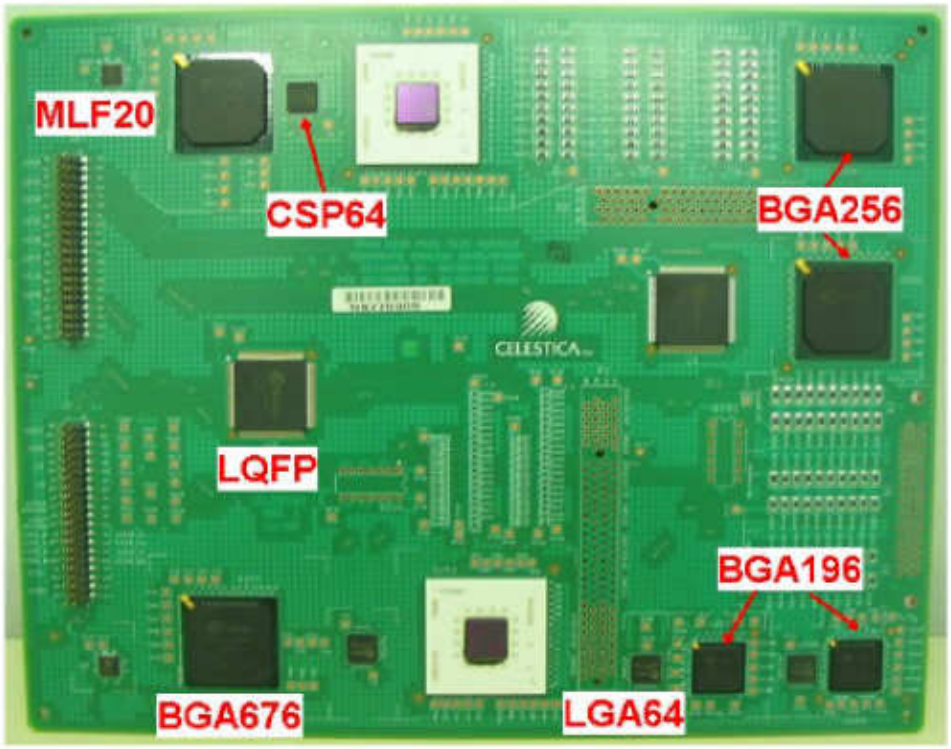
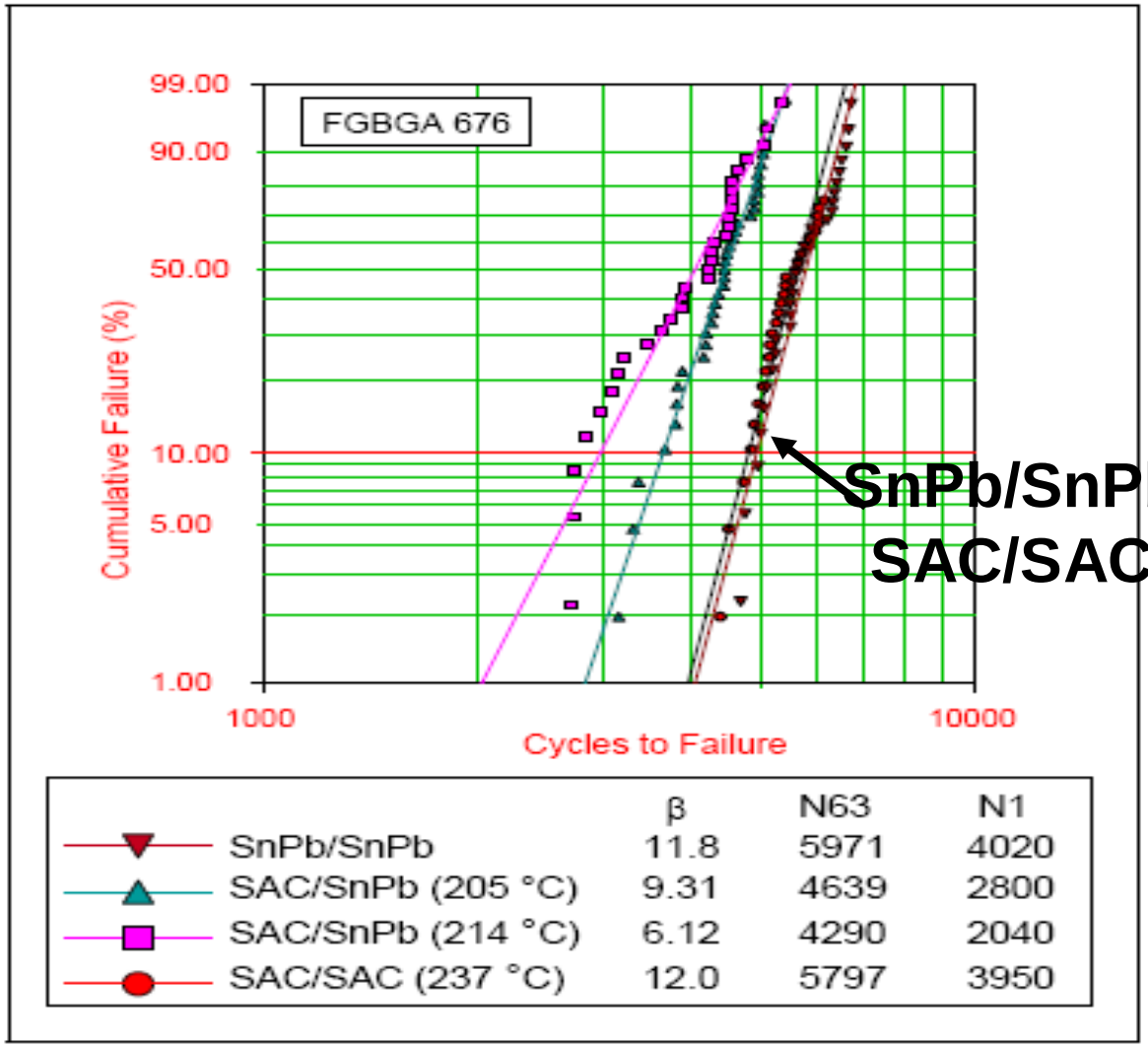
Thermal Cycle Test- Celestica RIA3



- 12 layer boards
- 203 mm x 253 mm x 2.36 mm
- Lead-free compatible laminate material
- Board finish – ENIG (Electroless Ni / Immersion Au)

Thermal Cycle Results (0-100C)- Solectron/Sun Microsystems

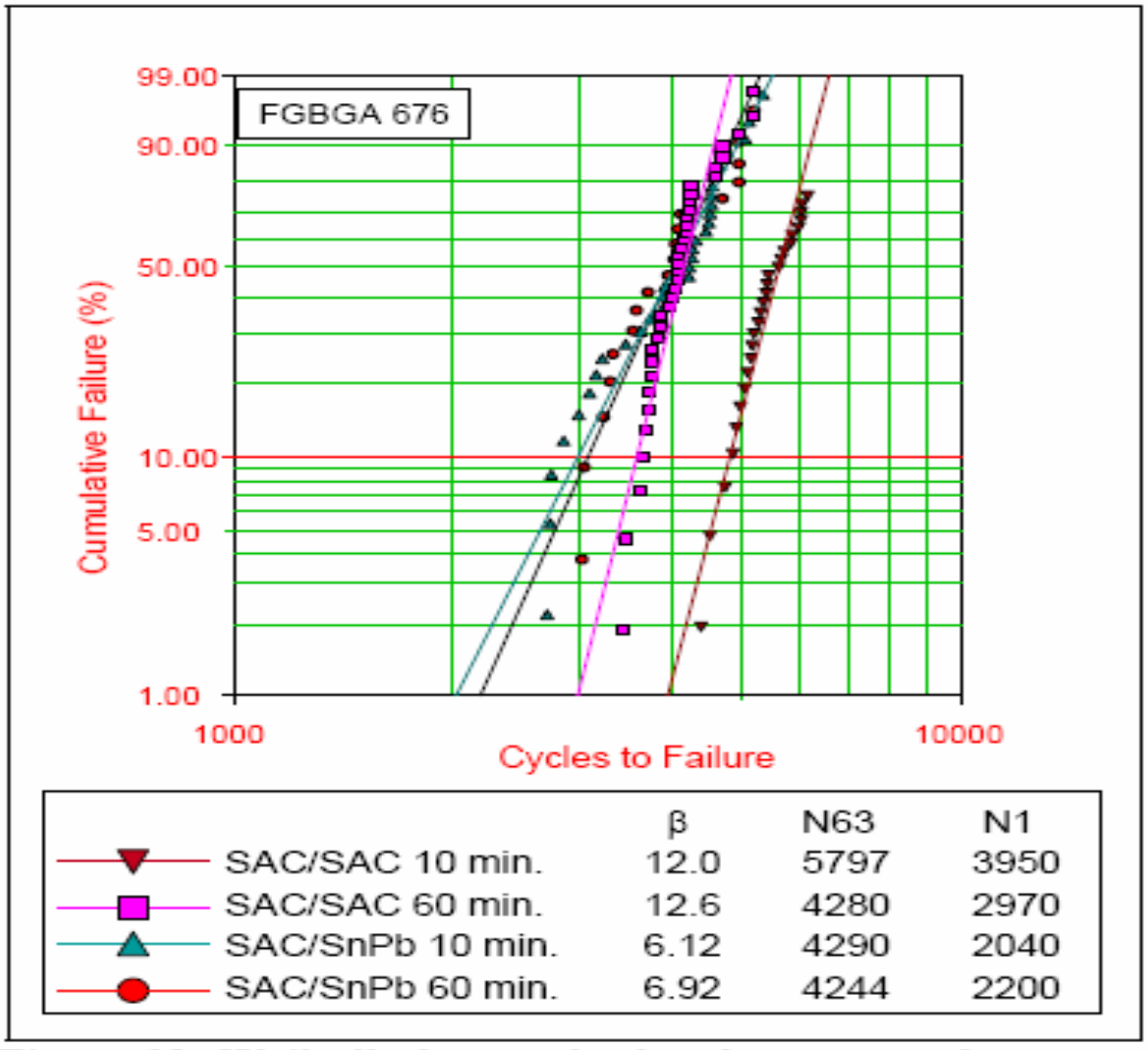


	β	N63	N1
SnPb/SnPb	11.8	5971	4020
SAC/SnPb (205 °C)	9.31	4639	2800
SAC/SnPb (214 °C)	6.12	4290	2040
SAC/SAC (237 °C)	12.0	5797	3950

0-100C, 40 min (10 min dwells, 10 min ramp/cool)

Ref: Bath, et al SMTAi 2005

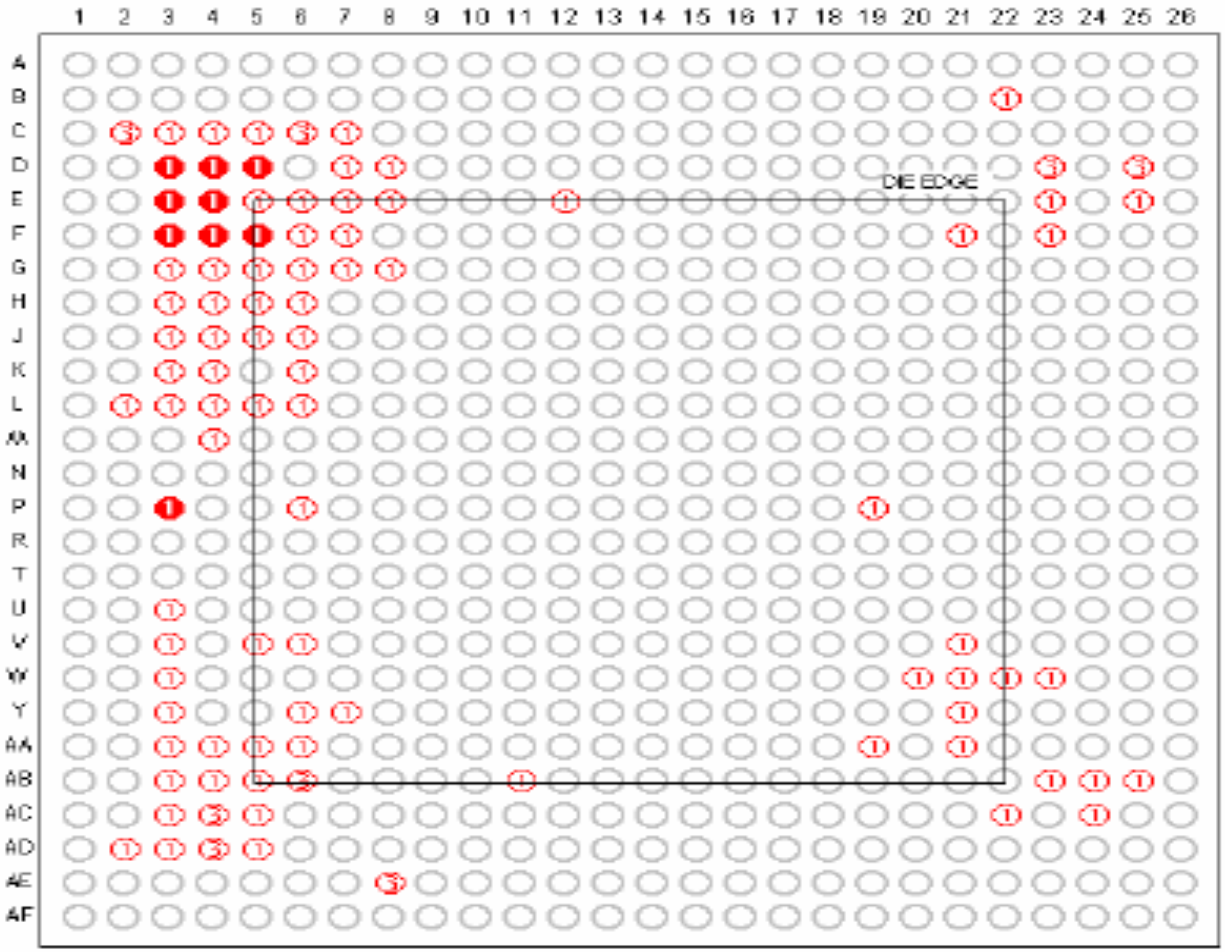
Thermal Cycle Results (0-100C)- 10 & 60 Min Dwells



	β	N63	N1
SAC/SAC 10 min.	12.0	5797	3950
SAC/SAC 60 min.	12.6	4280	2970
SAC/SnPb 10 min.	6.12	4290	2040
SAC/SnPb 60 min.	6.92	4244	2200

Ref: Bath, et al SMTAi 2005

Thermal Cycle Results (0-100C) SAC/SAC- 10 Min Dwells



❶	1.3%	Complete Fracture at Package/Solder Interface
①	11.4%	Partial Fracture at Package/Solder Interface
③	1.2%	Partial Fracture at PCB/Solder Interface
○	86.1%	No Pre-existing Cracks (no red dye)

Ref: Bath, et al SMTAi 2005

IPC 9701A Failure Definition & Actual Test

Electrical (High and Low Temperatures)	Continuous intermittent event monitoring (preferred reference) OR Continuous electrical resistance monitoring (maximum scan interval of all chains = one minute). Manual monitoring is not allowed.
Failure Definition	Event detector: 1000 Ω, 10 events (maximum), 1 micro-second duration (maximum), report first verified as time-to-failure AND/OR Data logger/Voltmeter: 20% nominal resistance increase (maximum), five readings/ scans (maximum)

Failure Definition:

Celestica: 20% increase and event detector

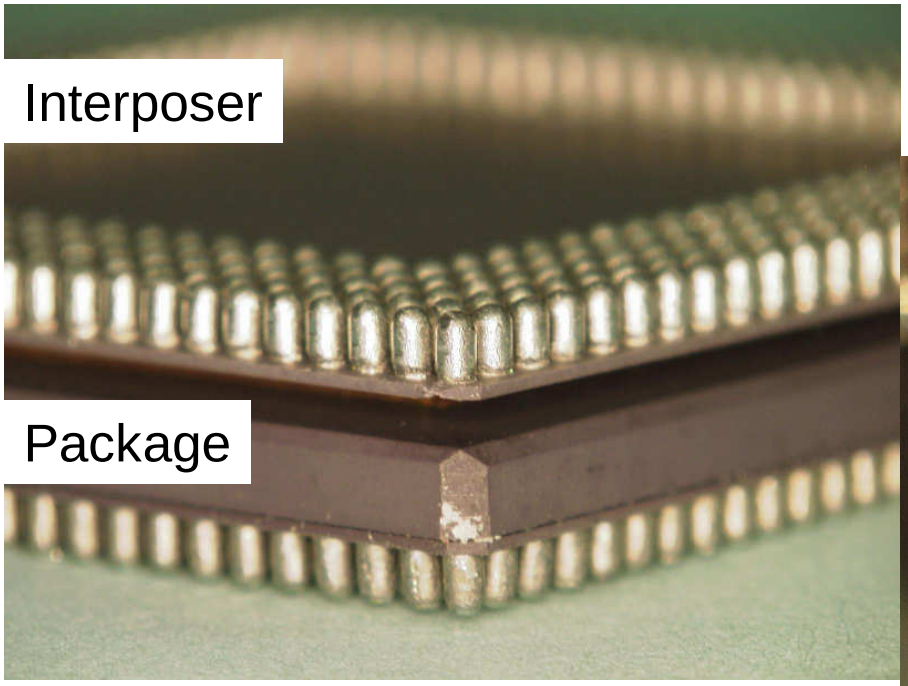
Solectron/Sun: Event detector, not specified failure

Xilinx: Event detector, >500 ohms

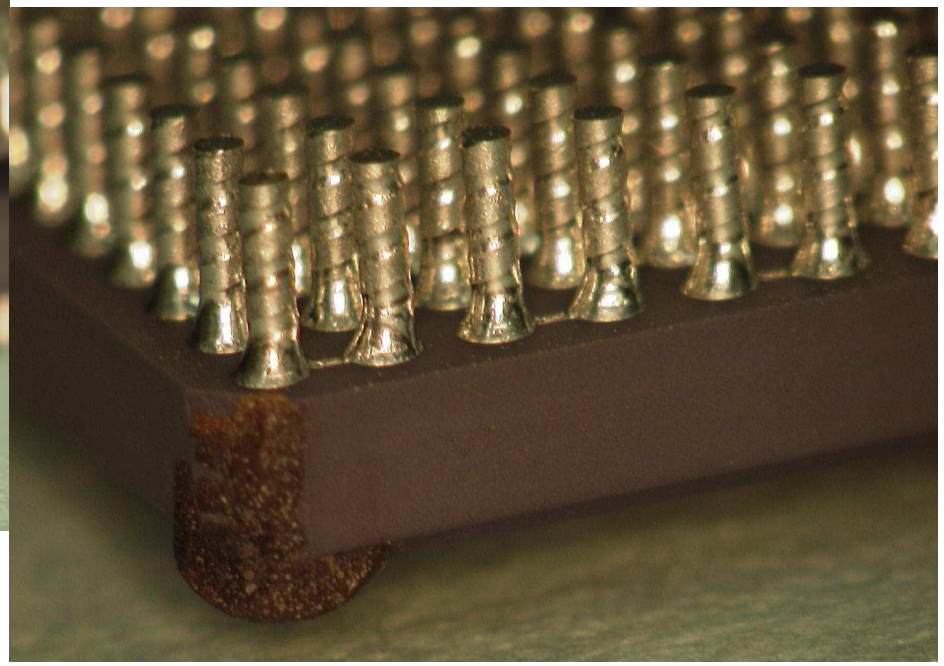
New Data for RIA3 In Harsh Environment

- JPL's Preliminary TC results using Celestica's RIA3 405/405. No failures to:
  - ~ 200 cycle (-130/85°C), 4 parts
  - ~ 200 cycles (-55°/125°C), 6 parts
  - ~ 200 cycles (-55°/100°C), 8 parts
- Pb-free vs SnPb
  - Mild (0°/100°C) – probably the same Solectron, Xilinx/Celestica?
  - Harsh (-55°/125°C) – SnPb>Pb-free? Xilinx & Celestica?
    - Remember- Electrical failure earlier than Dye & pry failure
- Future Activities
  - Rework PBGA 676 I/Os in 305/305
  - Include 305/305 assemblies into test matrix
  - Test more RIA3 in harsh environment

Current Activies: TC of Recolum CCGA 560 I/O



CCGA- Package-Interposer

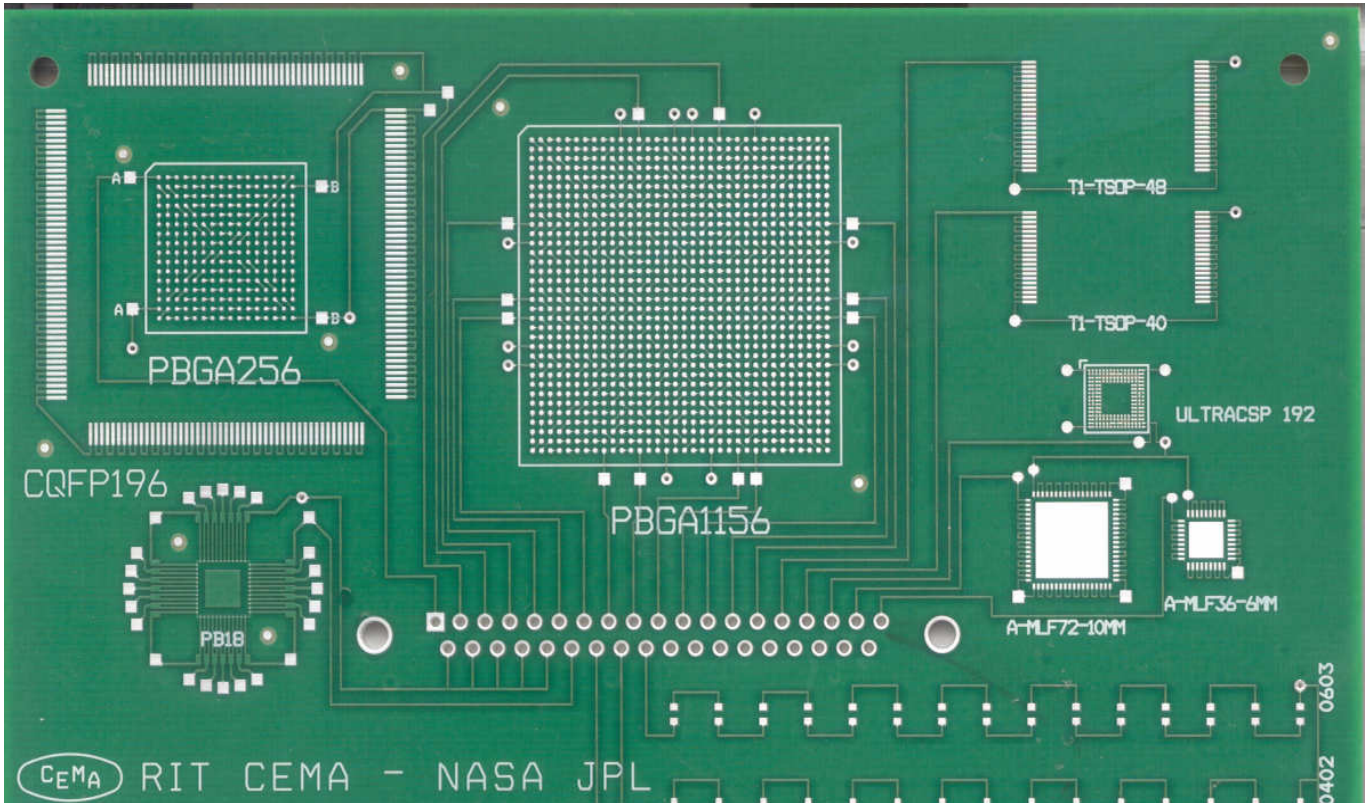


Recolumn Six Sigma Column

SEE: Microelectronics Quality and Reliability Workshop

MRQW – Dec 4-5, 2007

Current Activitie: Rel of High I/O & Low Pitch



EFFECT OF FORWARD & BACKWARD COMPATIBILITY OF SOLDER PASTE & COMPONENT FINISH ON FINE-PITCH COMPONENT ASSEMBLIES USING ENIG AND IMAG PWB FINISHES

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Center for Electronics Manufacturing and Assembly

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California Institute of Technology

ASME-InterPACK 2007

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