RTAX4000S Generic Burn-in For Programmed Devices

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Introduction

- **A "Generic Burn-in" method for a programmed Actel RTAX4000S product**
  - Implemented on RTAX4000S using UMC 0.15 µm process technology
  - RTAX4000S is Actel's most recent and largest antifuse FPGA
    - 4 million user gates
    - System Solution - 30 times the size of an RTSX32SU
  - Generic burn-in is not supported on RTAX2000S, RTAX1000S or RTAX250S
- **TOPICS**
  - Features of generic burn-in
  - RTAX4000S tile architecture
  - Super Cluster building blocks and terminology
  - Test implementation schematics and logic table
  - Initial results
  - Conclusion

Why Generic Burn-in?

- Actel customers will never need to generate specific test patterns for their programmed RTAX4000S design, saving both time and costs.
- ASIC burn-in test vectors often achieve less than 70% AC toggle coverage of the design whereas an Actel Generic Burn-in provides complete network exercise.
- Specific Burn-in boards are not required to accommodate custom user designs.
- RTAX4000S Programmed parts with multiple designs can be burned-in simultaneously using "Actel Generic Burn-In" boards.

RTAX4000S Device Architecture

- **RTAX4000S is structured in a 6x5 array of 30 core tiles.**
  - **Each core tile is composed of arrays of 336 super clusters and four SRAM blocks.**

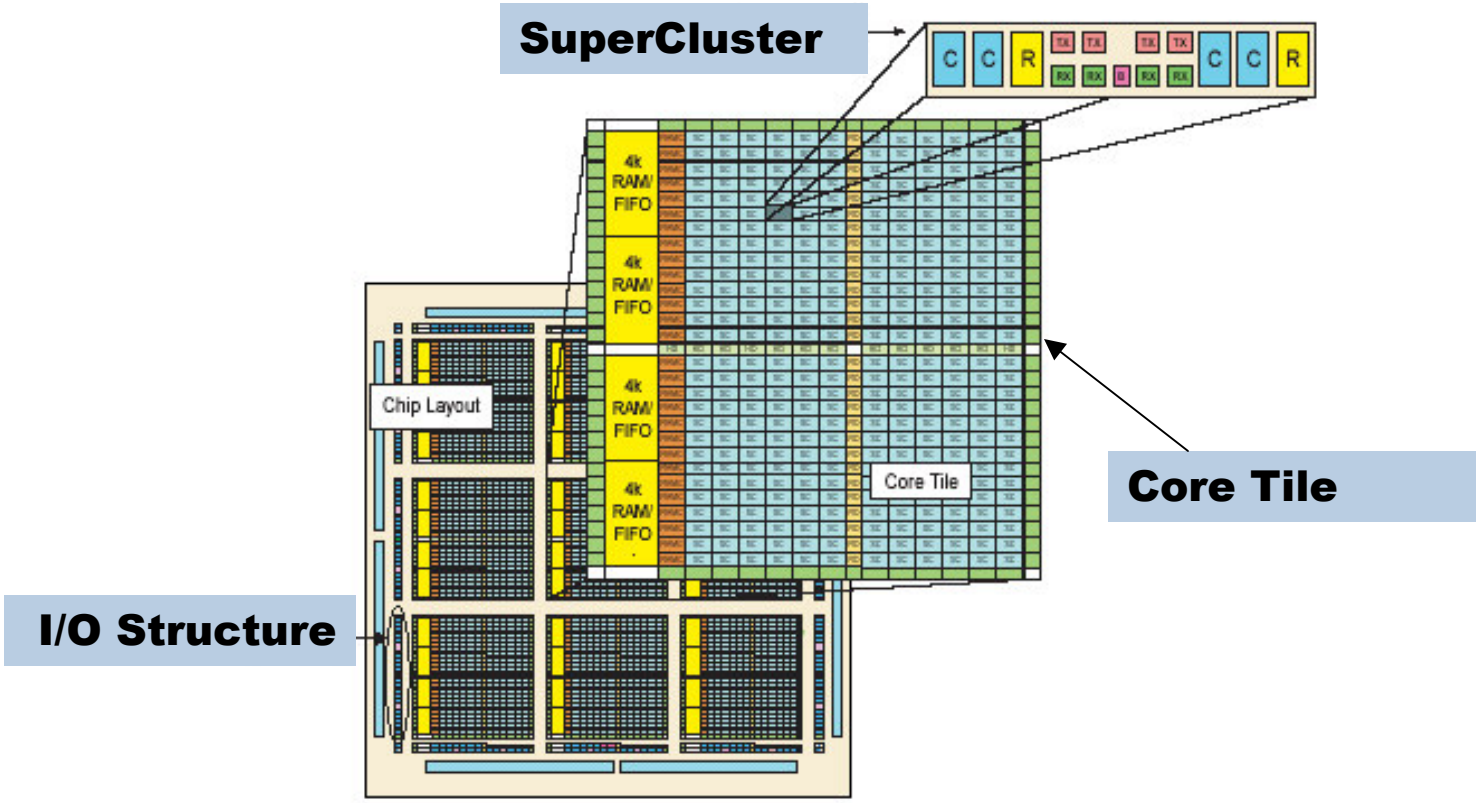


Figure 1: RTAX-S Device Architecture (RTAX1000S shown)

RTAX4000S SuperCluster

- **The RTAX4000S SuperCluster architecture integrates several logic cells consisting of Primary and Secondary logic cells.**

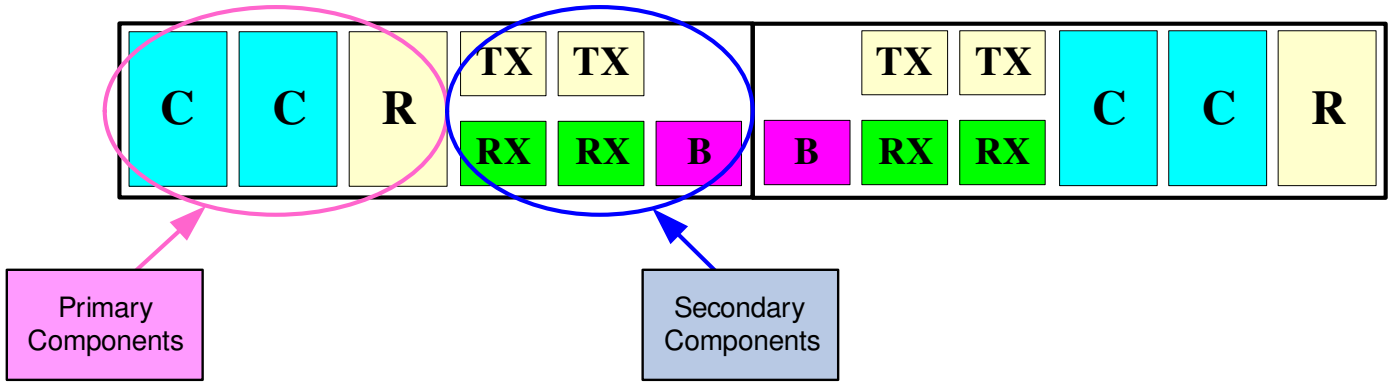


Figure 2: RTAX-S SuperCluster Block Diagram

- **Primary logic building components available to construct a design are:**
  - **C-Cell: A Combinatorial logic cell**
  - **R-Cell: A Register (or flip flop) cell**
  - **IO-DFF: (Registers used in the I/O clusters – not shown above)**

Secondary SuperCluster Components

- **Secondary building components shown in Figure 2 are:**
  - TX-Cell: Transmitter
  - RX-Cell: Receivers
  - B-Cell: Dedicated Buffers
  - Input and Output modules in the RAM cluster
- **Secondary components are either unused or are always driven by primary components.**
  - These are used for purposes such as non-inverting buffering functions, expanded fanouts, lengthy routing distances, and driving RAM block inputs.
  - No circuit additions or changes are required for secondary components as the primary modules will toggle these.

Generic Burn-in Circuit Implementation

- **Minor modifications were made in only two circuits.**
  - These changes were made in the combinatorial logic and the output portion of the RAM module.
- **The modifications do not have any significant timing delay in the two circuits affected.**

Logic Modules and Routing

- The level 1 routing structures (In and between SuperClusters)
  - FastConnect
    - *FastConnects with a single antifuse to make a connection and provides high-performance horizontal routing inside the SuperCluster and vertical routing to the SuperCluster immediately below it.*

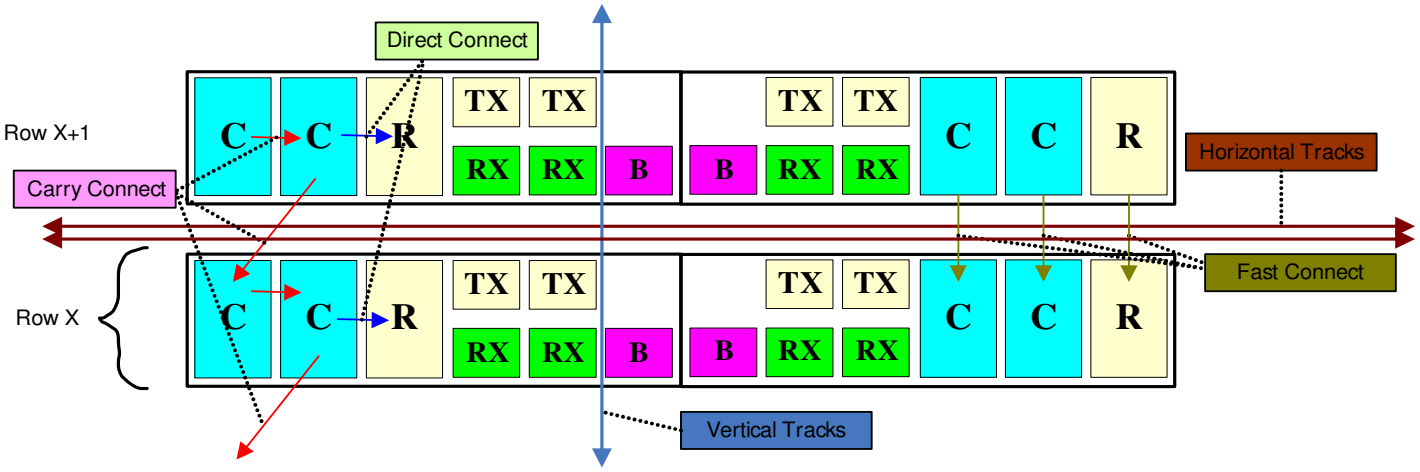


Figure 3: RTAX-S SuperCluster Routing Structure

  - CarryConnect routing
    - *CarryConnects which do not require an antifuse to make a connection are used for routing carry logic between adjacent SuperClusters*
  - DirectConnect
    - *DirectConnects which also do not require the use of antifuses provide the highest performance routing inside the SuperClusters connecting the C-cell to the adjacent R-cell*

RTAX4000S I/O Clusters

- Array Logic is surrounded by I/O clusters.

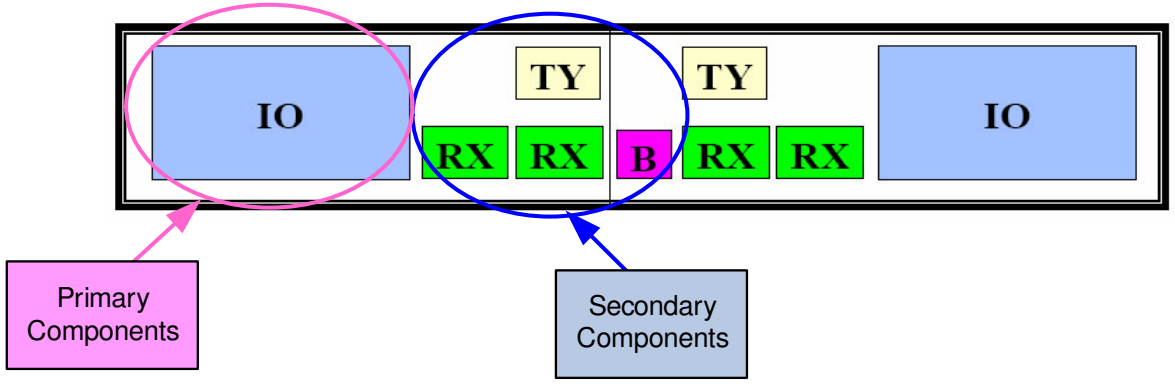


Figure 4: RTAX-S I/O Cluster Block Diagram

- An I/O Cluster includes two I/O modules, four RX modules, two TY modules, and a Buffer (B) module.
- Each I/O module has an input register (InReg), output register (OutReg) and enable register (EnReg).

Generic Burn-in Circuit Implementation

- The generic burn-in test is implemented using existing global test circuit commands.
- The control signals for the combinatorial module are shown below
  - ISOIN: Control signal to isolate low voltage transistors during programming.
  - TEST_SEU: Control signal to test the Triple Modular Redundancy (TMR) circuitry.
  - X3: Control Signal used in association with row selection using Silicon Explorer.
- The generic burn-in test control signals for the sequential module are shown in the following slide

Complete Truth Table For Primary Cells

- **The below figures show the truth table of how the outputs of the primary modules are toggled.**
  - Control inputs are toggled to switch the primary components between "Normal operation" and "Test mode."

C-Mod Truth Table				
ISOIN	TEST_SEU	X3	C-mod OUT	Mode
0	0	0	0	Test Mode
	0	1	0	
	1	0	0	
	1	1	1	
1	0	0	out	Normal operation
	0	1	out	Test Mode
	1	0	out	
	1	1	1	

Table 1: Combinatorial Module Truth Table

DFF Truth Table				
ISOIN	GBSET	GBRST	DFF OUT	Mode
0	0	0	0	Test Mode
	0	1	1	
	1	0	0	
	1	1	0	
1	0	0	0	Normal operation
	0	1	1	
	1	0	0	
	1	1	out	

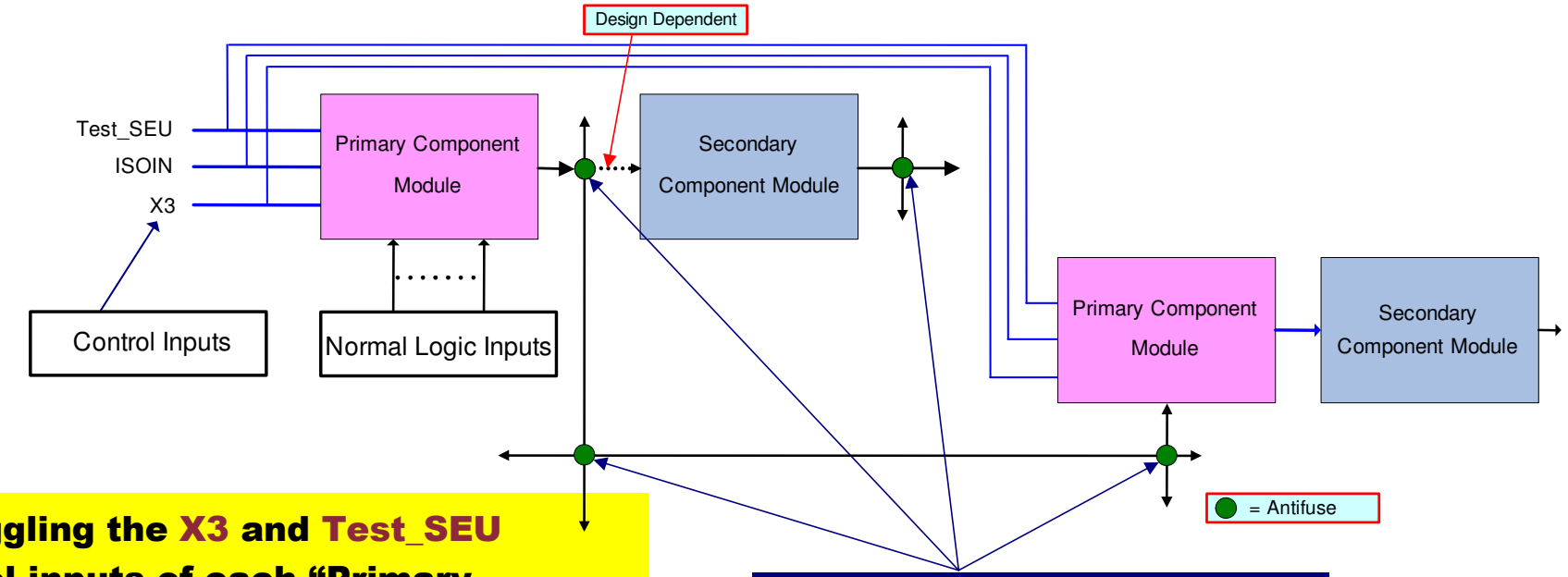
Table 2: Sequential Module Truth Table

Primary Module Output Toggles

  - Outputs of the primary components then drive inputs of the secondary components mentioned in Figure 2.

Simplified Signal Path Schematic

Schematic of the combinatorial module path

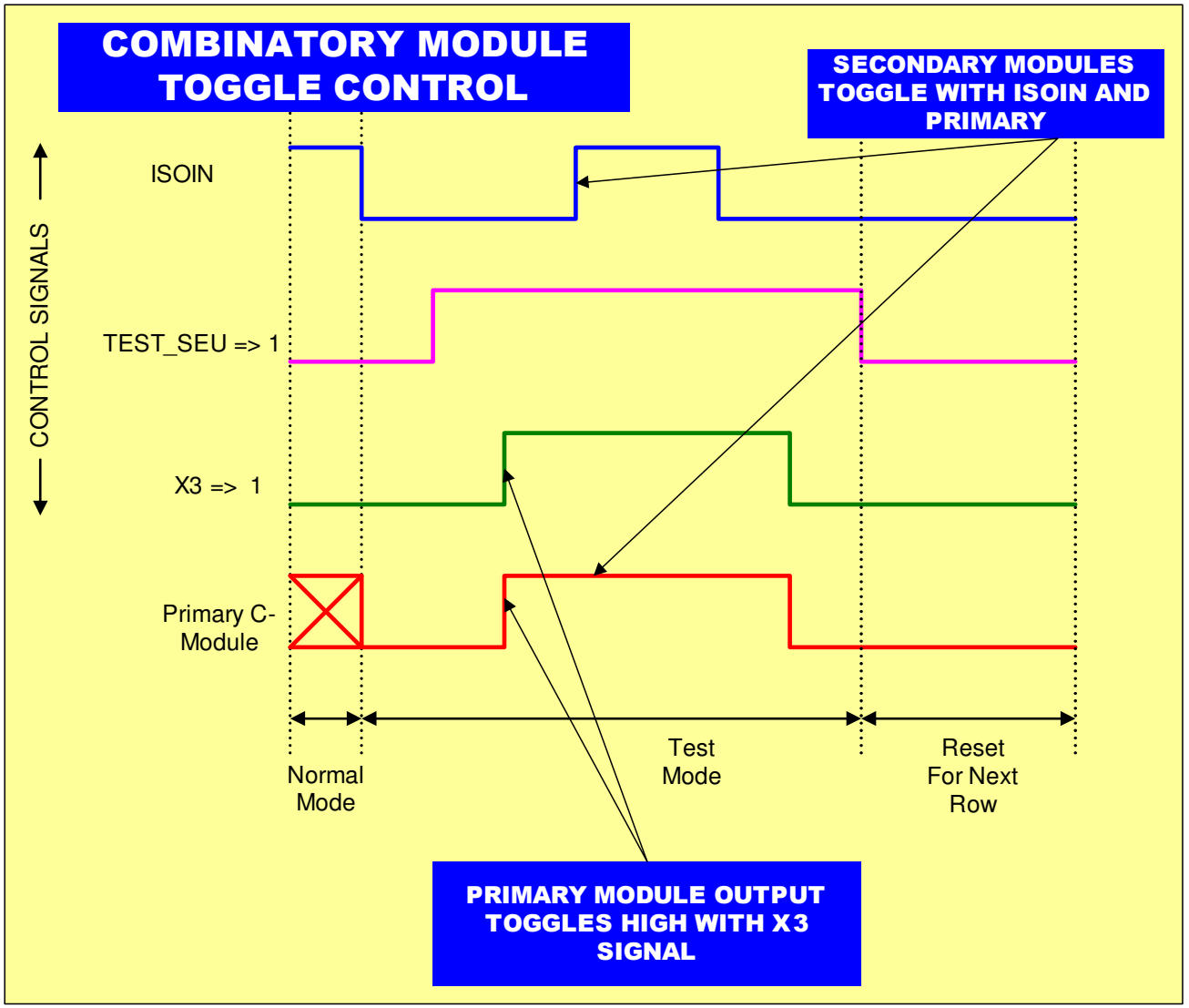


By toggling the X3 and Test_SEU control inputs of each "Primary Component" module, the outputs of the secondary modules will toggle. As a result, the network routing driven by that module will be exercised.

All antifuses associated with the normal user circuit path will be exercised.

Figure 5: Primary to Secondary Signal Path

Generic Burn-in – Combinatorial Module Waveforms



ISOIN: Control signal to isolate low voltage transistors during programming.

TEST_SEU: Control signal to test the Triple Modular Redundancy (TMR) circuitry.

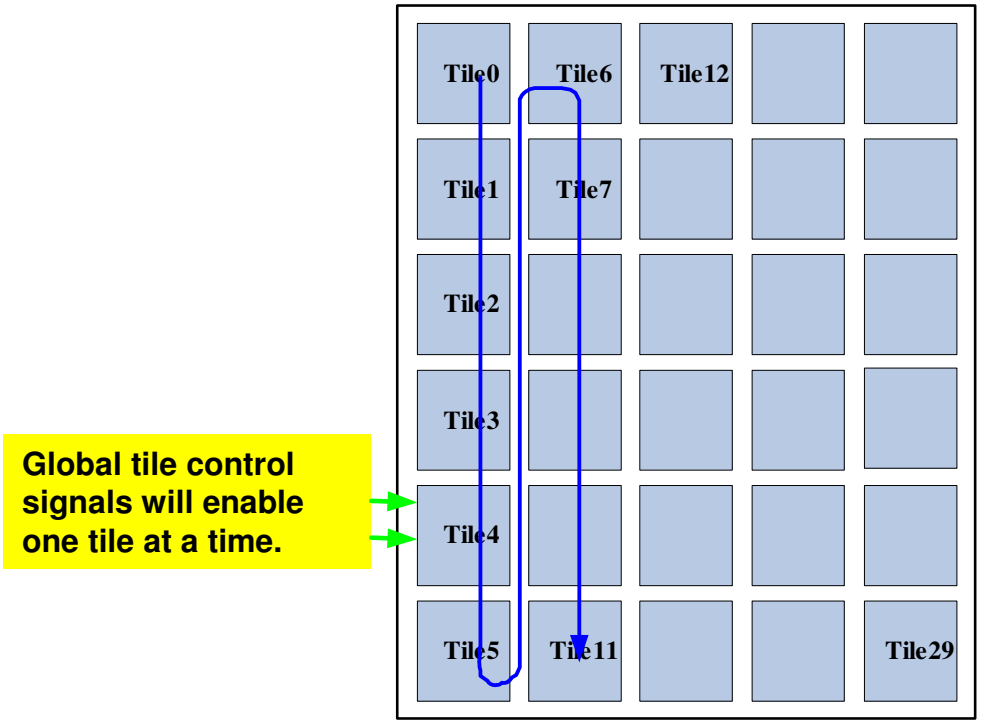
X3: Control Signal used in association with Silicon Explorer.

Complete RTAX4000S Burn-in Solution

- **Dynamic Blank Burn-in (DBBI), Static Blank Burn-in (SBBI) for E-flow**
  - CMOS logic gates
  - Un-programmed antifuses are voltage stressed
  - RAM blocks are exercised using BIST
  - I/O's are exercised using the BSR circuit
  - Clock networks are toggled
- **GENERIC BURN-IN For Programmed Devices**
  - All CMOS logic is exercised
    - Primary and Secondary modules
  - Programmed antifuses are current stressed
  - Clock Networks are toggled
  - All Programmed Nets are toggled
  - I/O's are exercised

Test Implementation

- **Tests are performed sequentially with one tile at a time activated to limit power consumption and noise.**
  - The test is done by exercising and monitoring modules in one tile at a time.
  - The test is done with the sequence as shown below.



Functionality of modules in a tile is checked before moving onto the next tile. Each logic module output is routed to the TDO pin and status of each device is displayed using software associated with the INCAL burn-in system.

Figure 6: Tile Test Sequence

Verification Results

- **Verification of the Generic Burn-in concept was performed with:**
  - Software simulation tools in the design phase based on a TCL (Test Control Language) script written to place a logic value onto a net via the programming circuitry and then reading the value back using the dedicated probe pins.
  - Bench level testing using dedicated Silicon Explorer probe pin outputs as well as TDO outputs verified cell toggling on the following modules.
    - C-Cells
    - R-Cells
    - IOENFF
    - IOINFF
    - IOOUTFF
    - RAM Module
  - Testing verification in burn-in system with sample of devices was successful.
  - Logging of pre and post burn-in data required.
    - Catching real time functional change in burn-in system is not possible.

Conclusion

- **The "Generic Burn-In" test methodology greatly simplifies performing Burn-In of programmed RTAX4000S parts**
  - Provides customer with 100% toggle coverage of nets in the customer's design including all logic modules, metal interconnects, and antifuses utilized in the customer's design.
  - Saves customer time and costs to create burn-in vectors and custom burn-in boards.
  - Provides customer with additional confidence for reliability.