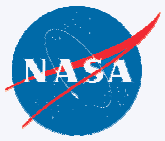

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FPGA Insertion Guidelines

November 27, 2007

Douglas Sheldon
NASA Jet Propulsion Laboratory
California Institute of Technology

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Documents That Already Exist

- MIL-PRF-38535
- JPL-D-20348
- GSFC EEE-INST-002
- Aerospace TORs:
  - MIL-STD-1546 (Parts Management) and MIL-STD-1547 (Technical Requirements) have been updated (2007) and published as Aerospace Technical Operating Reports (TOR)
  - "New PMP Technology Insertion Guidelines" - ATR-2005(9308)-1
  - "Parts, Materials and Processes Control Program for Space and Launch Vehicles" - TOR-2006(8583)-5235
  - "Technical Requirements for Electronic Parts, Materials, and Processes Used in Space and Launch Vehicles" - TOR-2006(8583)-5236
- Various internal design guidelines for each NASA center, government contractor, etc.

Why do we need another FPGA related document?

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Leading Edge VLSI

- **FPGAs represent the leading edge of highly scaled CMOS technology in spacecraft use.**
- **The "bathtub" is shrinking for modern, foundry based devices.**
- **Past approaches to high reliability parts have limitations:**
  - **Conservative design (guardband) to address wear out**
    - ***Too expensive, loss of performance***
  - **Burn-in to address defects.**
    - ***Too expensive***
    - ***Difficult to perform***
    - ***Doesn't address new types of possible failures***

QuickTime™ and a
TIFF (Uncompressed) decompressor
are needed to see this picture.

Mitra/Agarwal ITC 2007

Insertion guidelines needed to comprehend these changes

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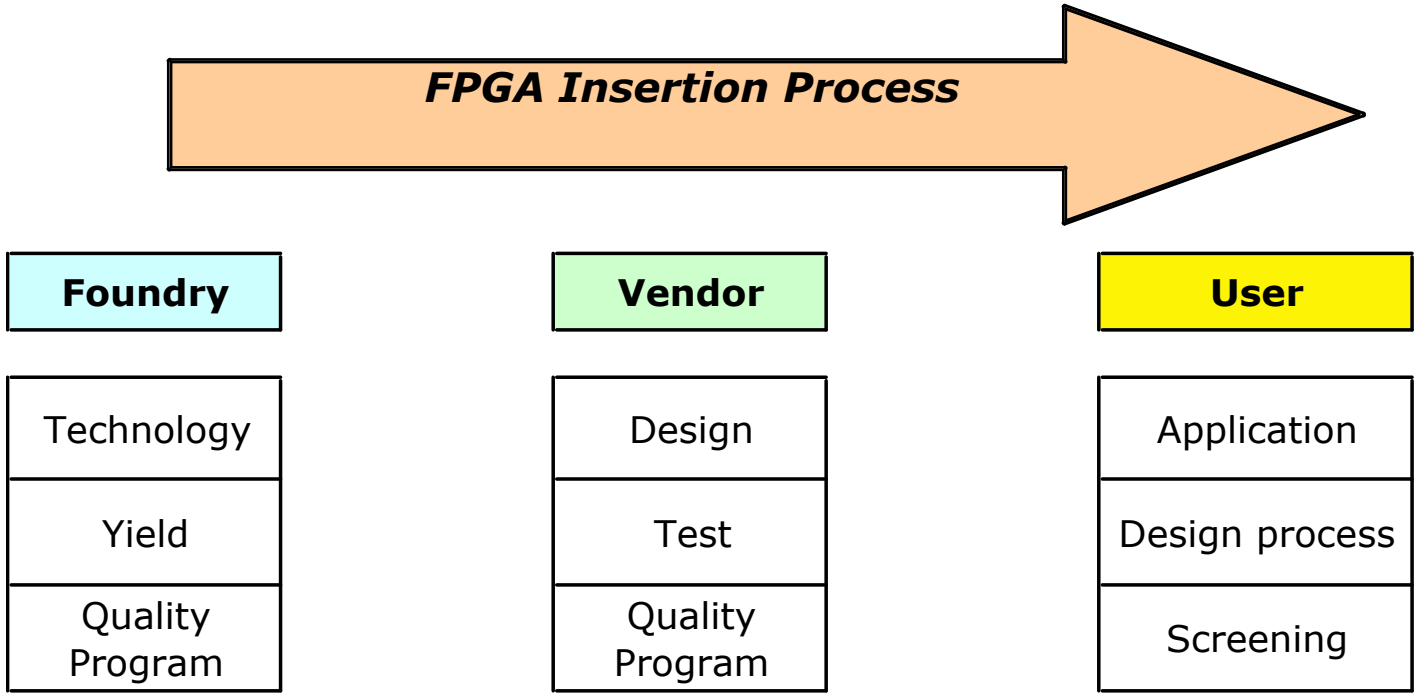
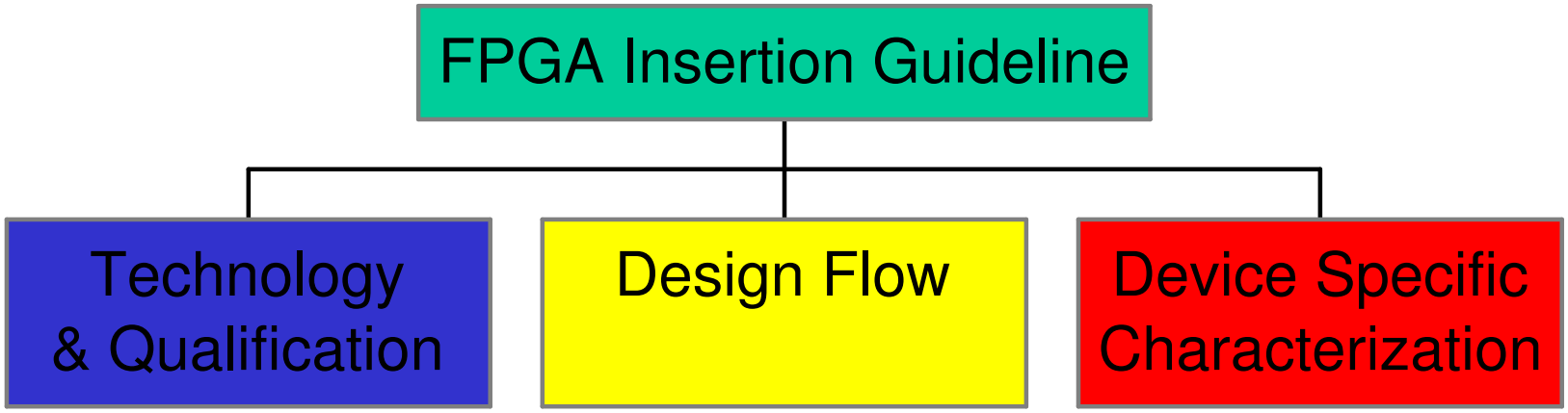
Overall FPGA Insertion Process Flow



Successful insertion requires significant contributions from all three areas.

Insertion Guideline Structure



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FPGA Insertion Guideline Structure

- Technology and Qualification
  - A through understanding of the details of how the FPGA is manufactured and how it might fail.
  - The understanding of these failure mechanisms is then used to develop qualification tests and milestones to ensure the highest quality FPGA is obtained for use.

- The Design Flow
  - –The processes and tools used by the design organization to ensure that the design and implementation of the FPGA are adequate.
  - –The FPGA is a design-centric device and the design process plays a pivotal role in the success of the overall insertion process.

- Device Specific Characterization
  - –New and developing area for FPGAs, additional to vendor testing.
  - –Well-established concepts such as burn-in screening and life prediction have now become *application specific* parameters.
  - –Due to this application specific nature, on-board characterization of each design on each device becomes a requirement for successful risk mitigation and management.

Technology and Qualification

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Technology and Qualification

- **Wafer Level Reliability** (Electromigration, TDDB, Hot Carrier, NBTI, Antifuse, etc)
  - Physics of Failure approach
  - What models are used and why
- **Activation Energy**
  - All failure modes
  - Periodic Monitoring
- **Process variability analysis**
- **Wafer Lot Acceptance**
  - How is it defined
- **Long Term Reliability Testing and Failure Rates**
- **Manufacturing**
  - Process must be documented
  - System must be established to ensure configuration and control
  - Statistical Process Controls must be implemented
  - Evaluation of maturity of manufacturing process
    - Multiple manufacturing lots
    - Process and performance repeatability
    - Yield

Technology and Qualification

- **Device Qualification**
  - MIL-PRF-38535 Group A, B, C and D Testing
    - Group A – electrical
    - Group B – mechanical
    - Group C – die related/life test
    - Group D – package - ***flip chip, CGA, LOTS of new technology***
  - ESD, Latch-up Testing
  - Testing for Other Failure Mechanisms (i.e. low activation energy)
- **Special screens (as required)**
  - **Thermal runaway**
- **Radiation Testing**
  - **TID, SEU, SEE**
  - **Group E for guaranteed performance**

Foundry

- **Technology**
  - **Process qual with simple test structures**
  - **Process qual usually done with SRAM or similar cells**
    - ***Need other structures to address specific FPGA vendor die size, interconnect layers, package issues.***
  - **Die/wafer volume that is significant (>100 wafers)**
  - **Long term testing in package parts (plastic)**
  - **Flip chip packaging**

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Foundry Documentation

- **Foundries should have extensive standards that document their quality and reliability programs and methodologies**
- **Reliability examples:**
  - **JEDEC JEP143, Solid State Reliability Assessment and Qualification Methodologies.**
  - **JEDEC JEP122, Failure Mechanisms and Models for Silicon Semiconductor Devices.**
  - **JEDEC JESD91, Method for Developing Acceleration Models for Electronic Component Failure Mechanisms.**
  - **JEDEC JESD34, Failure-Mechanism-Driven Reliability Qualification of Silicon Devices.**
- **Quality examples:**
  - **EIA-557, Statistical Process Control Systems**
  - **EIA-670, Quality System Assessment**
  - **ISO 9001:2000, Quality Management Systems – Requirements**
  - **JESD671, Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems).**

Audit of Foundry by User

- **An ISO Audit (and related certification) of Foundry is not sufficient.**
- **ISO vs FPGA Space User Audit**
  - **ISO Audit - "Do you have a re-work procedure"**
    - **Yes? - then pass**
  - **FPGA Space User Audit - "Do you have a re-work procedure"**
    - **Yes?**
      - **What are the conditions?**
      - **Number of re-work times?**
      - **How is engineering involved?**
      - **How will this affect *MY PRODUCT*?**
- **Auditing the Foundry by both the User (and Vendor) are important.**

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Qualification Tests Foundry Needs to Perform

- Electromigration
- Stress Migration
- Thermal Cycling (Cu Interconnect)
- Intermetal Dielectric Reliability
- DC Hot Carrier Injection
- Voltage Ramp Dielectric Breakdown
- TDDB
- Plasma Process Induced Damage
- Ion Contamination (BTS and TVS)

- Negative Bias Temperature Instability
- Long term life (HTOL)
- Early Life Test
- Temperature Cycling
- THB/HAST
- Yield & Defect Density Calculation
- ESD and Latchup Characterization
- Process Control Monitor
- DPA/Construction Analysis

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On-line WLR Information Example

Monthly Wafer Level Reliability

FPGA users need access to this level of information

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Vendor vs User = Yield vs Risk

- All FPGA vendor decisions come down to wafer & die yield.
- The high rel FPGA user wants risk mitigation and/or risk retirement.
- How you retire risk may not be the same as how you increase yield.
  - High yield => reduced or eliminated burn-in
  - Low risk => lots of screening/testing
- ***Fatal defects associated with yield loss are related with latent defects that affect device reliability*.**

$$R = Y^k$$

$$where\ k = Area_{reliability}/Area_{yield}$$

- *The more information/understanding about yield, the better the insertion process*

Understand Vendor Test Flow

- Interconnect coverage
  - Is 99.9% enough? Need 99.99%?
- 100% resources testing
- Functional Testing:
  - Memory tests
    - MarchC, MATS, etc
  - Configuration memory
    - Patterns
  - Driven Metal lines
    - Shorts/opens
- AC testing
  - Delays
    - Blocks and interconnects
    - BIST implementations
- Signal Integrity
- Custom designs
  - Resource utilization
  - Methodology
- ***Understanding what the vendor is testing for helps the user understand concerns, risks, etc.***

Design Flow

The Design Flow

- The design flow has two fundamental pieces, **process and documentation.**
- The **process** refers to the intellectual and engineering activities that define the FPGA design from conception to implementation.
  - this process must be rigorous and methodical.
- **Documentation** refers to the accepted and approved standards that define requirements and success criteria at each stage of the process.
- A successful process must include clear and meaningful **documentation** and the documentation must accurately reflect the goals and requirements of the design **process**.

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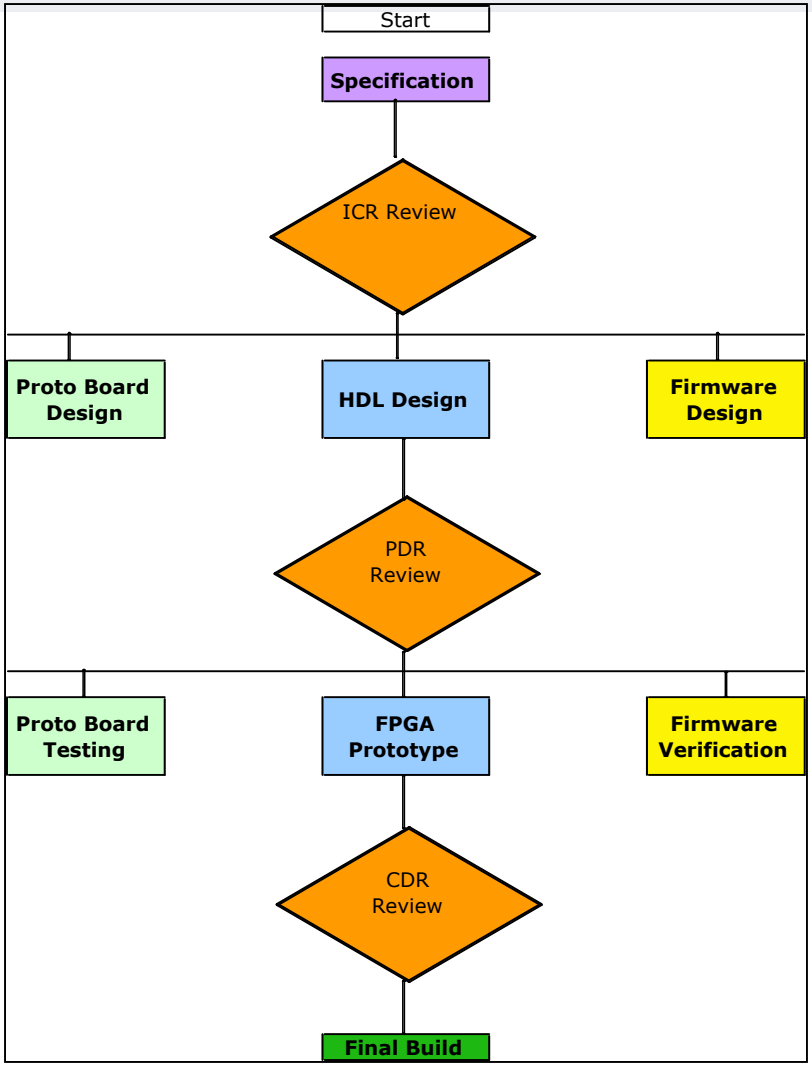
Conceptual and Practical FPGA design flow



- **A well established and documented flow.**
- **Clear progress gates exist to validate moving on to the next level.**
- **The parallel nature of FPGA development is shown.**
  - **Several groups must work (communicate) effectively to ensure successful insertion**

FPGA Specification

- The specification document will describe the implementation and the plan to achieve the given implementation.
- Preliminary implementation technology choice. Describes the choice of FPGA and other components.
- Initial partitioning firmware/hardware/external components.
  - How the design will be partitioned between FPGAs, other components, and firmware.
  - Block diagram showing the partitioning of the design
- Preliminary 'intellectual property' (IP) selection
  - IPs are existing designs that can be incorporated into the FPGA. These may be purchased, licensed, or they may already be exist. This section of the document lists those IPs which will be included, with justification.
- Test approach
  - Much of the FPGA schedule is related to test. Unless a function is tested completely, there is no guarantee that it will work correctly. This section of the specification details the test approach to be used.
- Preliminary FPGA device and package selection

FPGA Specification

- Configuration management approach
  - Even a perfect design can be corrupted if an incorrect version is ultimately implemented. Configuration management and version control are extremely important in maintaining the integrity of the design. A well documented Configuration management approach must exist.
- Review plan
  - This shows the formal reviews and peer reviews and when they will occur.
- Designate a fault-tolerant design approach
  - For flight FPGAs we are very concerned with fault tolerance. Expected reliability under defined radiation levels, temperature ranges, temperature cycling, anticipated lifetime would be listed. This section explains how the design will meet those requirements.
- Electrical computer-aided engineering (ECAE) tools to be used
  - The FPGA designers will use a variety of sophisticated design tools. This section lists those software/prototyping tools planned for the work.

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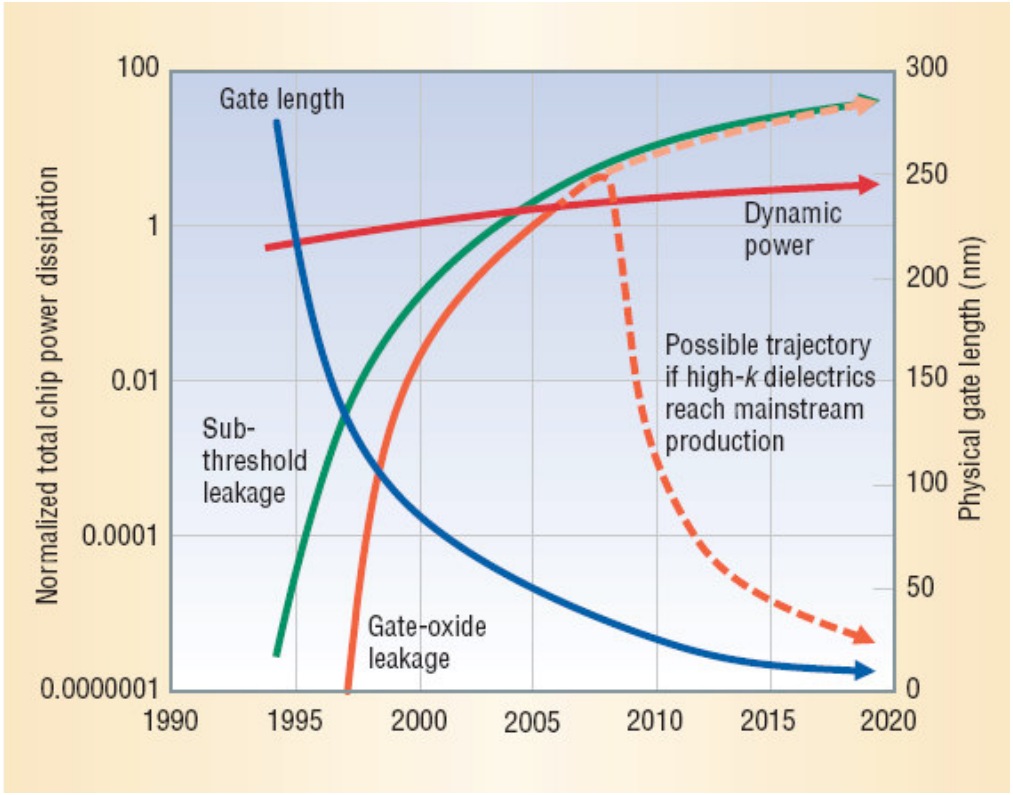
The *Graph* of FPGA Insertion

Static and Dynamic Power Dissipation versus physical gate length (nm)



International Technology Roadmap for Semiconductors (ITRS) 2001, 2002.

- **Managing FPGA power is the key engineering activity for all current and future FPGA qualification.**
- **Power and its effect on die temperature and hence on degradation mechanisms will determine the long term success or failure of FPGA designs.**
- ***Understanding an FPGA's power means understanding its design, technology and application.***

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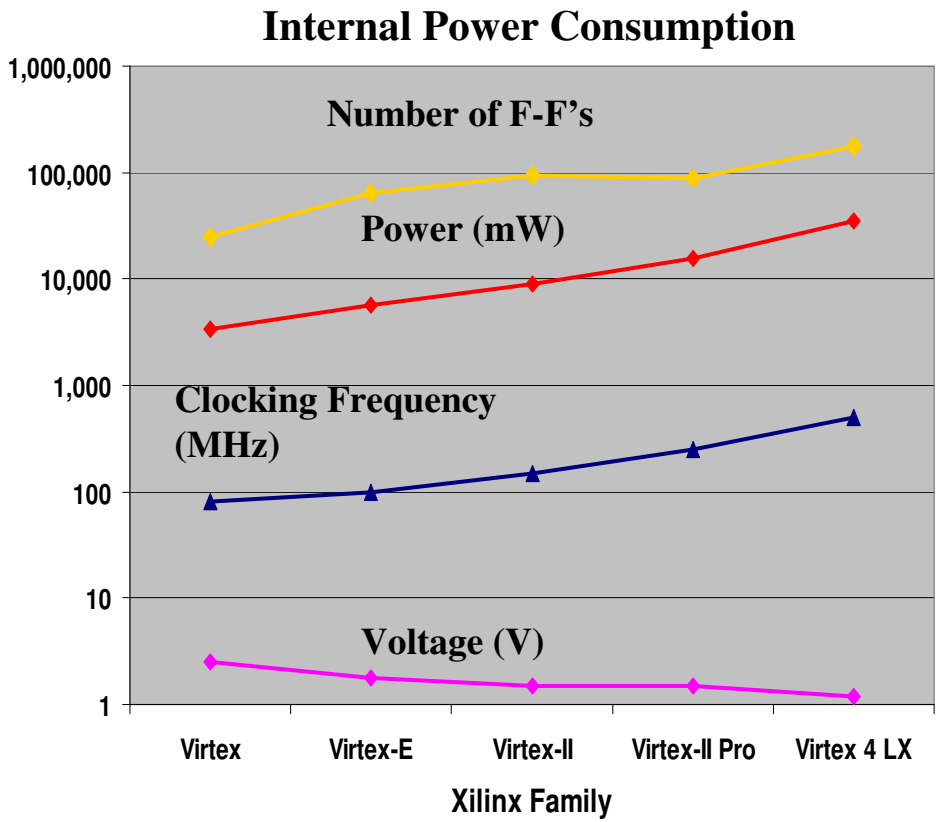
FPGA Power Modeling

(French/Wang/Anderson/Wirthlin - MAPLD 2005)

- **Number of logic blocks & maximum operating frequency track Moore's Law**
- **Voltage reduction is slower**
- **Resulting power increase is exponential**
- **Power needs to be a first class design constraint**



Power calculated assuming 80% device utilization, 80% peak clock frequency, 12.5% toggling rate. Internal logic only, no I/O.

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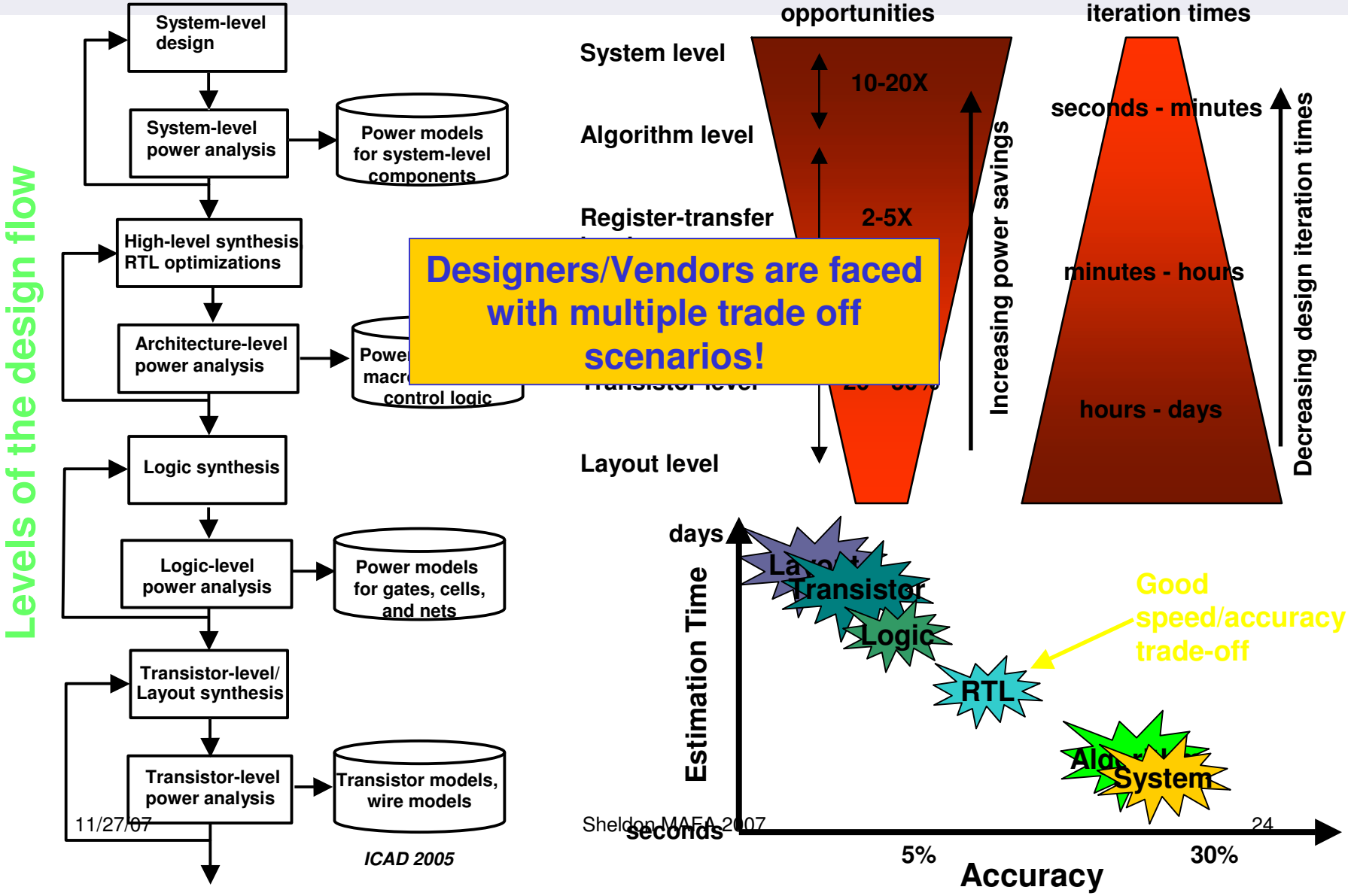
FPGA Power Estimation Flow



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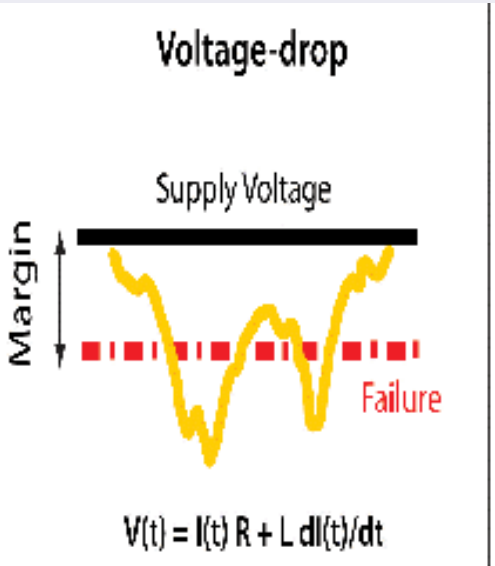
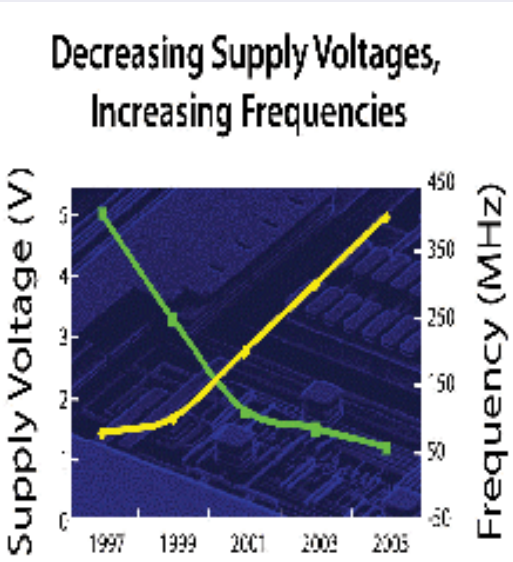
Smaller Geometry FPGAs and Voltage Requirements





- **As process geometries have shrunk, so too have the required supply voltages, but the frequencies have gone up, resulting in decreasing margins available to accommodate voltage-drop.**
- **If voltage drop is not limited, the consequences can be disastrous. If the voltage drop increases beyond the target threshold, the operating performance of the cell is reduced. Voltage drop also affects noise immunity, and under extreme conditions, leads to functional failure.**

Kitcher, Sep EETimes 2006

Device Specific Characterization

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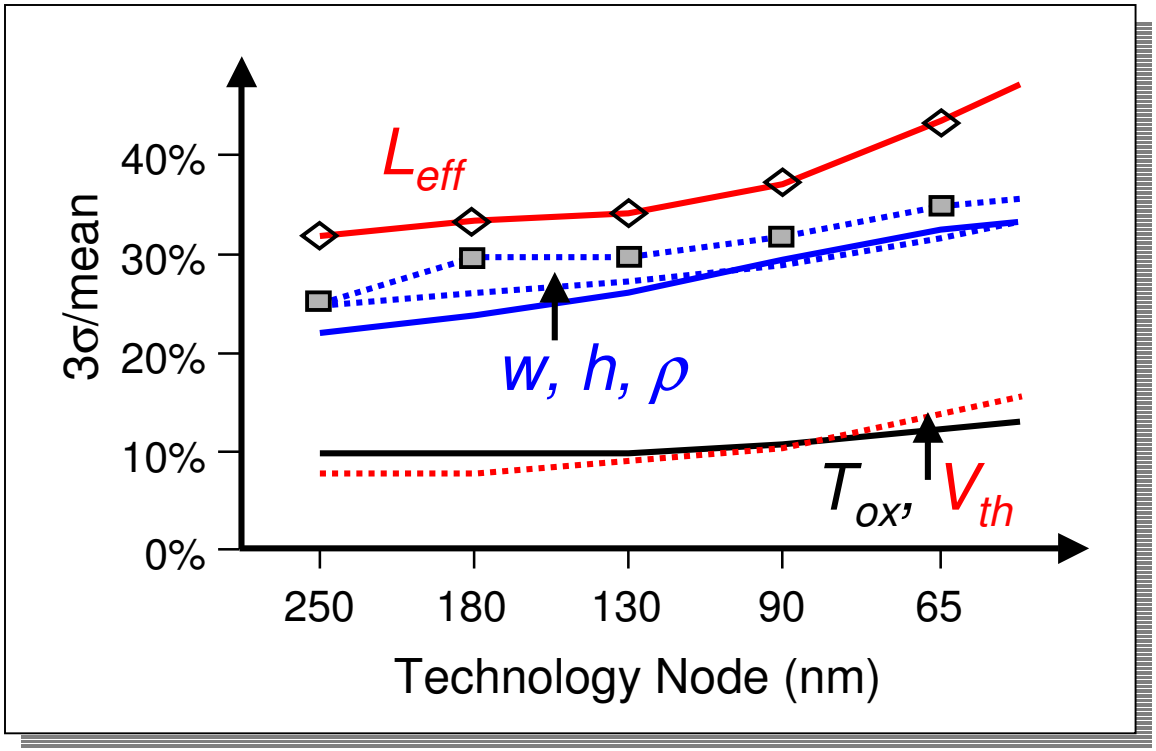
Process Variations vs. Scaling



- **Scaling related dynamic degradation effects are only going to get worse.**
- **Operating margins will decrease as uncontrollable technology variations increase.**
- **What was once manageable (i.e. limited/no impact on circuit performance) will become a measurable degradation.**

H. Qin UC Berkeley and S. Nassif, IBM

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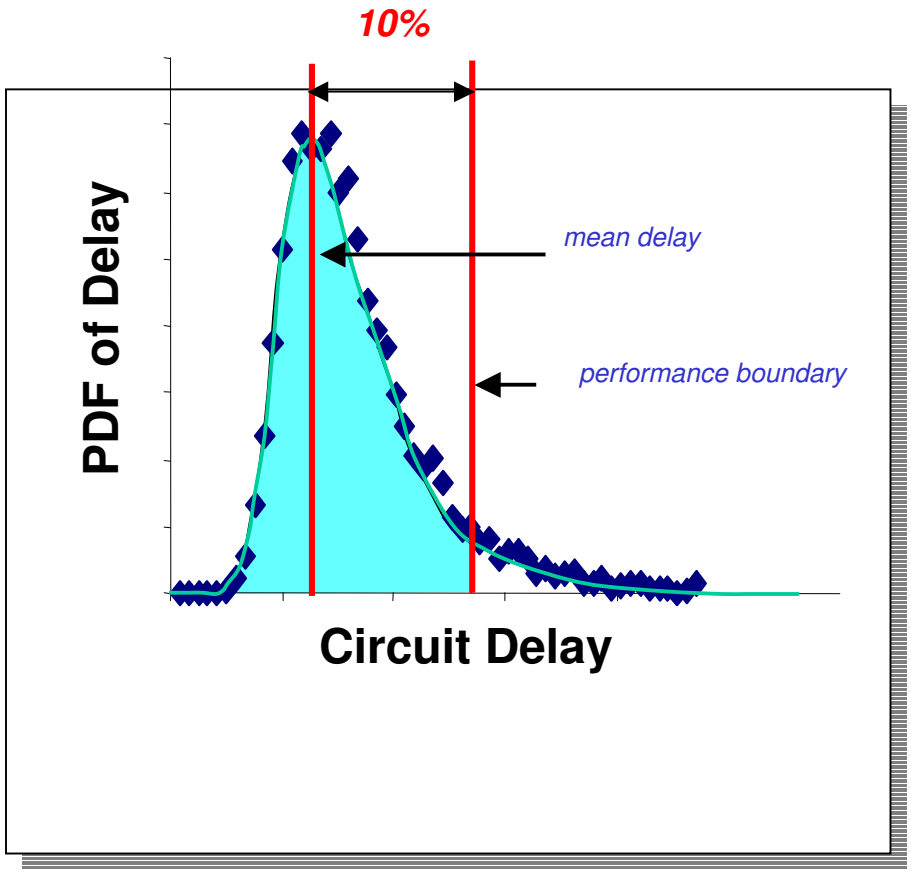
Successful Qualification of FPGAs - Application Sensitive



*Performance boundary = mean delay *(1σ +10%)*

- **Circuit delay due to resistive changes (failures) during operation are becoming the major qualification and reliability concern.**
- **These changes can be due to:**
  - **Antifuse ageing**
  - **hot carrier degradation, etc.**
- **Distributions of delay at t=0 often is non-linear due increased variations in voltage and geometrical parameters.**
- **This non-linearity will only continue to increase as a result of long term operation.**
- **Designs need to have a reliability benchmark/rating (antifuse consumption, LUT usage, etc). =>** ***Application specific qualification***

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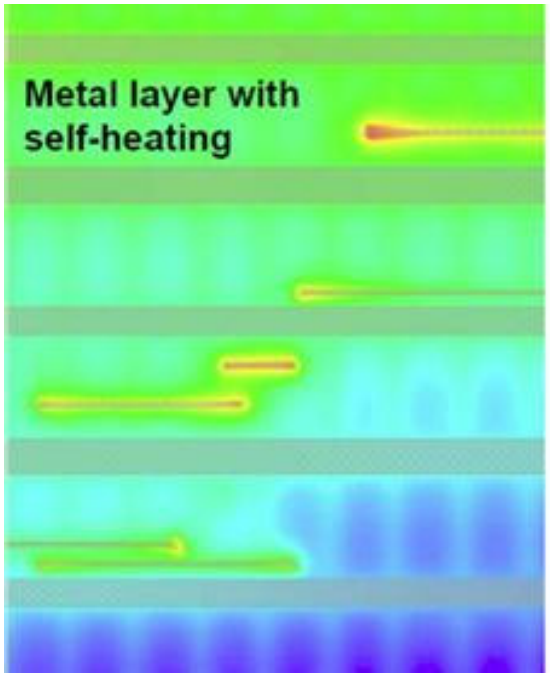
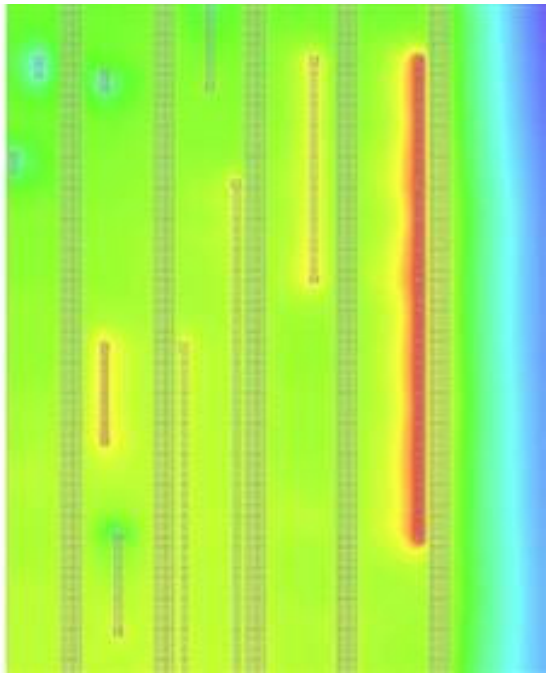
Example of Local Power/Temp Variations





- Electromigration in power and ground tracks causes timing problems, because the increased track resistance associated with a void can result in a corresponding voltage drop.
- This will, in turn, cause increased delays and noise susceptibility in affected logic gates as discussed above.
- Power and ground electromigration can also cause major functional errors to occur, because the voids may eventually lead to open circuits while the hillocks and whiskers may cause short circuits to neighboring wires.

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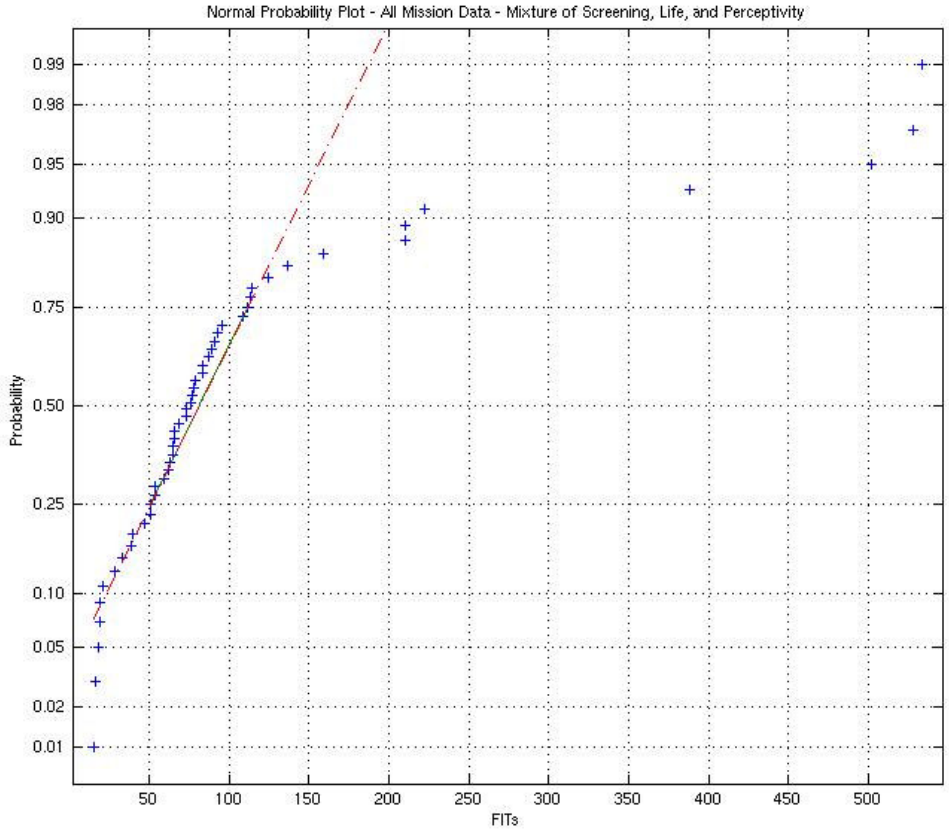
Example - Application Specific Risk Reduction



- **FIT Rates for JPL Missions using RTSX generation FPGAs**
- **JPL requirement that ALL designs have FIT Rate analysis using Aerospace calculator**
  - **Calculator inputs are design specific .adb files**
- **FIT Rates are calculated for various mission times, screening and design's timing sensitivity**
- **Approximately 85% of the distribution is normally distributed**
- **Outliers are flagged and in certain cases, re-designed via help of vendor.**

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Risk Methodologies Need to become more Sophisticated

- The assumption of constant failure rate and steady-state temperature may cause some errors in reliability prediction.
  - Failure rate might change even during the useful life of a device.
  - Temperature, itself, might also vary with time

JPL FPGA Risk Matrix Example

Activity	Low Risk	Medium Risk	High Risk
Technology			
Tech-1	X	X	
Tech-2	X		
Antifuse			
Antifuse-1	X	X	
Antifuse-2	X		
Design			
Design-1	X	X	
Design-2	X		
Screening			
Screening-1	X	X	
Screening-2	X		

$$Risk\,Factor(T,F,DS) = \sum_i a_i T_i + b_i F_i + c_i D_i + e_i S_i$$

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Federal Reserve Bank of San Francisco June 2005

- "Risk-management practices at financial institutions have undergone a quantitative revolution over the past decade or so."
- "Increasingly, financial firms rely on statistical models to measure and manage financial risks, ranging from market risks (such as exchange rate fluctuations) to credit risks (such as borrowers' default probabilities) to operational risks (such as expected losses due to fraudulent transactions)."
- "Such models have gained credibility because they provide a *coherent framework for identifying, analyzing and communicating these risks*. However, *models are only simplifications of reality and cannot capture every aspect of these risks*."

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Possible Gotcha - Subcontractors .vs. Primes

- Primes develop extensive FPGA guidelines, procedures, requirements, etc.
- Subcontractors sometimes ignore, disregard, disagree, etc.
- This discontinuity undermines effective FPGA insertion.

Backup

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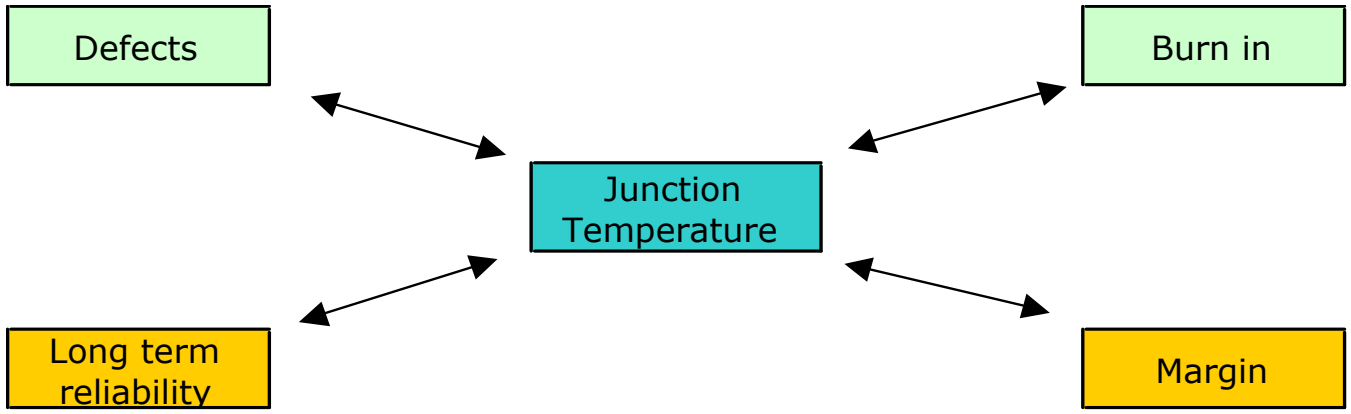
Relationship of Junction Temperature to Qualification

- **General overall concerns for qualification:**
  - **Workmanship (quality, level of defects)**
  - **Reliability (operation that causes long term failures)**
- ***The increase in junction temperature due to scaling is beginning to reduce the effectiveness of burn in and reduce the amount of margin available to prevent long term degradation***



Impact of Variations

- Circuit timing
  - Timing specifications have to be pushed further and further away from mean value.
  - Yield loss occurs otherwise.
- Power consumption:
  - Extra leakage at standby mode.
- Design methodology:
  - Traditional worst-case bounded design approach is wasteful on resources.
    - Redundancies in logic and circuits are necessary to ensure correct functionality; but they also come at expenses.
  - Besides speed and power, yield becomes another important parameter in circuit design.
    - Effective yield-aware design optimization methods are needed.