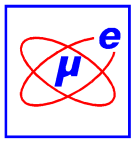


Micro-RDC

Microelectronics Research Development Corporation

Microelectronics Research Development Corporation

4775 Centennial Blvd. Suite #130
Colorado Spring, CO 80919
719-531-0805

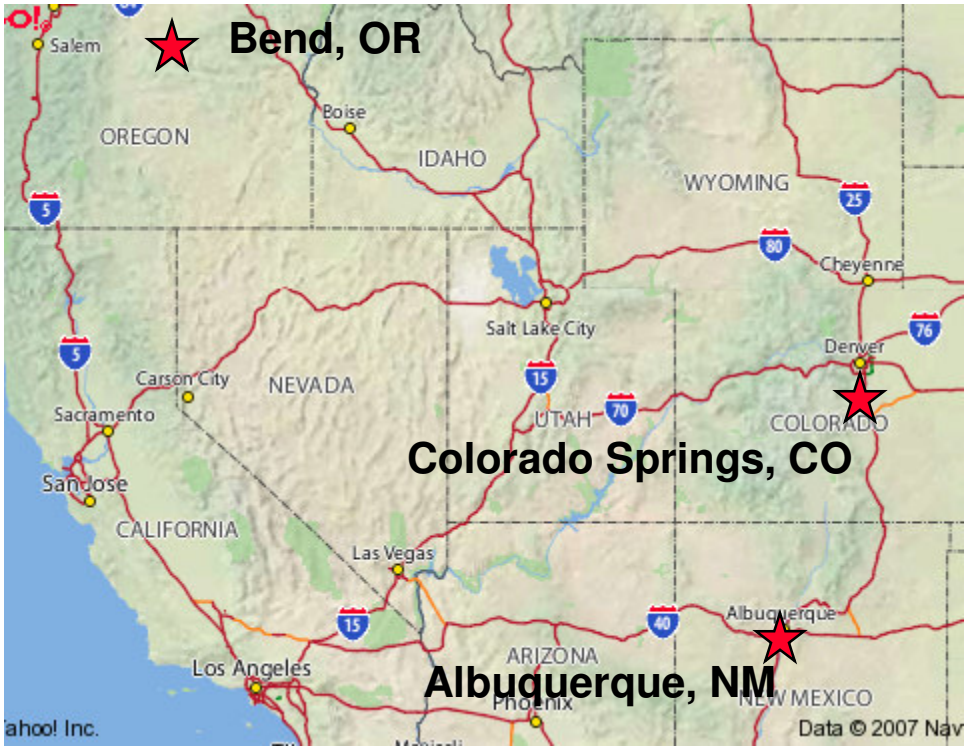
8102 Menaul Blvd. NE, Suites A, C, & D
Albuquerque, NM 87110
505-294-1962

2491 NE Twin Knolls Drive, Suite #106
Bend, OR 97701
541-382-9500

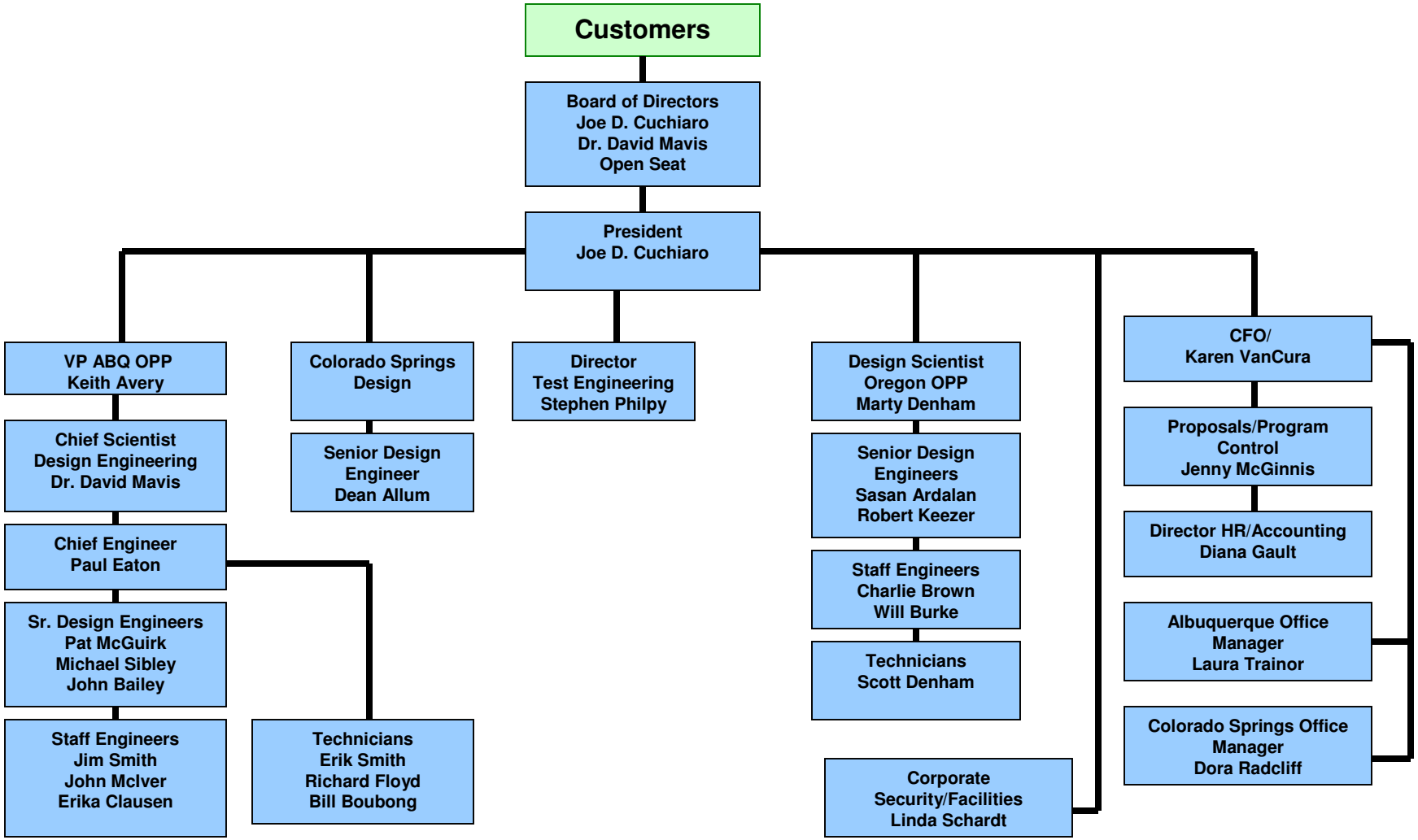

Microelectronics Research Development Corporation
Radiation Effects Research
RHBD Structured ASIC
Radiation Effects Testing
Cyclotron Institute

Micro-RDC

- **Employee Owned Small Business**
  - **27 Employees**
    - **21 Technical**
    - **6 Administrative**
  - **Three Offices**
    - **Colorado Springs, CO**
    - **Albuquerque, NM**
    - **Bend, OR**



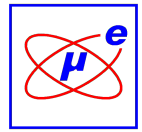
Organizational Structure



Micro-RDC Business Focus

- **Radiation Effects Research and Development**
- **Radiation Test Services**
- **Design Services**
- **“Product” Development**

Radiation Effects Research and Development



- **Technology Characterization**
- **Mitigation Approaches**

Radiation Effects Research and Development

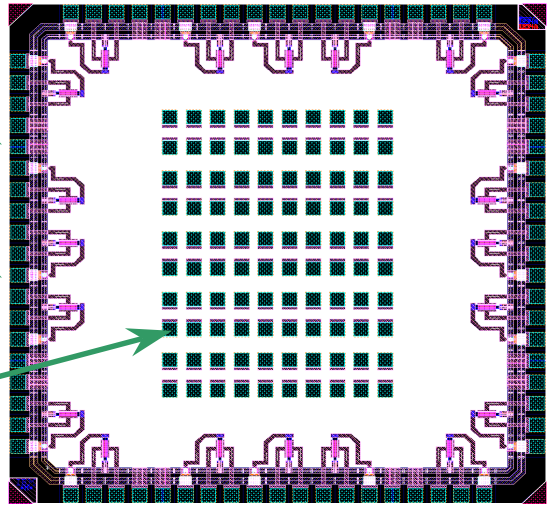
Radiation Effects on New Technologies

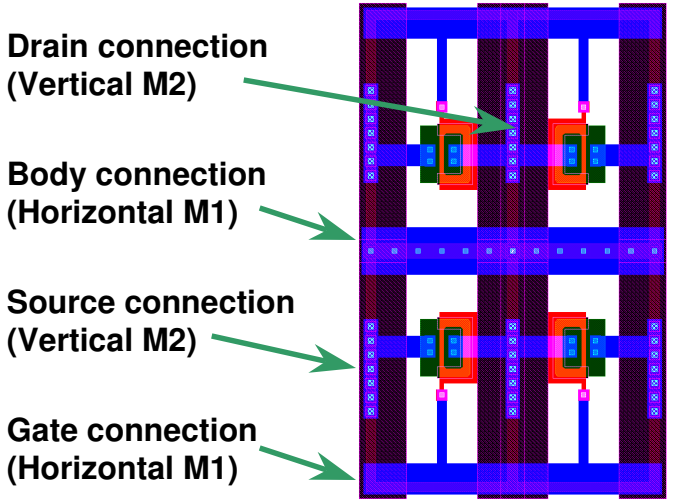
- Total Ionizing Dose
- Single Event Effects – Latch-Up, Upsets, Transients
- Prompt Dose/Dose Rate – Latch-Up, Upsets

Mitigation Approaches

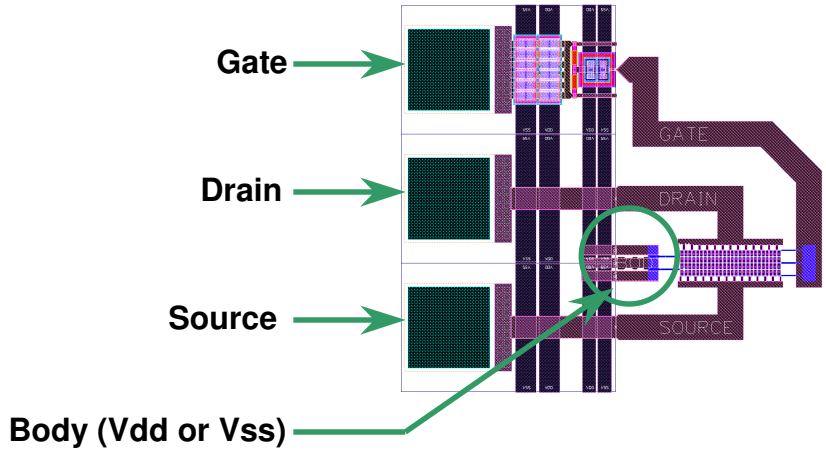
- Simulation
- Transistor Design
- Circuit Design
- Engineered Substrates

❑ Characterization Test Vehicles - Transistors



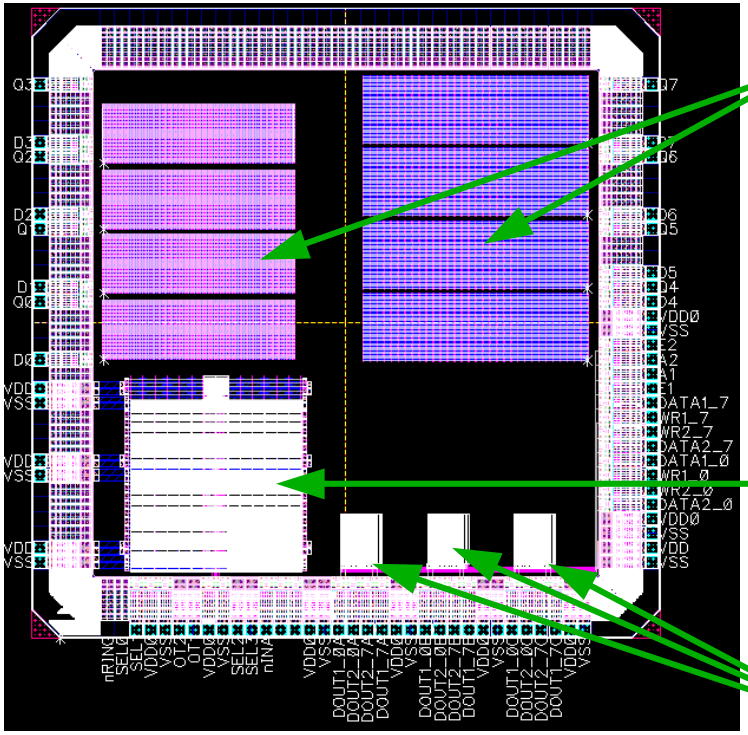


- ❑ Transistor arrays
  - Two dedicated test chip peripheries
  - Total of 40 different geometries
  - Full ESD gate protection for wire bonding
  - Co60 TID testing
- ❑ Probe pad arrays
  - Three test chip core drop ins
  - Total of 75 different geometries
  - Simple diode gate protection for probing
  - ARACOR TID testing



Radiation Effects Research and Development

❑ Characterization Test Vehicles - Circuits

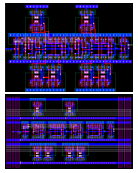


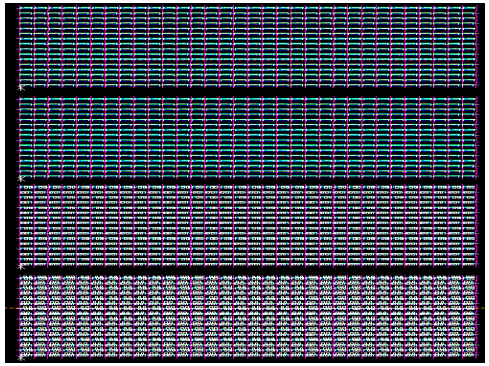
Integrated Test Chip

SET Pulse Measuring

Multiple Arrays

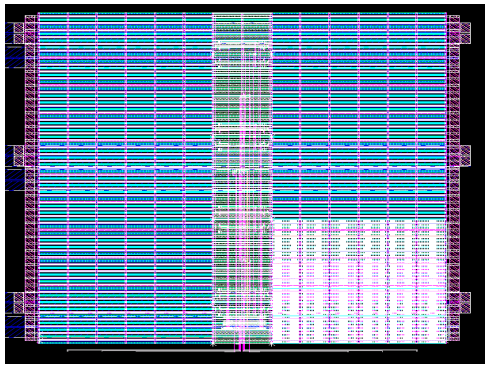
Multiple Configurations



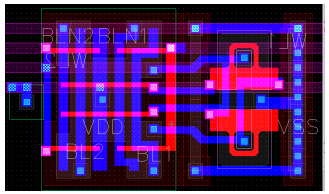


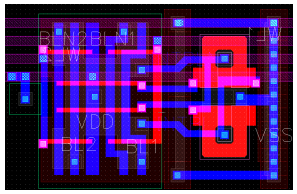
Delay Chains

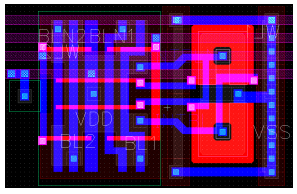
Timing Validation



Distributed SRAM







Radiation Effects Research and Development

Model Development and Simulation

- **Collection dynamics must be established by circuit response**
  - **Currents must decrease as voltages collapse (reduced E fields)**
  - **Pulse broadening will occur naturally (longer times will be needed to clear a fixed charge from the substrate)**

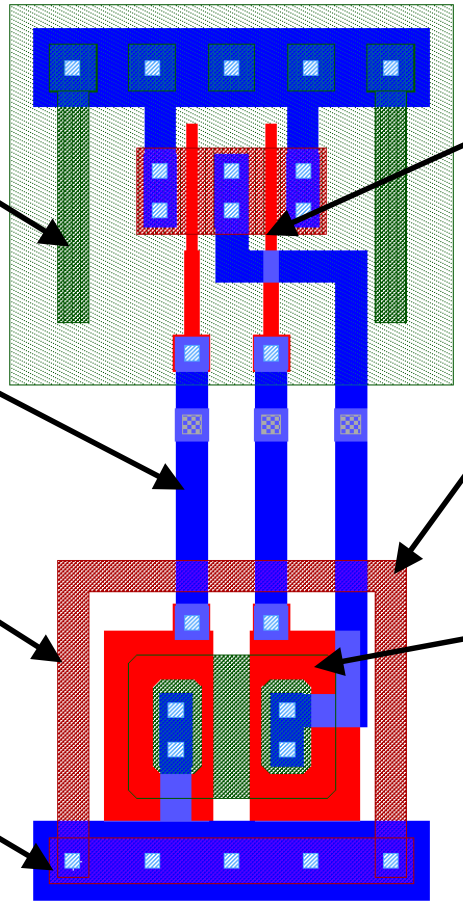
- **New SPICE model reflects these dynamics**
  - **Equivalent Collection Model (ECM) designed to capture the effects of node voltage collapse**
  - **Variational calculus to solve integral equation with variable limits:**

$$\text{Solve for } \mathrm{I}(t): \quad \int_0^{t(s)} \mathrm{I}(t')dt' = \mathrm{Q}(s), \quad \text{given } \mathrm{Q}(s=\infty)$$

  - **Note that $\mathrm{I}(t)$ is implicitly defined from an integral whose limit of integration varies according to the circuit response**
  - **Recombination / diffusion included by damping $\mathrm{Q}(s)$ as function of time**
  - **Boundary condition $\mathrm{Q}(s{=}\infty)$ likely dependent of V_{dd}**
  - **Implement solely with standard SPICE elements**

Radiation Effects Research and Development

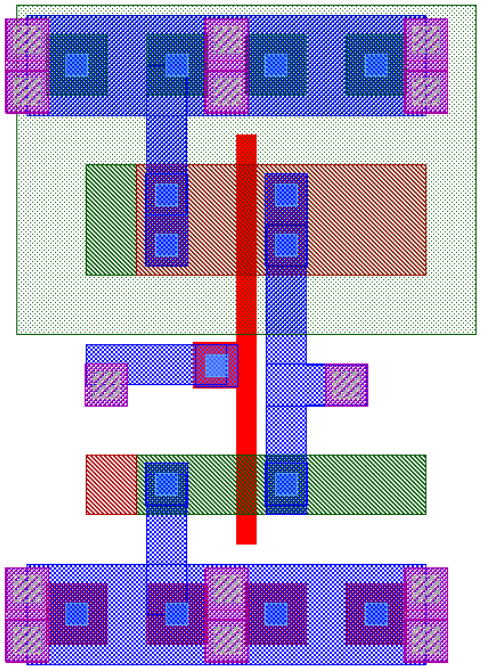
❑ Transistor Design

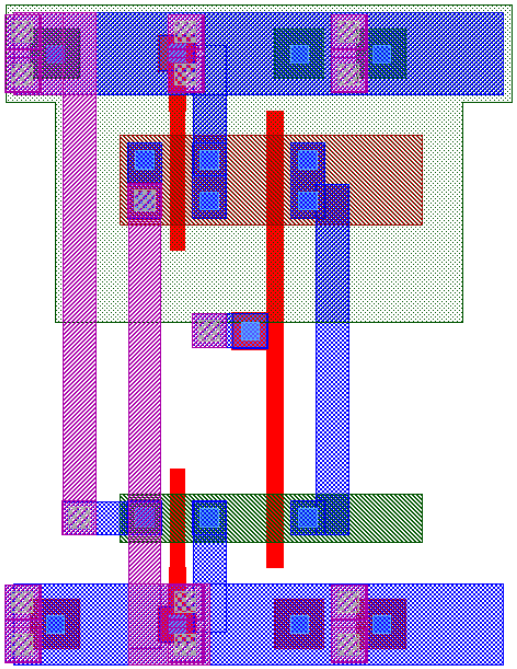


Radiation Effects Research and Development

Design Hardening

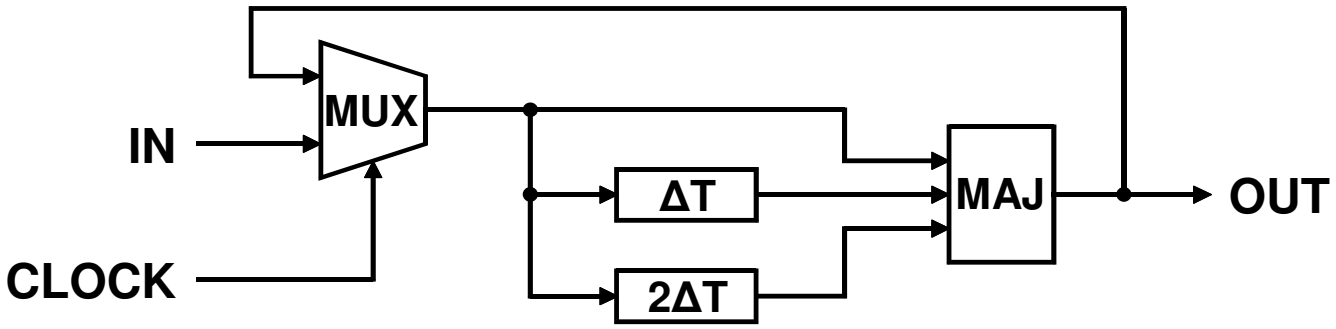
- Abutted substrate contacts on transistor sources provide recombination
- Gate isolated reverse biased junctions near critical nodes provide hard rail collection diodes





Circuit Design

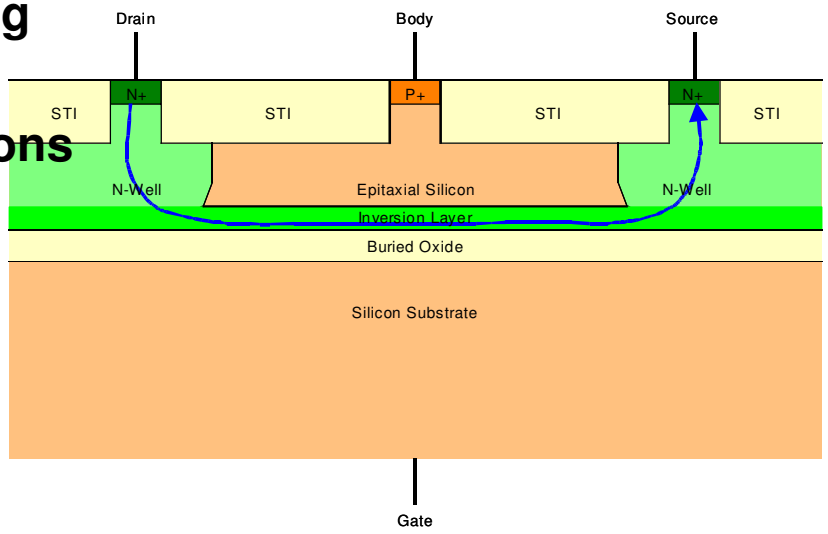
- Data latch SEU/SET mitigation
  - Temporal sampling to achieve both spatial and time redundancy
  - Variable sampling delay for hardness / performance tradeoff
  - Immune to multiple node strikes and transients on any node
  - Self scrubbing, does not integrate errors as normal TMR



- SRAM SEU mitigation
  - Conventional 4T storage with dual-port PMOS access
  - EDAC for single bit errors
  - Scrubbing to reduce multiple bit errors

Radiation Effects Research and Development

- **Substrate Engineering**
- **New method under investigation**
  - **Electric field induced inversion layer in place of HDBL**
  - **Can be located much closer to surface**
  - **Can remove charge through drift, rather than through diffusion and recombination**
- **Attractive for a number of reasons**
  - **Uses standard CMOS processing**
  - **Requires no mask changes**
  - **Requires no process modifications**



Radiation Effects Research and Development

Engineered Substrates

- Develop test methods to characterize
  - Lateral diffusion
  - Digital SET pulse widths
  - Upset threshold LETs
  - Latchup
  - Dose-rate charge collection

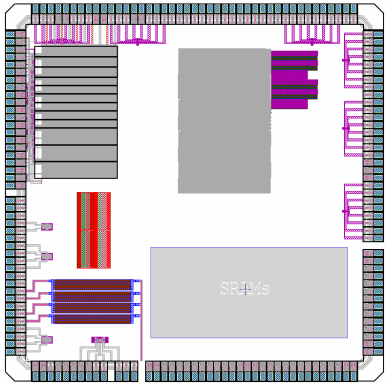


Figure 1. Layout of the entire test chip.

- Design and layout reusable test chip suite (in order of attack)
  - SRAM with various critical node separations
  - Digital SET shift registers retargeted to Jazz 180 nm
  - Transient propagation circuits
  - Diffusion, latchup, photo-diode, photo-transistor structures
  - Basic transistors to monitor device parametric parameters
- Support design and development with 3d-device simulations
  - CFDRC

Radiation Test Services

- Technology Characterization
- Total Ionizing Dose
- Single Event Effects
- ELDRS
- Prompt Dose

Radiation Test Services

- Follow Mil Std 883 Practices
- Total Ionizing Dose
- Single Event Effects
  - Latch-up
  - Upset
  - Transients
- Dose Rate/Prompt Dose
  - Latch-up
  - Upset
- Enhanced Low Dose Rate Effects (ELDRS)

Radiation Test Services

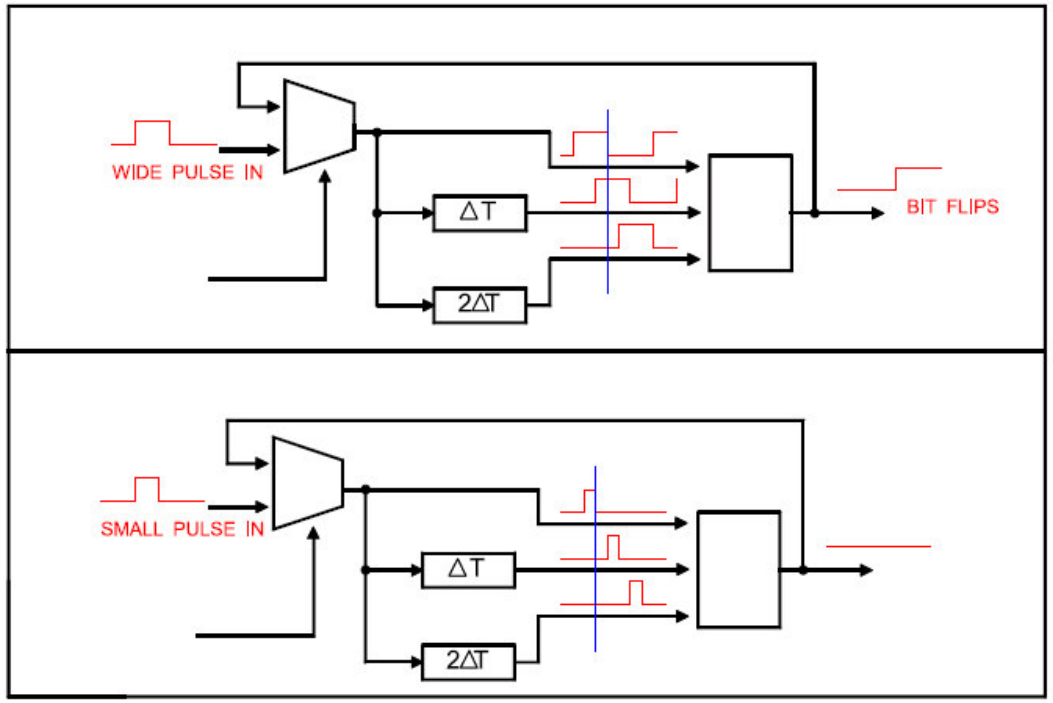
Facilities

- AFRL Cobalt 60, LEXR, Cesium, and Flash X-Ray
- Longmire Laboratory
- Berkeley Cyclotron
- Texas A&M Cyclotron
- Brookhaven National Lab – Tandem Van de Graaff
- Indiana University Cyclotron
- Etc.

Radiation Test Services

Variable Delay Temporal Latch

- Shift register immune to upset if transient width < ΔT filtering delay
- Vary ΔT with current starved delay chain
- Measure error cross section as function of ΔT



Least-Squares Fit Data Analysis

Mathematical statement of the problem

- **Data:** $y_i \pm \sigma_i, \quad i = 1,n$
- **Parameters:** $a_j, \quad j = 1,m$
- **Function:** $\mathrm{y}(x_i, \vec{a}), \quad x_i = independent\ variables$
- **Minimize Chi-Squared of the fit to the data:** $\mathrm{X}^2 = \sum_i \frac{1}{\sigma_i^2}\left[y_i - \mathrm{y}(x_i, \vec{a})\right]^2$
- **Solve:** $\frac{d\mathrm{X}^2}{da_j} = 0, \quad j = 1,m$

Generic least squares fitting method

- **Linearize:** $\vec{\beta} = \delta\vec{a} \cdot [\alpha]$
- **Iterate:** $\vec{a} \rightarrow \vec{a} + \delta\vec{a}$, where $\delta\vec{a} = \vec{\beta} \cdot [\varepsilon]$ and $[\varepsilon] = [\alpha]^{-1}$

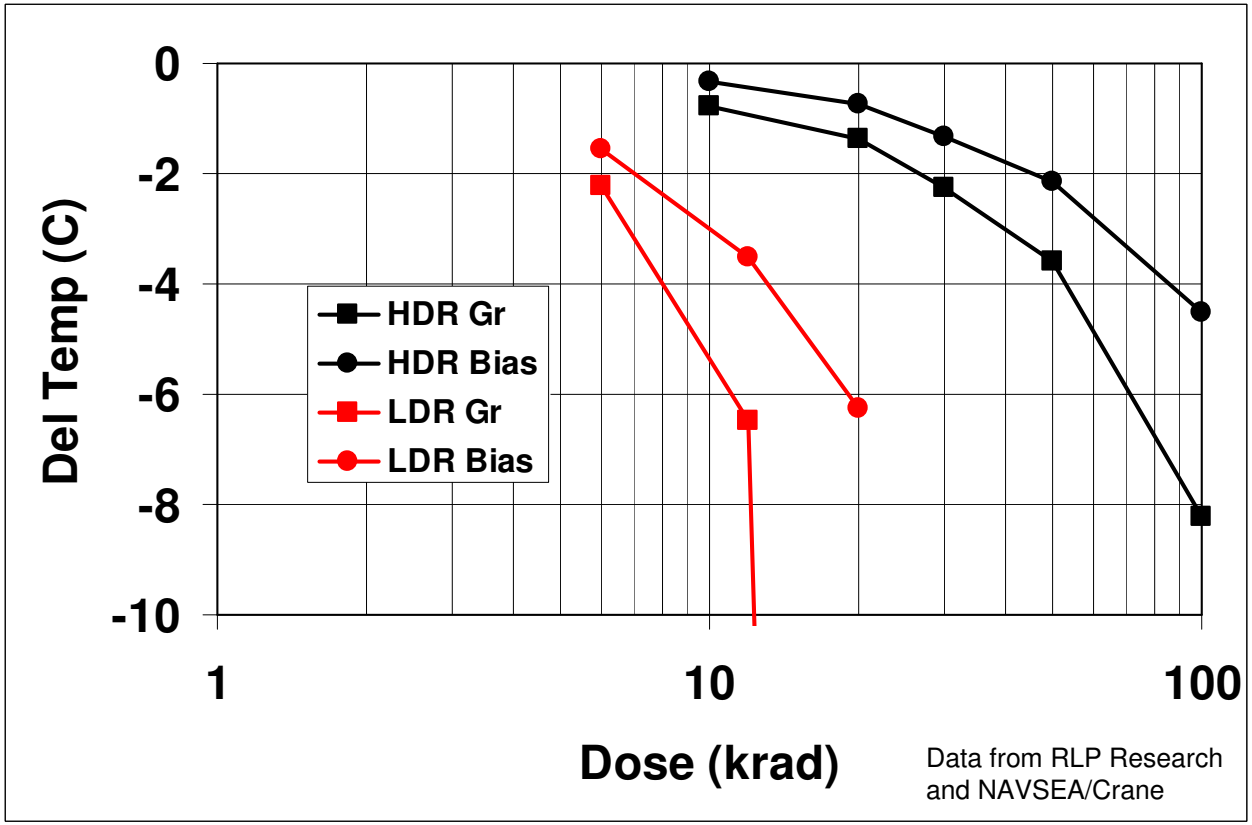
$$\beta_k = \sum_i \frac{1}{\sigma_i^2}\left[y_i - \mathrm{y}(x_i, \vec{a})\right]\frac{\partial y_i}{\partial a_k} \qquad \alpha_{jk} = \sum_i \frac{1}{\sigma_i^2}\frac{\partial y_i}{\partial a_j}\frac{\partial y_i}{\partial a_k}$$

- → **Best fit parameters** a_j **that minimize** X^2
- → **Parameter uncertainties** $\Delta a_j = \sqrt{\varepsilon_{jj}}$ **that reflect the data uncertainties**

Radiation Test Services

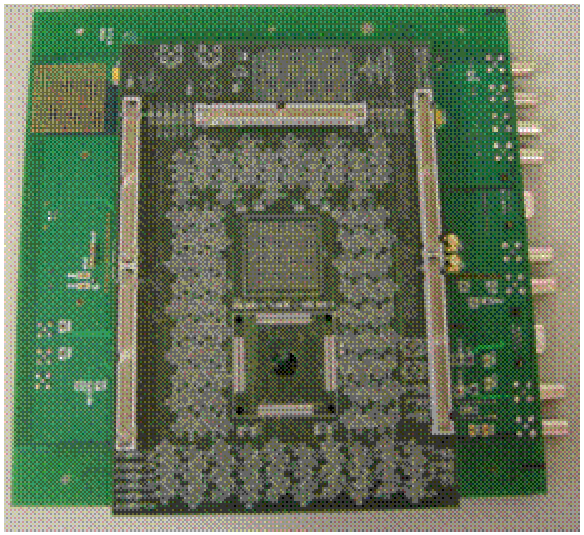
❑ Typical ELDRS Data

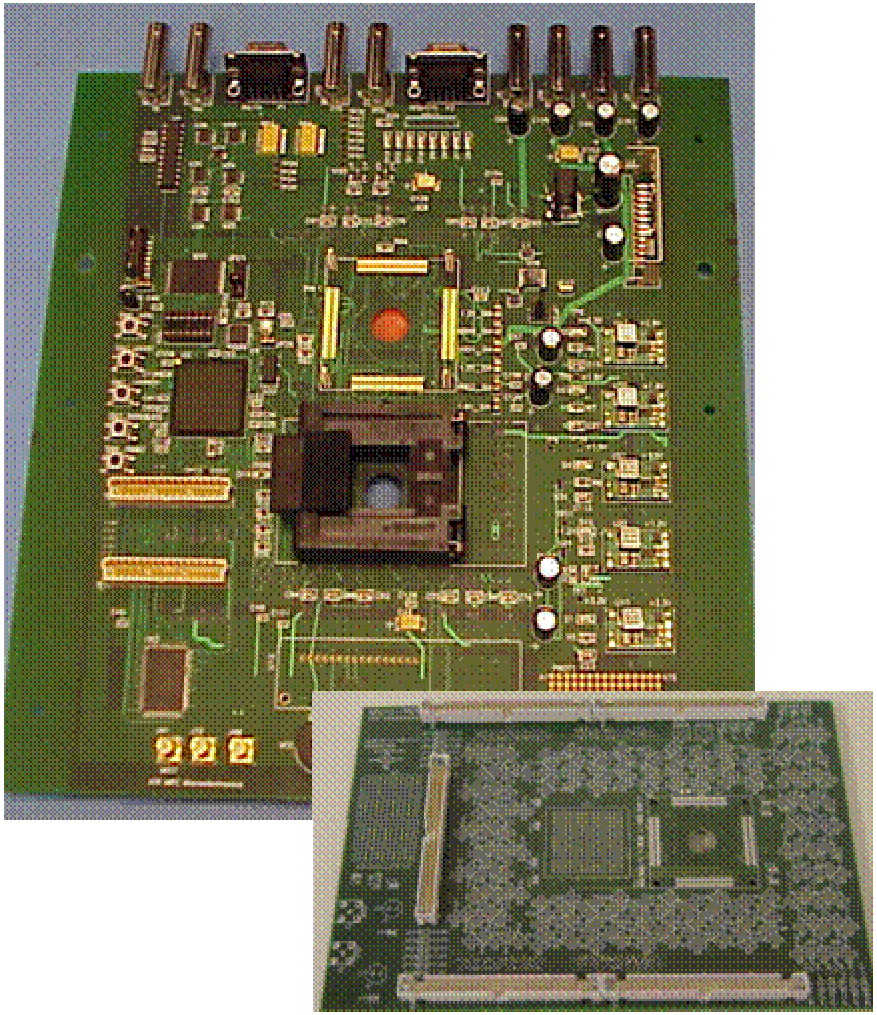
AD590 average change in ℃ vs. dose for high and low dose rate irradiation at two biases



Radiation Test Services

- **Test Hardware**
- **FPGA Test Board**
  - **Standard test platform**
  - **Custom daughter card**
  - **Leverage existing code**
  - **Used for multiple tests**





Design Services

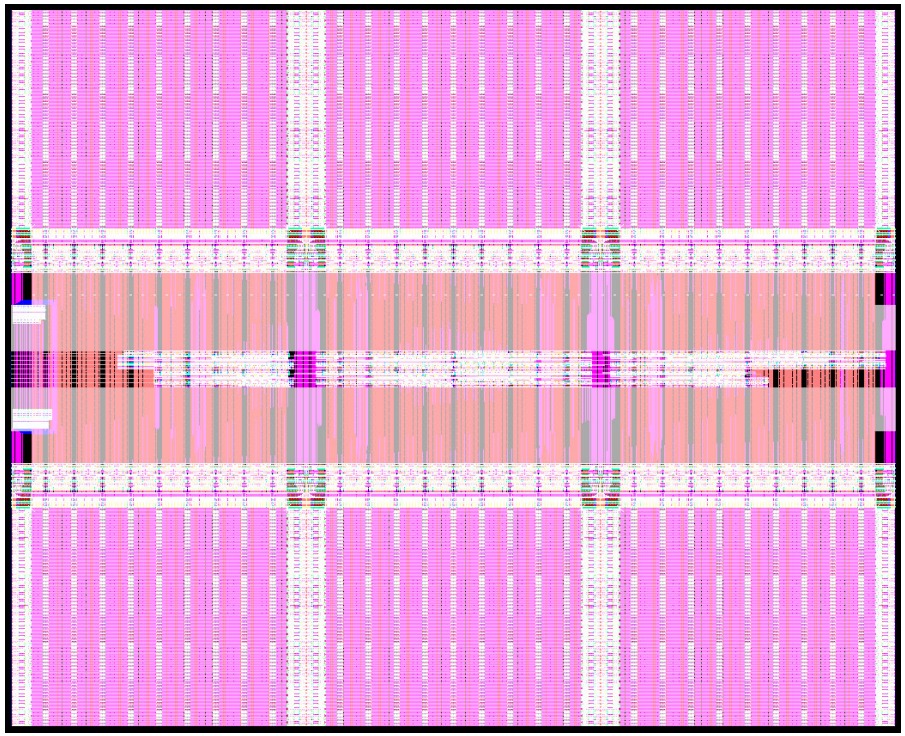
- Custom ASIC Development
- Circuit Design
- System Design
- High Density Packaging

Design Services

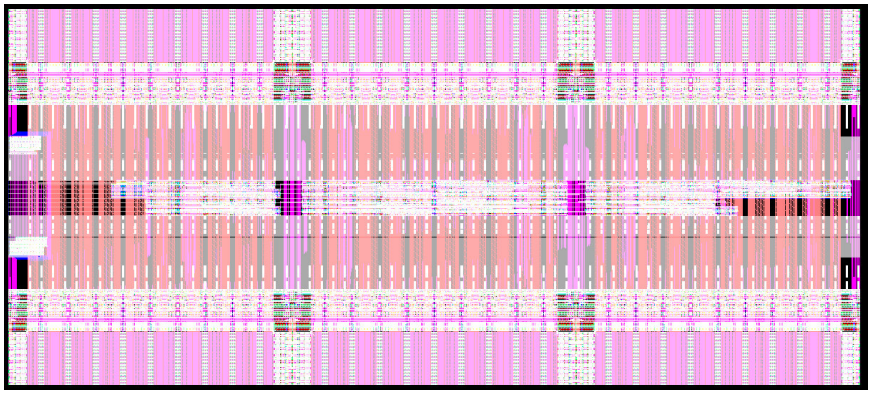
- **Research and Design of Integrated Circuits**
  - **In-house CAD tools**
    - **PC Based Design, Layout, and Simulation**
  - **Access to advanced CAD tools via AFRL SEAMS center**
    - **Workstation Based Design, Layout, and Simulation**
  - **Foundry Flexible**
- **Circuit Design for Responsive Space**
  - **SPA-U/S**
  - **ASIMs**
  - **Flex Circuit Module**
- **Advanced Packaging**
  - **Multi-Chip Modules**
  - **Chip-on-Board**

Design Services

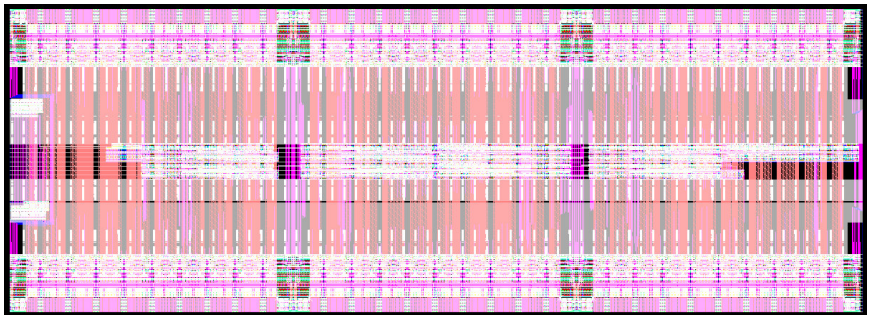
❑ Memory Development



1K X 72



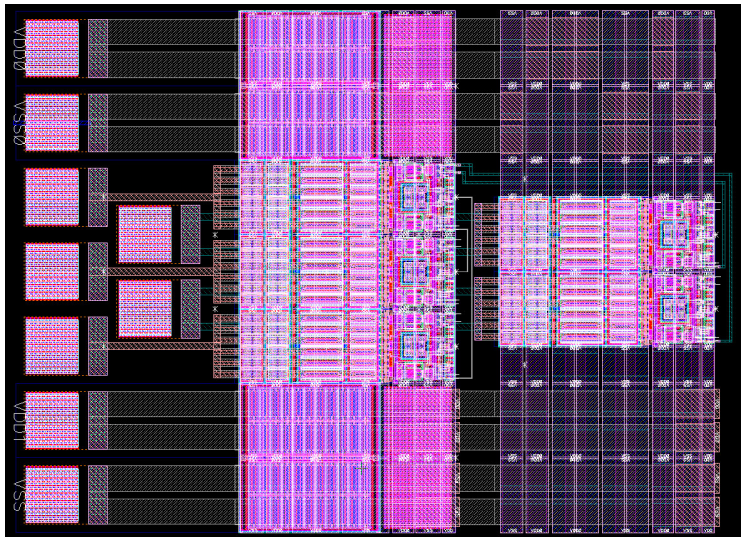
256 X 72

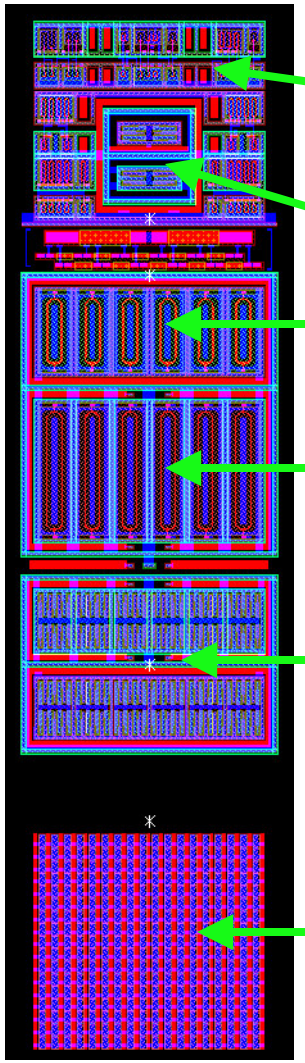


64 X 72

Design Services

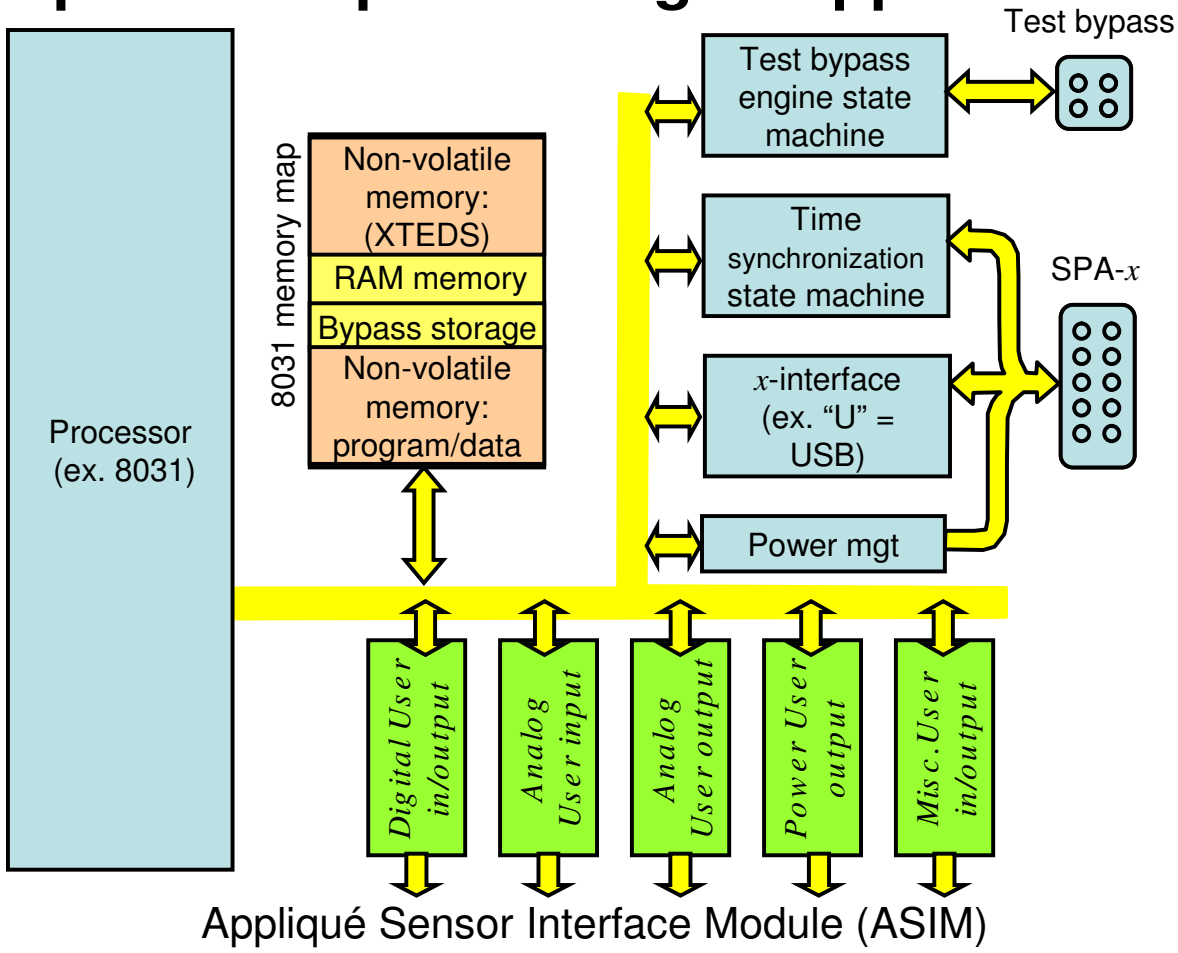
- **IO Development**
  - **IO Pad Pitch is 64 microns**
  - **Staggered Pad Layout**
  - **Effective Staggered Pad Pitch is 32 microns**
  - **Annular Gates for All NFET's and PFET's**





Design Services

❑ Responsive Space Design Support



Design Services

Key AT Technologies

- eFuses
  - Must be only destructively readable (i.e. damaging the component).
  - Antifuses and other programmable ROMs possible.
- Key Structures that disintegrate upon known reverse engineering efforts.
  - Key focus: Apply in-depth understanding of nano-scale IC technology to effectively prevent reverse engineering of critical keys.
- Ciphers
  - Maximal Length Linear Feedback Shift Registers (LFSRs)
    - Sufficiently large N or effectively large N required for sufficient entropy.
    - Complex LFSR-based scramblers that obfuscate tap sequences.
  - Other, included Blowfish, Twofish, and other Block Ciphers
- Cost-effective NVRAM
  - Ability to determine that a series of unauthorized attempts have been made to determine stored keys.
  - NVRAM (after several attempts) completely locks part out forever.
- Automation Tool Flow enhancements
- RHBD Techniques

“Product” Development

- **Structured ASIC**

"Product" Development

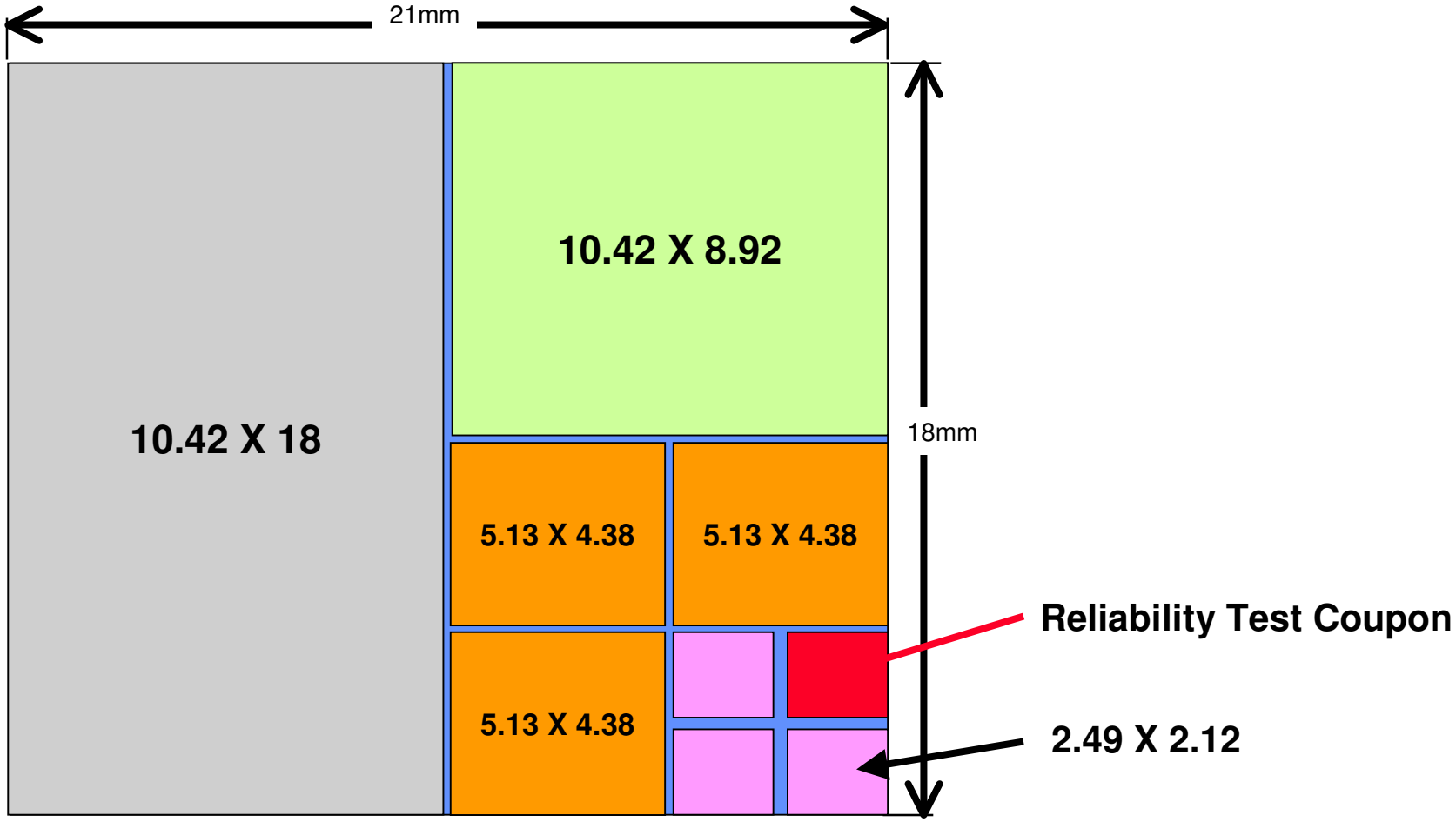
Structured ASIC Goals

- Current Options for Radiation Hardened Parts
  - Custom/Standard Cell ASIC Design
  - Rad-Hard by Process Foundry
- RHBD on Structured ASIC
  - Use radiation hardening by design (Micro-RDC)
  - Leverage commercial foundry
  - Leverage commercial structured ASIC
    - Existing Architecture (ViASIC ViaMask)
    - Existing Tool Set (ViASIC ViaPath)
  - Reduce design cycle
  - Reduce fabrication cost

Provide Rad-Hard Devices in Timely Manner at Reasonable Cost

“Product” Development

❑ Structured ASIC Reticle



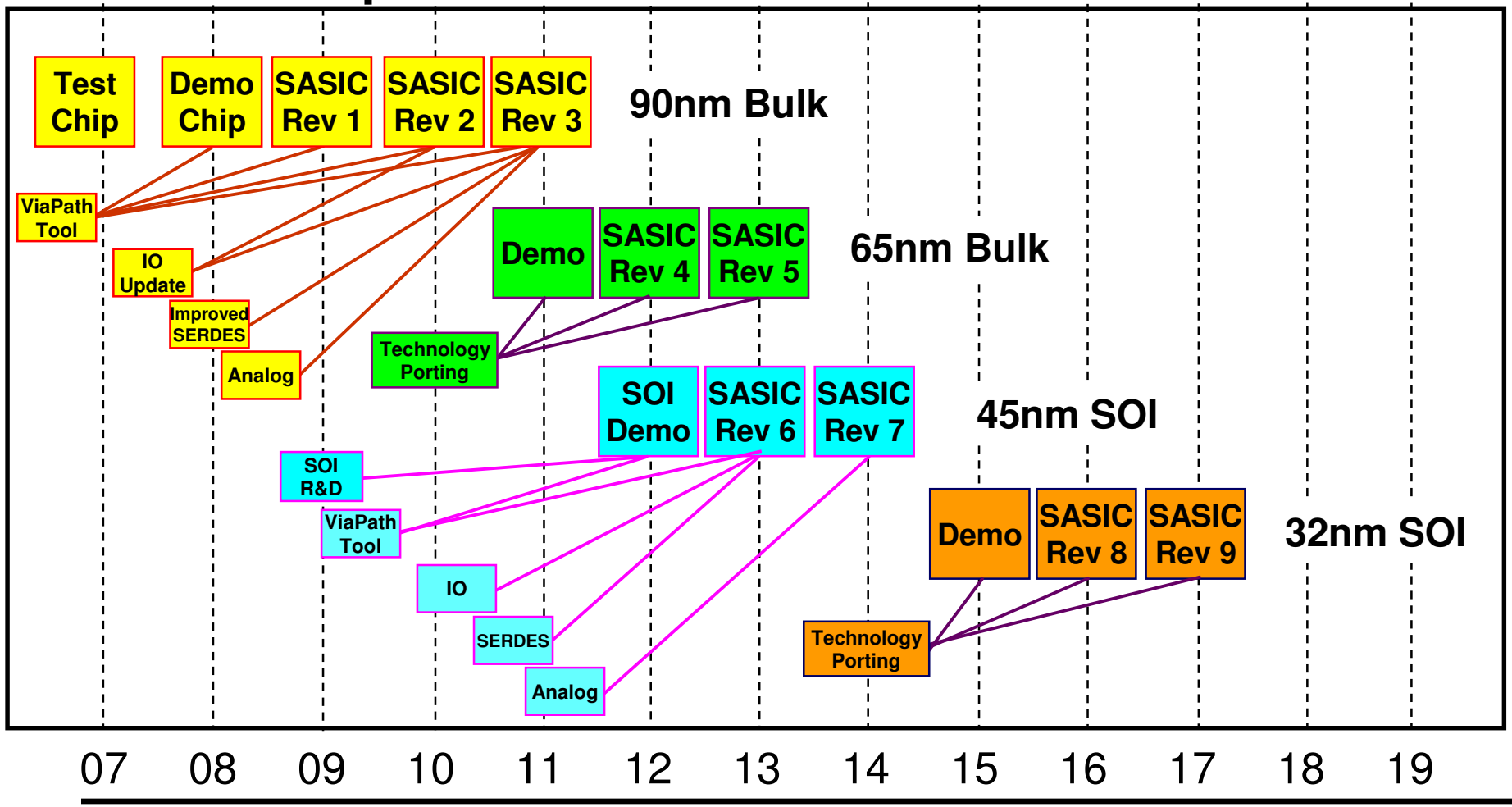
"Product" Development

Structrued ASIC Chip Size and Features						
Chip	Size (mm^2)	Macros	Memory (bits)		Logic (Equivalent Gates)	IO
			Embedded	Block		
Large	187.56	SERDES, PLL/DLL	1828710	?	2532060	LVDS, CMOS ~330 Regular ~600 Staggered
Medium	92.95	SERDES, PLL/DLL	906227	?	1254776	LVDS, CMOS ~200 Regular ~375 Staggered
Small	22.47	None	219077	None	303337	LVDS, CMOS ~120 Regular ~200 Staggered
X-Small	4.85	None	47334	None	65540	CMOS ~50 Regular

Block Memory: ~15mm^2 per Mbit
SERDES: 1.125 GHz Physical Layer Only
PLL/DLL: 100MHz – 1.25GHz
LVDS IO: Number of transceiver pairs is TBD.
CMOS IO: 2.5V standard input, output, bi-direct, etc.

"Product" Development

❑ Roadmap



“Product” Development

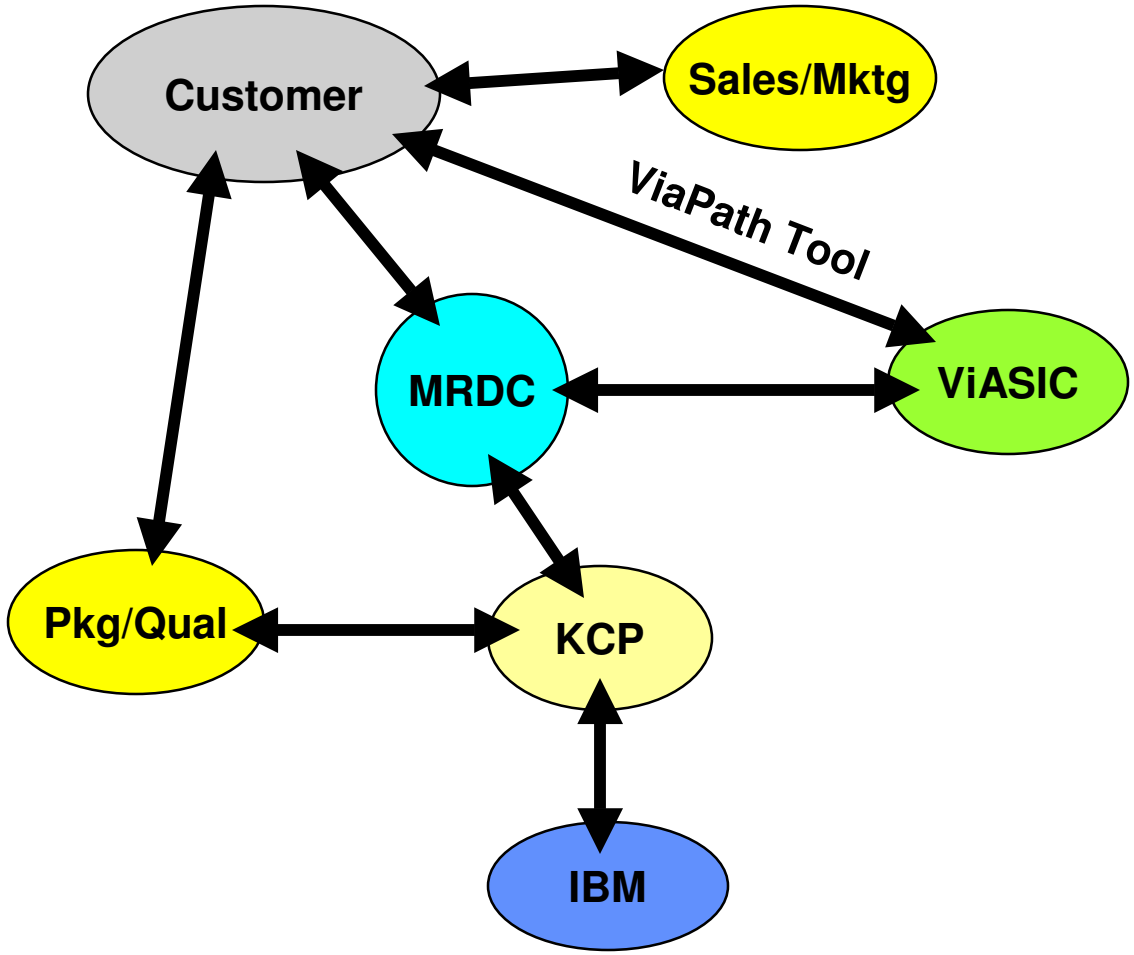
❑ Product Flow

Inputs:

- Concept
- VHDL/Verilog
- ViaPath GDSII

Outputs:

- Bare Die
- Packaged Parts
- Qualified Parts



Summary

- Tightly held employee owned company
- Leaders in Radiation Effects
  - Research, Mitigation, Test, and Data Analysis
- Single Event Transient Pioneers
- Developing Broad-based Test Capability
- Design Capability
  - IC's, Circuits, Systems
- Leveraging R&D Into "Products"
  - Structured ASIC