Ramon Chips, Haifa, Israel

Technion 1925

2000

Ramon Chips

Ramon Chips is named in memory of Col. Ilan Ramon, Israeli astronaut who died on board the Columbia space shuttle, 1/2/2003

RadSafe™ Technology
and
JPEG200 image compression ASSP

Prof. Ran Ginosar, CEO, Ramon Chips

MAFA, November 2007

Summary

- RadSafe™: Technology for RH ASICs
  - Rad-Hard-by-design
  - ASICs designed "normally" – standard EDA
  - On commercial CMOS processes
- Examples
  - FPGA conversions
  - LEON3-based SoC
    - 150 MHz, dual-core
  - JPEG2000 encoder
    - 44 Mpix/sec, 1 Tops
    - 4Mbit + 500Kgates, 30 M Tx, < 3W

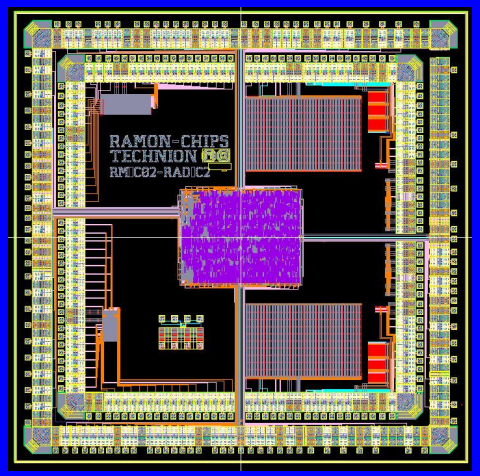
Ramon Chips History

- 2002-2004 research at Technion—Israel Institute of Technology
- Incorporated in 2004
- Privately held
- Already made, qualified and delivered several Rad-Hard ASICs

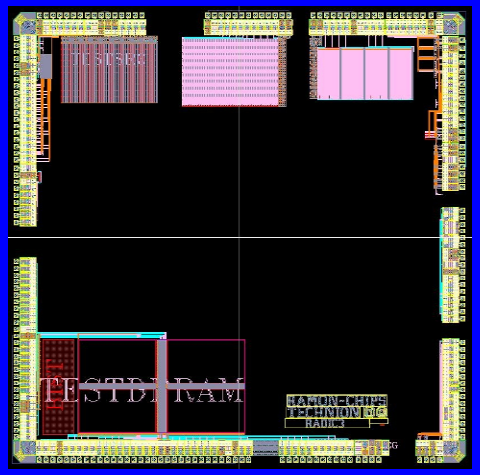
Goals

- Rad-Hard
- Low cost
- Short time-to-product

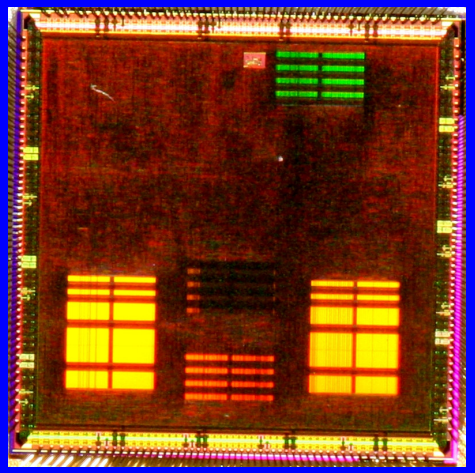
Various Chips



FPGA conversion



Radiation & qualification test



LEON3 SoC prototype

Ramon Chips Technology

- RadSafe™ – Rad Hard By Design
  - Standard commercial 0.18u CMOS process
  - Special libraries (our own)
  - Special methodology
  - Standard EDA and flow for ASIC design
- Why use a standard commercial process?
  - Inexpensive
  - Reliable
  - High performance
  - Available: Can fabricate any time
- Result: RH infrastructure for normally designed ASICs

TID protection

- Achieved by geometry
  - At transistor level
- Result: RH levels (300 Krad)
  - All space missions
  - Long life

Latch Up (SEL) protection

- Achieved by geometry
  - At transistor level
- Result: No SEL ever detected
  - At LET above 100 MeV·cm^2/mg

SET protection

- Glitch filters
  - No delays inserted
- Special methodology
  - No asynchronous signals
  - Special clock trees

SEU protection (flip-flops)

- Special FFs
  - Continuous self-correction
  - Spread wider than heavy-ion impact area
- SEU tests:
  - Less than 10^{-12} errors/bit/ day [LEO]
  - LET threshold 38 MeV·cm^2/mg
  - Tested up to LET above 100 MeV·cm^2/mg

SEU protection (SRAM cores)

- EDAC (optional)
- Special layout / placement
  - Separated bits of same word
- SEU levels in SRAM
  - Less than 2×10^{-7} errors/bit/ day [LEO]
  - LET threshold 3 MeV·cm^2/mg
  - Tested up to LET above 100 MeV·cm^2/mg
  - In tests, all errors were corrected by EDAC
    - Typical MTBF > 1,000 years

SRAM cores

- Single port SRAM
  - Speed >250MHz
- Dual port SRAM
  - Speed >120MHz
- Power 2nW/MHz/bit

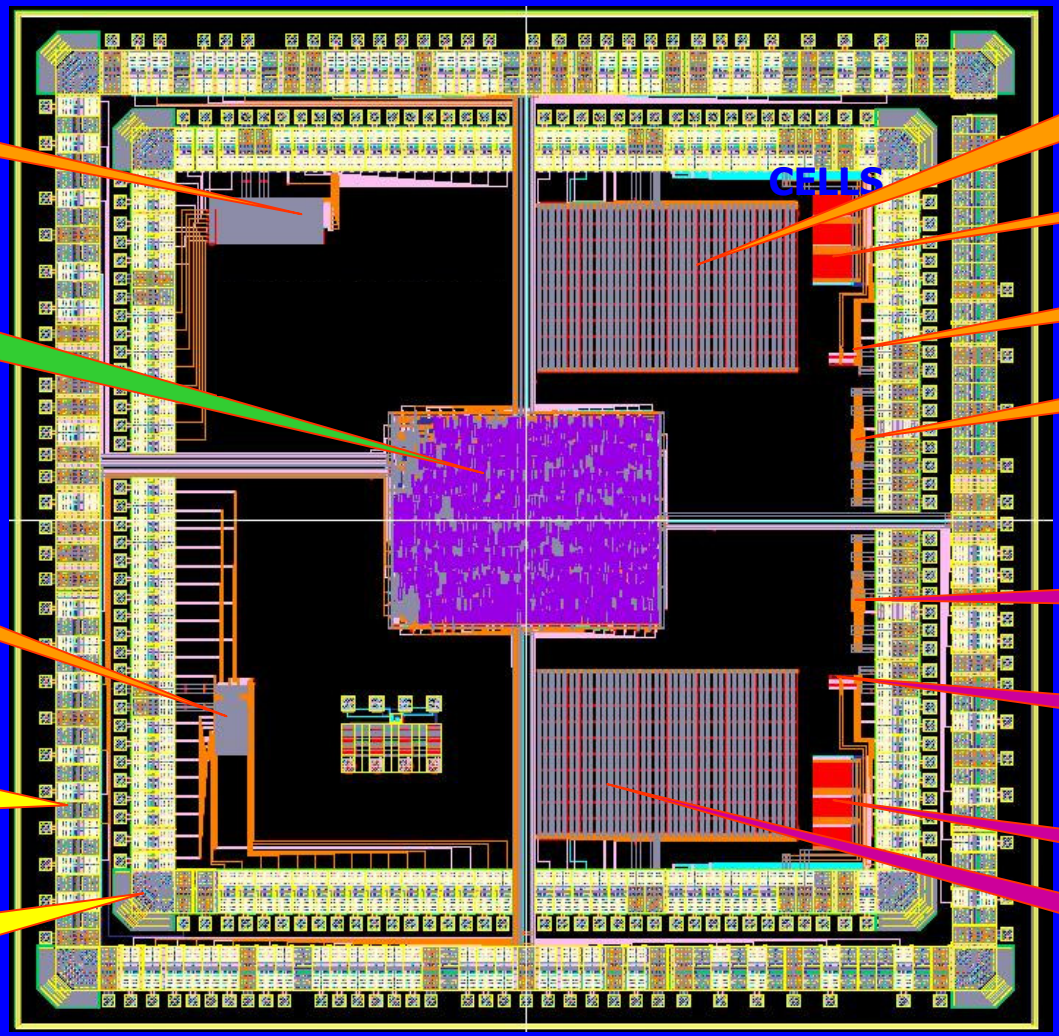
RH Libraries

- Logic standard cell library
  - >80 cells
  - 100—200 MHz
  - 1.8V and 3.3V
- I/O cell library
  - LVTTL, LVCMOS, LVDS, 5Vtolerant, Cold Spare, SSTL, AGP
  - High speed I/O > 400 Mbits/sec
- SRAM
- Digital DLL
- Libraries enable large chips
  - 5 Mgates or 8 Mbit or combinations

RH Physical Design

- Robust layout cells and methods
  - Solid power grid
  - Special interconnect design rules
  - Special via design rules
  - Special stress relief rules
  - Rad-Hard ESD cells

First Test Chip (1.8+3.3 V)



SRAM 1.8V

Functional logic

DLL 1.8V

Logic Pad-ring

Test Pad-ring

1.8V Shift Reg

1.8V Ring Osc

1.8V Lib Cells

1.8V Transistors

3.3V Transistors

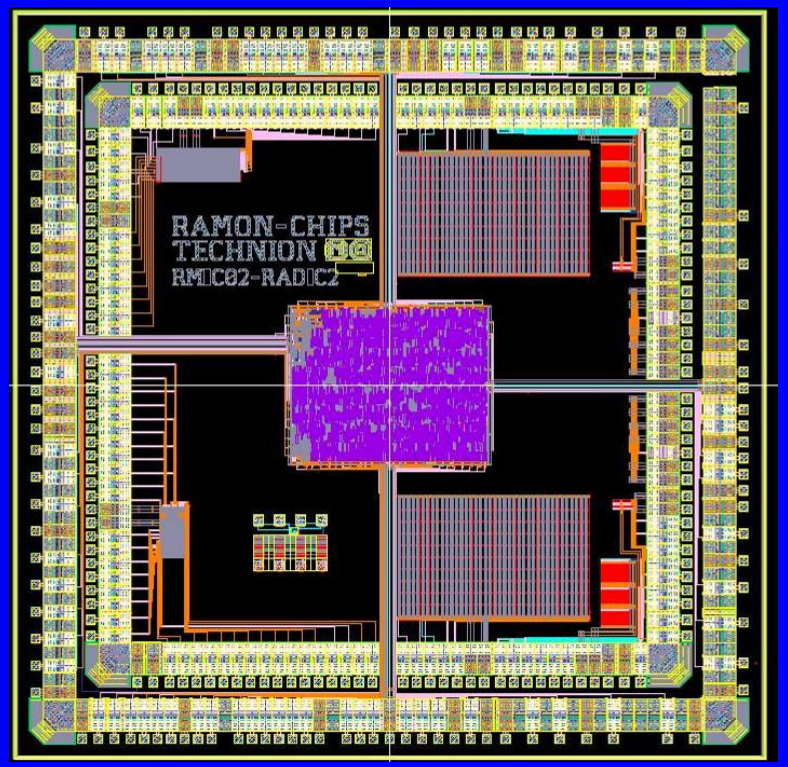
3.3V Lib cells

3.3VRing Osc

3.3V Shift Reg

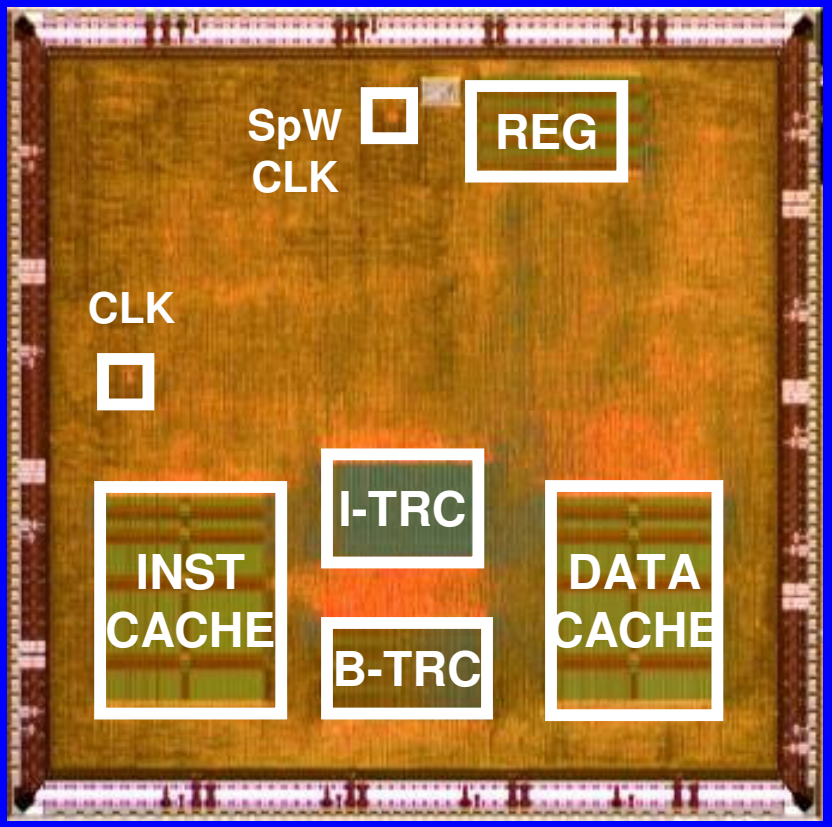
FPGA→ASIC Conversion

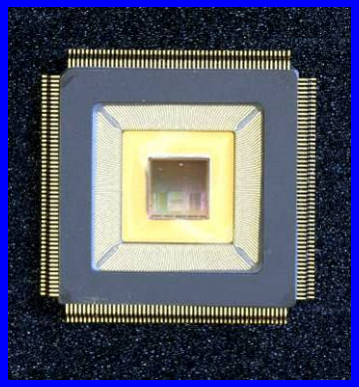
- For a SAR payload
  - Transmitter control
- 3x faster
- Lower power
  - Reduced > 95%
- Shared die with a test chip



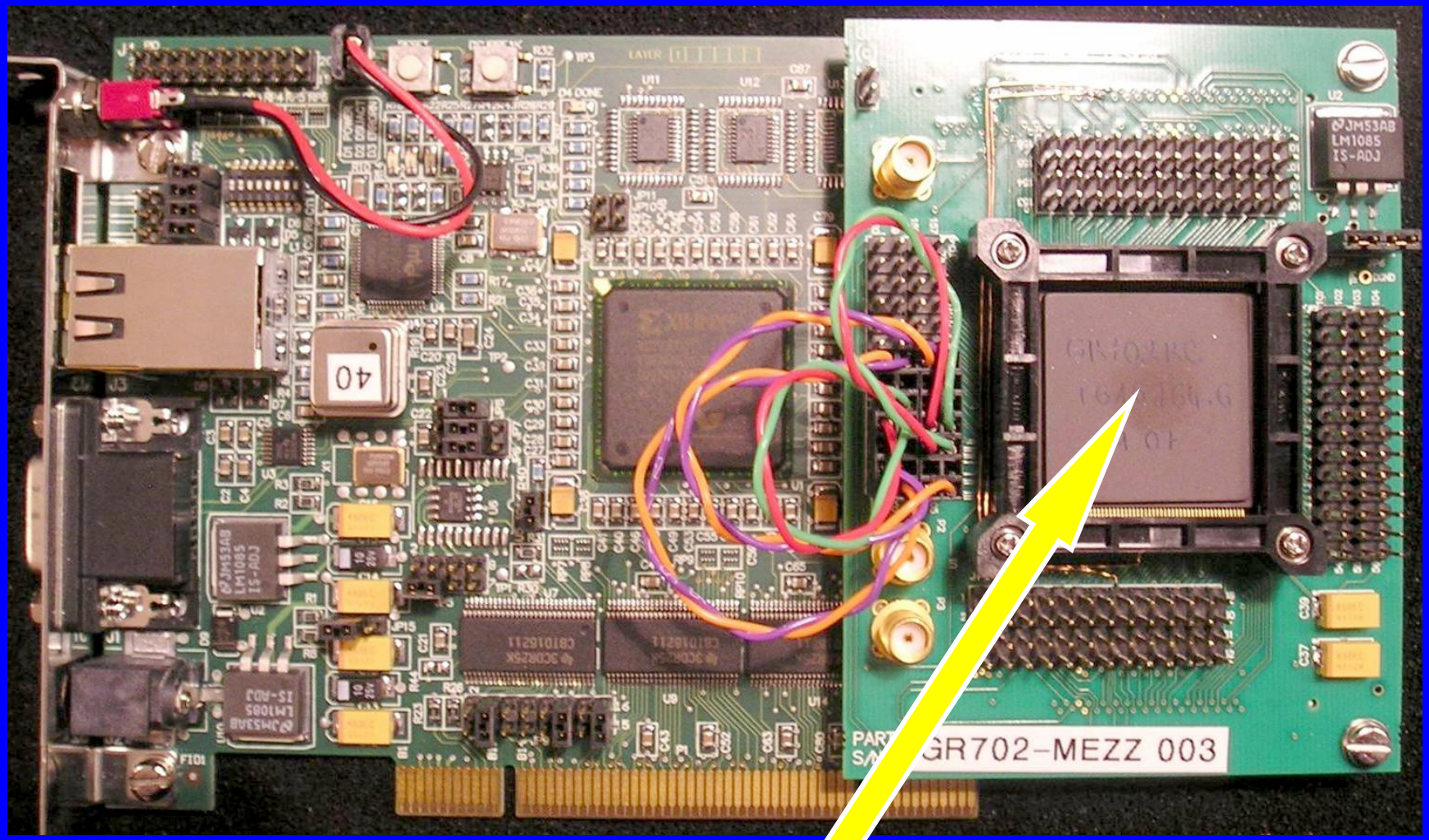
LEON3FT SoC

- Prototype in 2006
  - GR702RC
- Tested:
  - 120 MHz (CPU)
  - 250 Mbps (SpW)
  - All SEUs corrected





GR702RC SoC Test Board



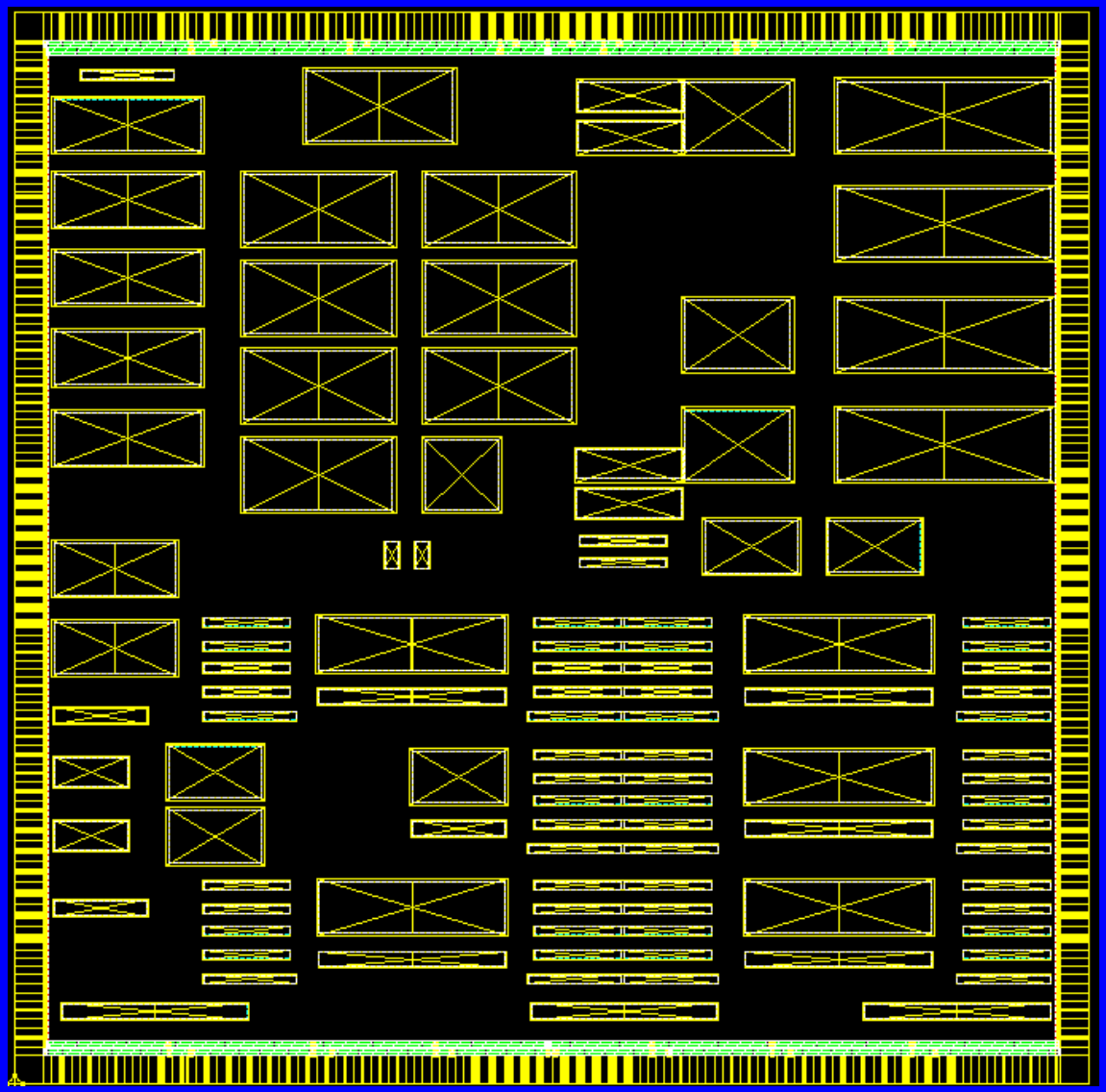
GR712RC: LEON3FT SoC

- Planned for 2008
- Dual Core, 150 MHz
- Multiple I/O ports
  - 6 SpW, 2 CAN, 1553, Ethernet, CCSDS TM/TC, SPI, I2C, 6 UART, ...
  - Selectable subset configurations
- Ceramic 256-pin QFP to support speed

Image Compression ASSP

- Standard JPEG2000
  - From Alma Tech (GR)
- 4 Mbit (150 cores), 500 Kgates, 30M transistors, 12×12mm, < 3W
- Uses 2 external SDRAMs (88MHz)
- Pre-validated on FPGA at full speed
- For imaging satellites
  - ASSP: 44 12-bit Mpix/s, 1 Tops
  - Many ASSPs in system
- Fab in 2008

JPIC Layout (mostly memories)



Summary

- RadSafe™
  - On commercial process, using standard EDA
  - Proven Rad-Hard-by-design
  - Proven quality
  - High performance, low power, low cost ASICs
- Example projects
  - FPGA conversions
  - LEON3FT-based dual-core SoC
  - JPEG2000 encoder