Radiation Effects Issues for SOI in Next Generation SRAM-based FPGAs

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Acknowledgements

Worked by the AFOSR MURI program

MURI

Authors would like to thank Kitt Reinhardt and Ron Schrimpf for their contributions to this research.

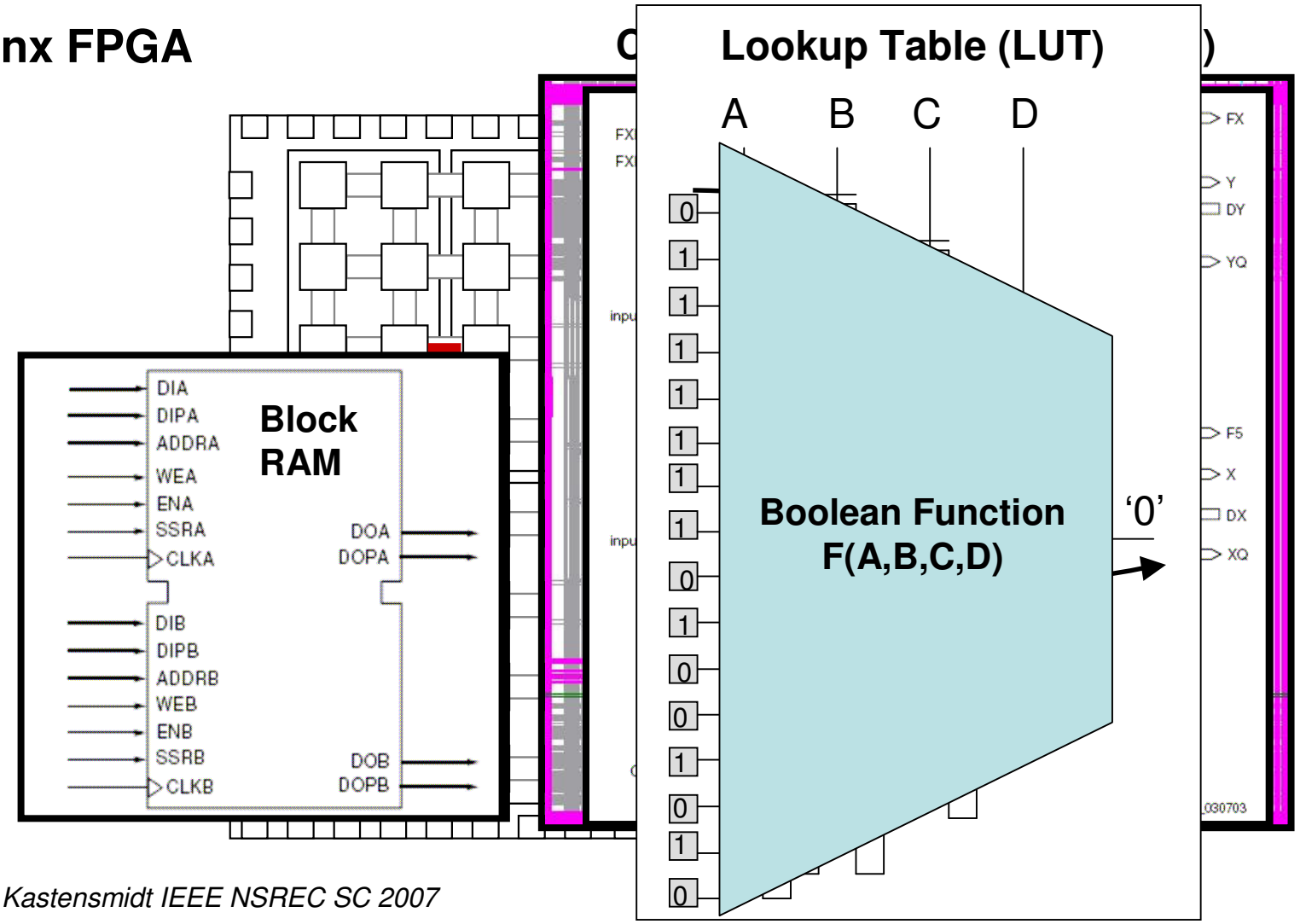
Presentation Topics

- SEE Effects in SRAM-based FPGAs
- TID Effects in SOI Technologies

Presentation Topics

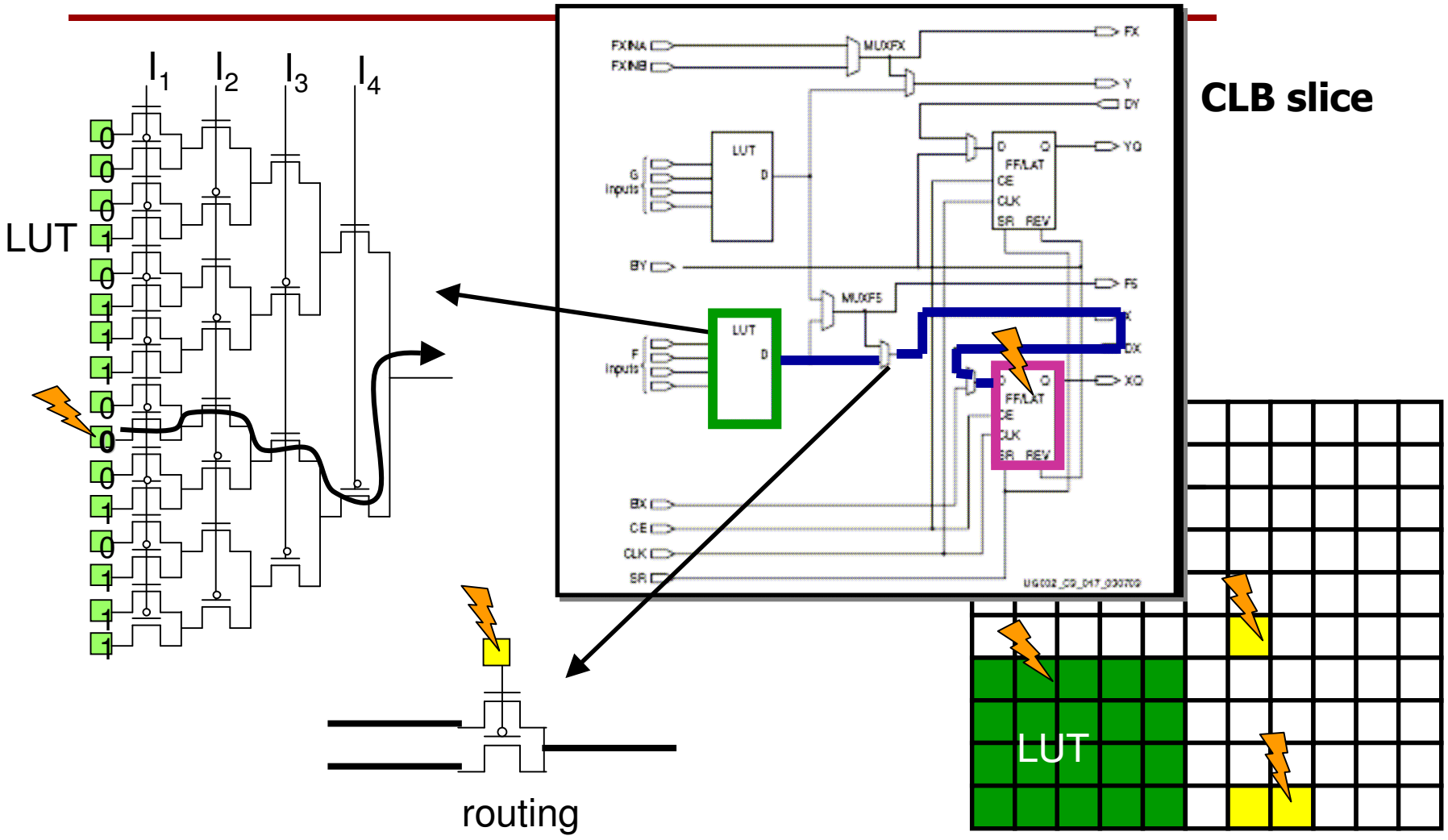
- **SEE Effects in SRAM-based FPGAs**
- **TID Effects in SOI Technologies**

SRAM-based FPGA Architecture



after Kastensmidt IEEE NSREC SC 2007

SEU in SRAM-based FPGAs: CLB slice



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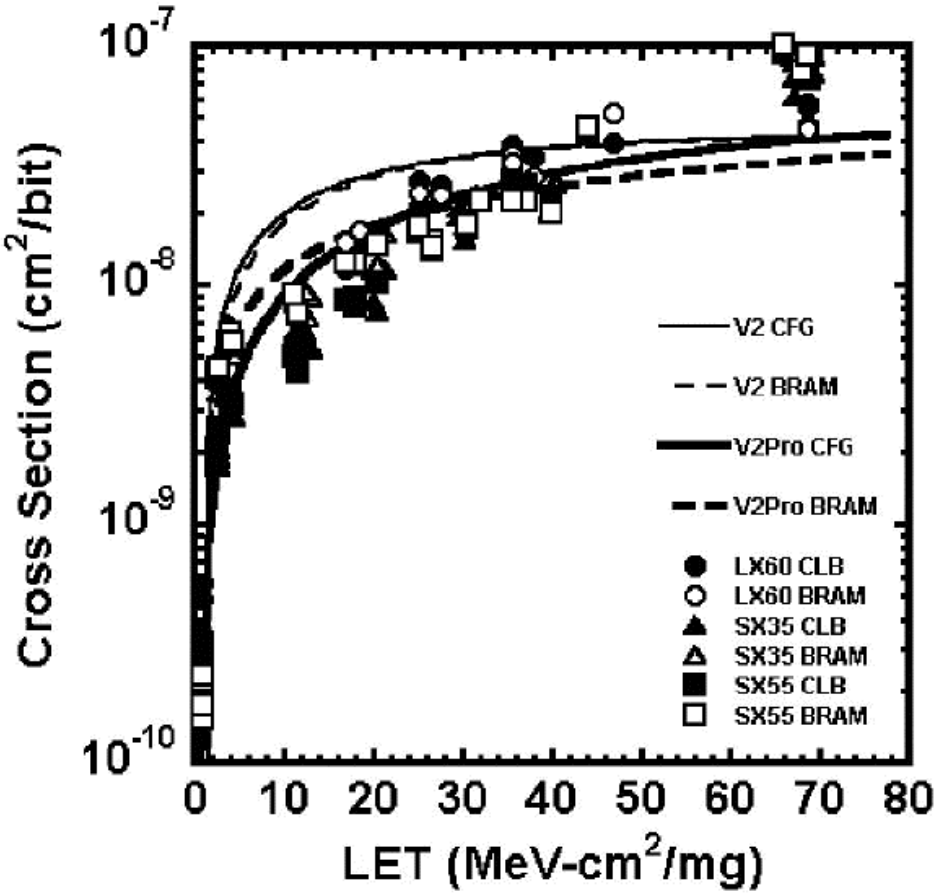
SEE Characterization – Heavy Ion:
Static Testing in Virtex4



- **Sensitivity in Virtex4 similar to Virtex-II**
- **Increase at high LET believed to come from MBUs**
- **Block RAM more susceptible than CLB**

after George, et al. IEEE Radiation Effects Data Workshop, 2006

SEE Characterization – Heavy Ion:
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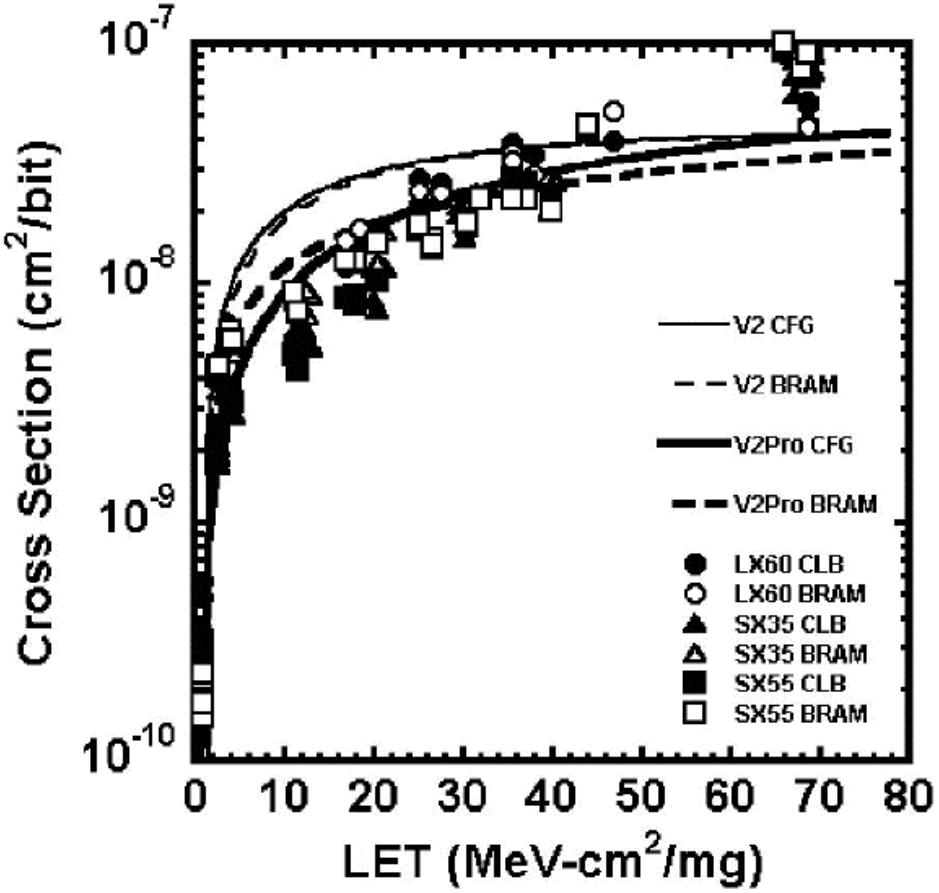


- **Sensitivity in Virtex4 similar to Virtex-II**
- **Increase at high LET believed to come from MBUs**
- **Block RAM more susceptible than CLB**

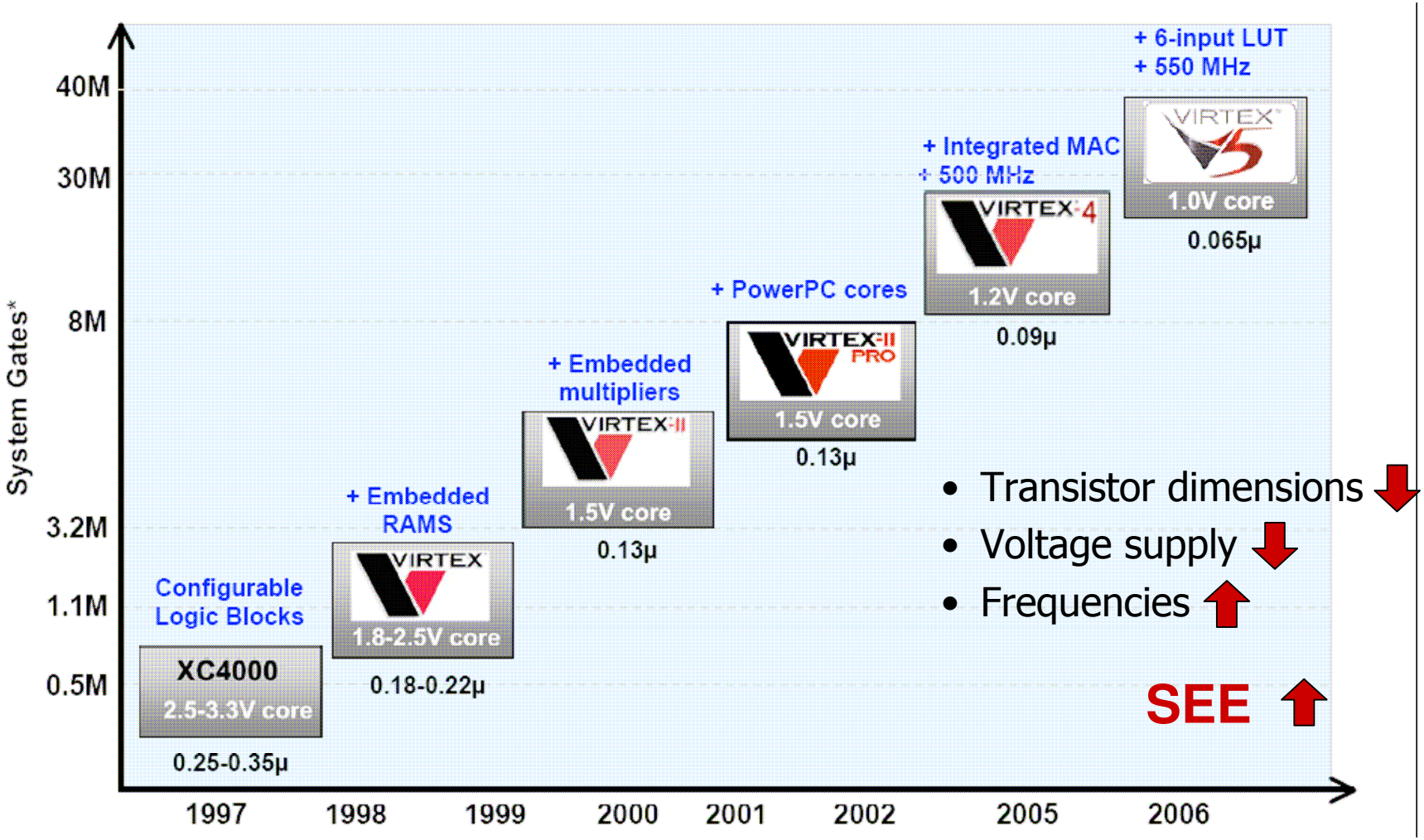
Possible Explanation

Transistors in BRAM are thin oxide 90 nm devices

Transistors in CLB are thick oxide 100 nm devices with longer channels

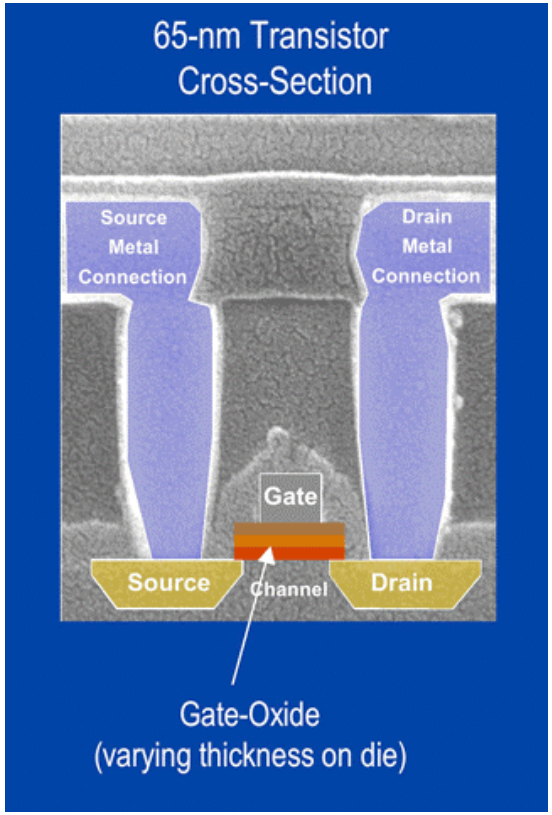
after George, et al. IEEE Radiation Effects Data Workshop, 2006

Technology Scaling in Xilinx FPGAs



after Kastensmidt IEEE NSREC SC 2007

65 nm bulk triple oxide process



- **65-nm XC5VLX50 Virtex™-5 FPGA manufactured by Toshiba and UMC**
- **35% lower dynamic power achieved with lower supply voltage and capacitance, hard IP**
- **Same low static power with introduction on 3rd medium thickness oxide**

Xilinx WP246 (v1.2) February 1, 2007
http://www.xilinx.com/prs_rls/2006/xil_corp/06128xlnx_chipworks.htm
http://www.dsp-fpga.com/articles/holmberg/

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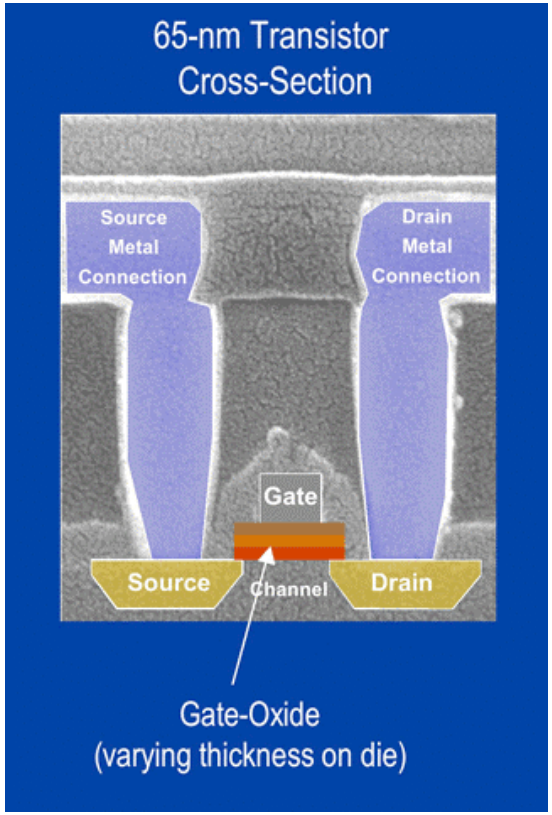

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SEE susceptibility remains a major concern due to reduced dimensions and supply voltage, increased frequency, and increasing threat of MBUs in bulk technology

Xilinx WP246 (v1.2) February 1, 2007
http://www.xilinx.com/prs_rls/2006/xil_corp/06128xlnx_chipworks.htm
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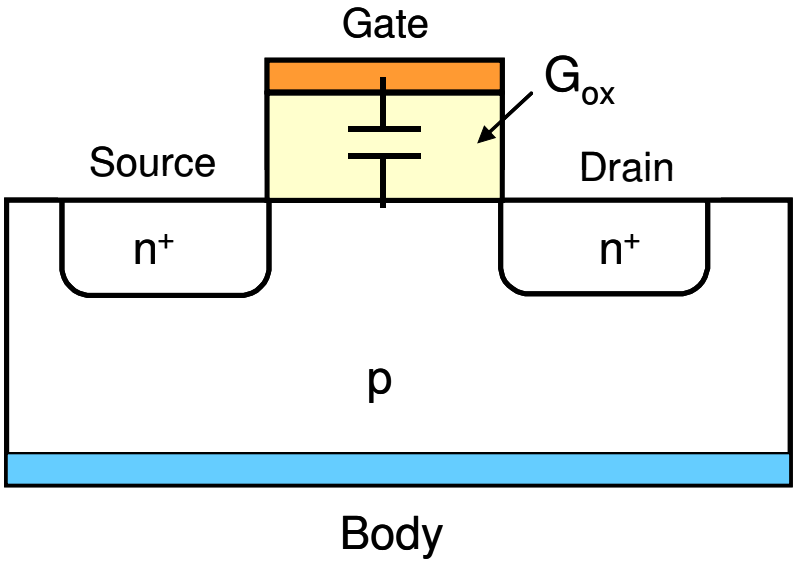
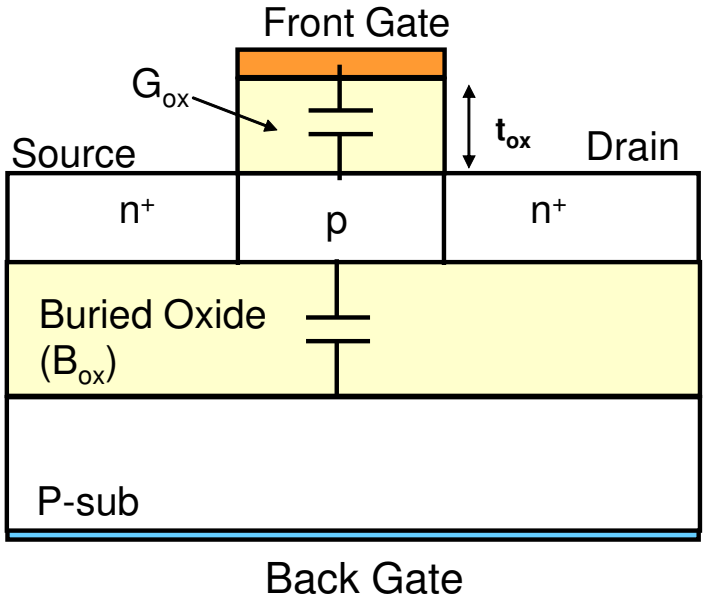
Bulk vs. SOI: Structure

Bulk



Drain and source regions diffused into a deep body (well or substrate) region

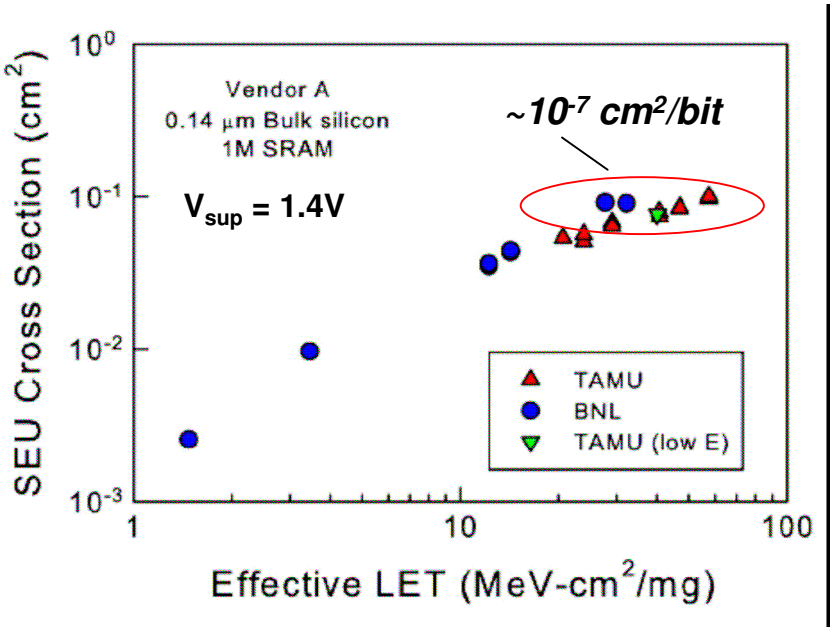
Planar SOI



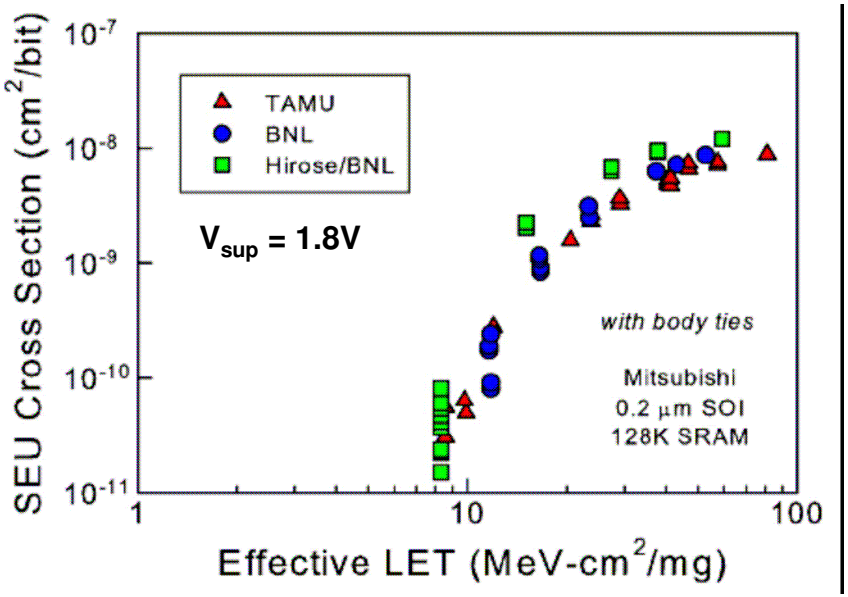
Drain, source and body formed in thin silicon film between two dielectrics (G_{ox} and B_{ox}), with or without body tie

Bulk vs. SOI: SRAM SEU response

Bulk



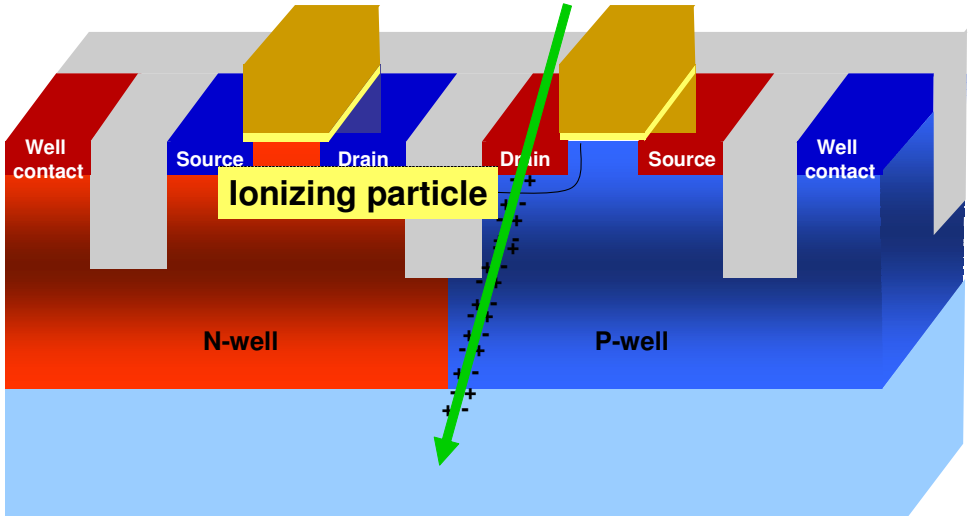
Planar SOI



While the bulk technology is slightly smaller, the significantly higher threshold LET and lower cross-section for the SOI parts indicates superior SEE tolerance in SOI technologies.

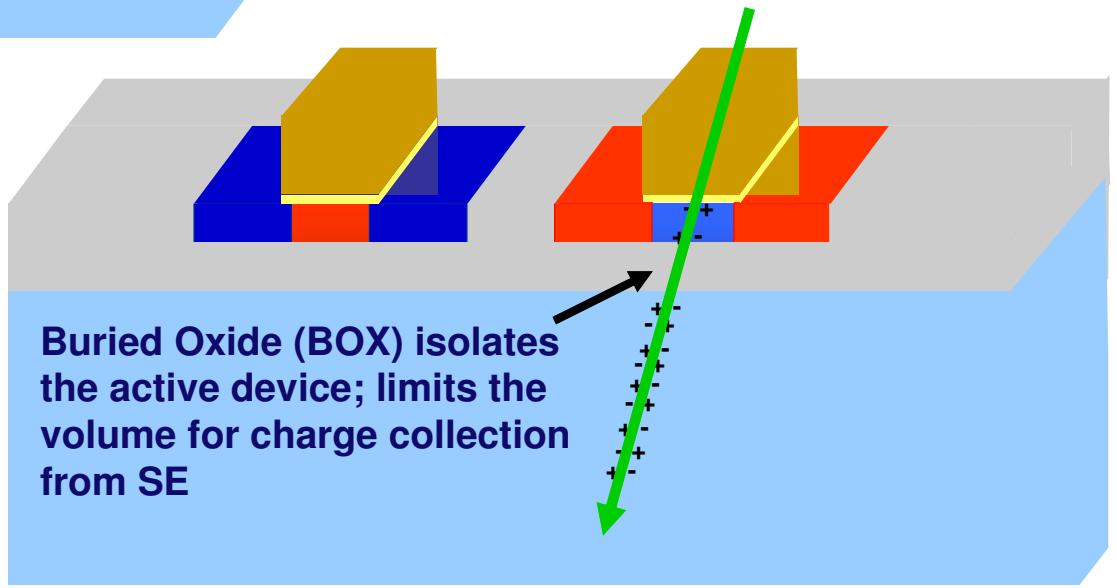
after Dodd et al., IEEE TNS Aug. 2007

Advantage of SOI for SEE



Bulk

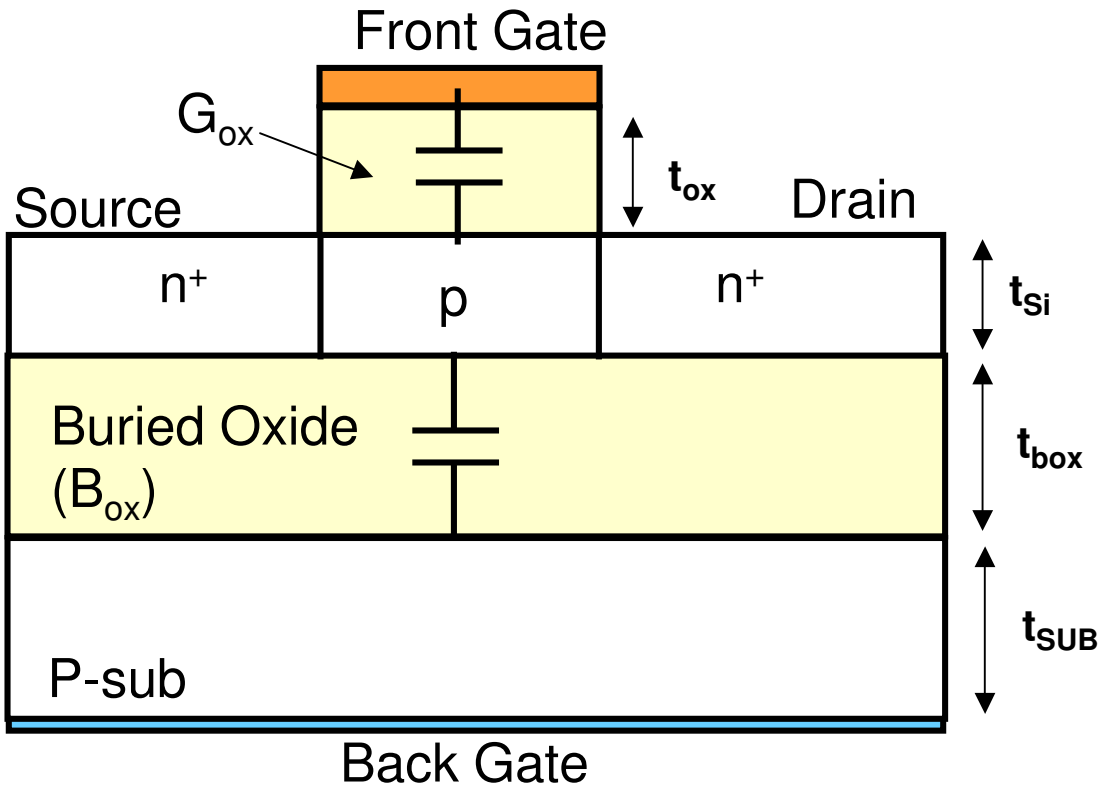
SOI



Presentation Topics

- SEE Effects in SRAM-based FPGAs
- **TID Effects in SOI Technologies**

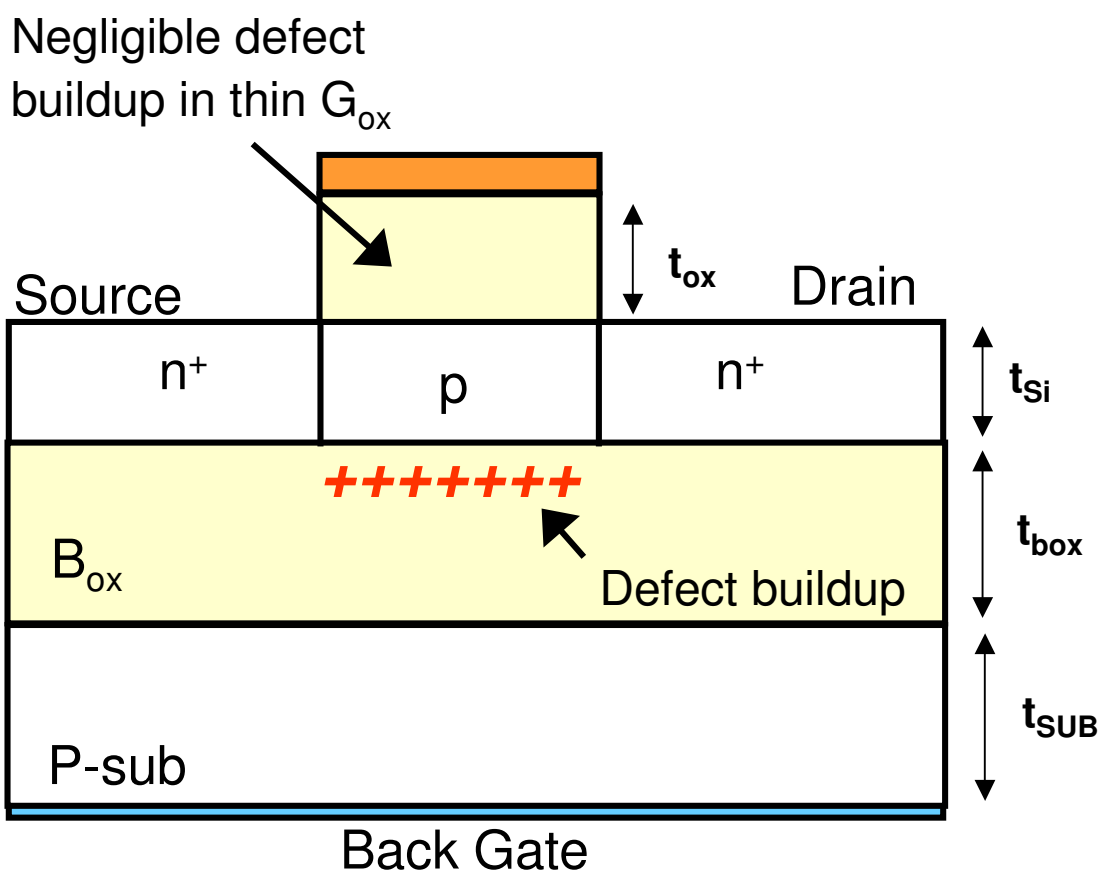
Silicon on Insulator (SOI) Transistor



Key Advantages:

- **Reduced junction capacitance**
- **V_T control via dual gate operation**

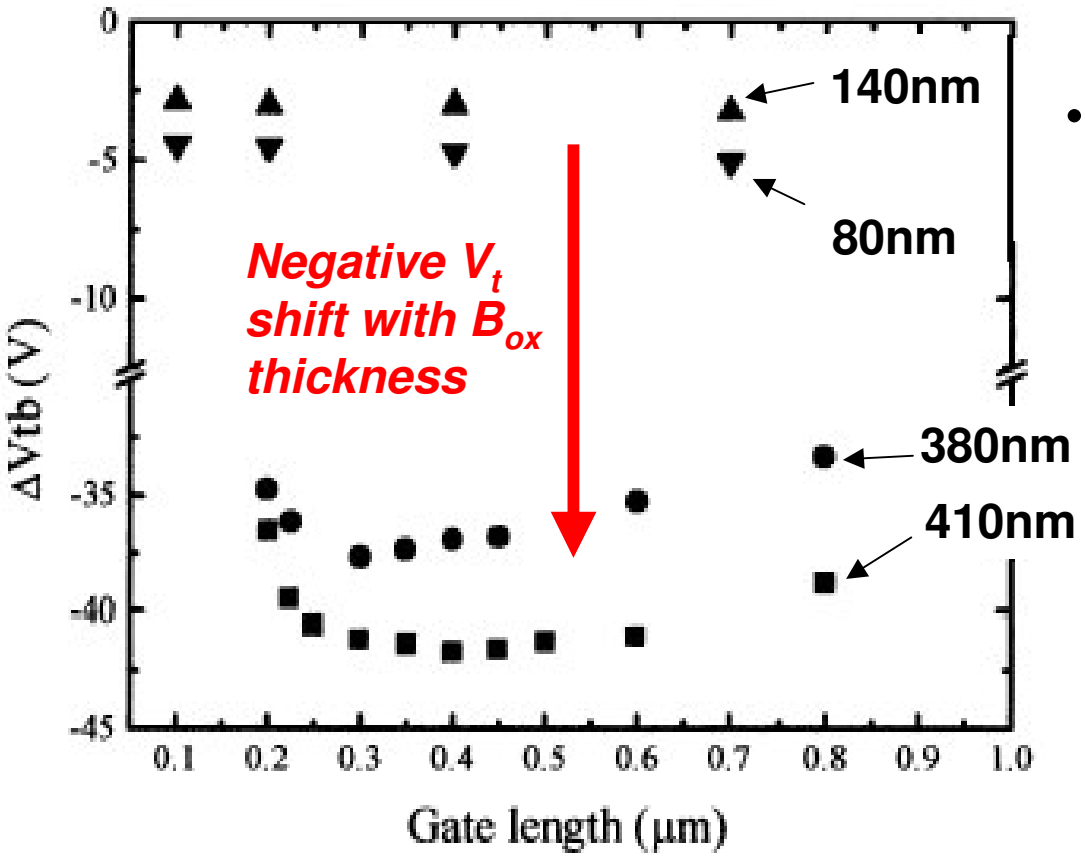
TID Effects in SOI



- **Much of SOI TID susceptibility due to defect buildup in thick B_{ox}**

t_{ox} < 5 nm
t_{box} > 80 nm

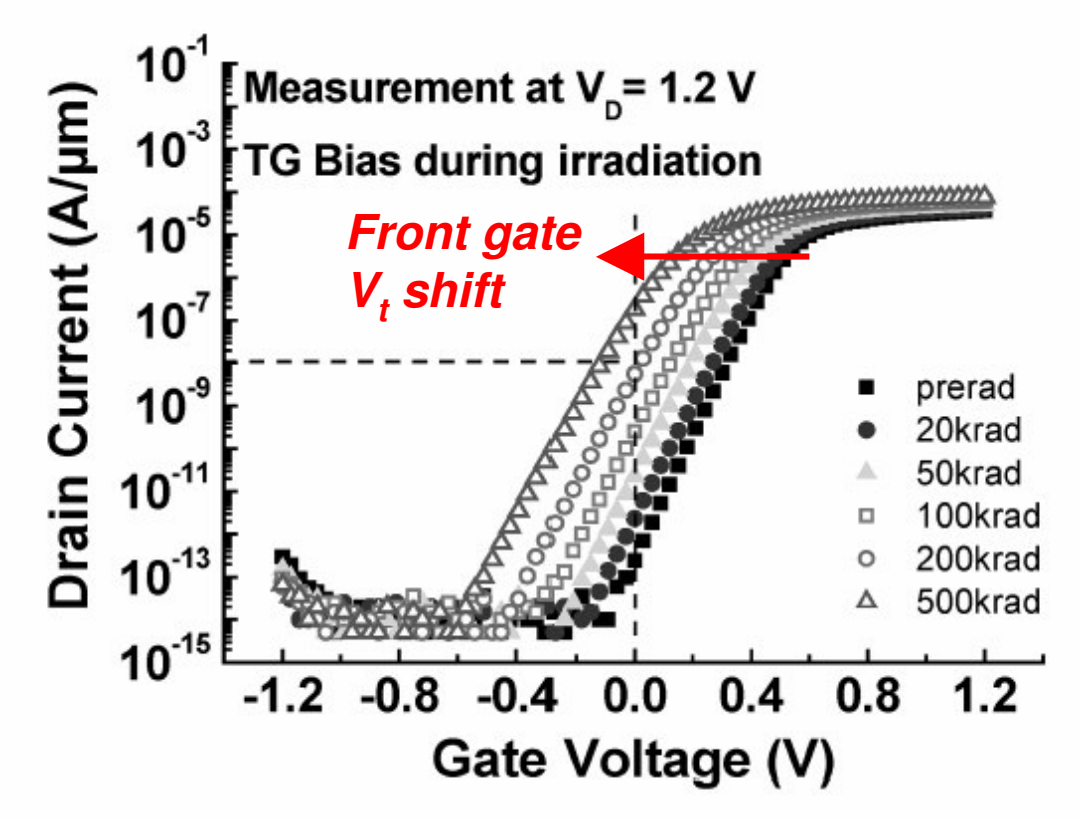
TID Effects in SOI



after Flament et al., IEEE TNS 2003

- **Radiation damage to B_{ox} can cause**
  1. **Reduced frontgate V_t caused by gate coupling**
  2. **"Latch effect" due to non-uniform charge build-up and impact ionization**
  3. **GIDL enhanced back-channel leakage**

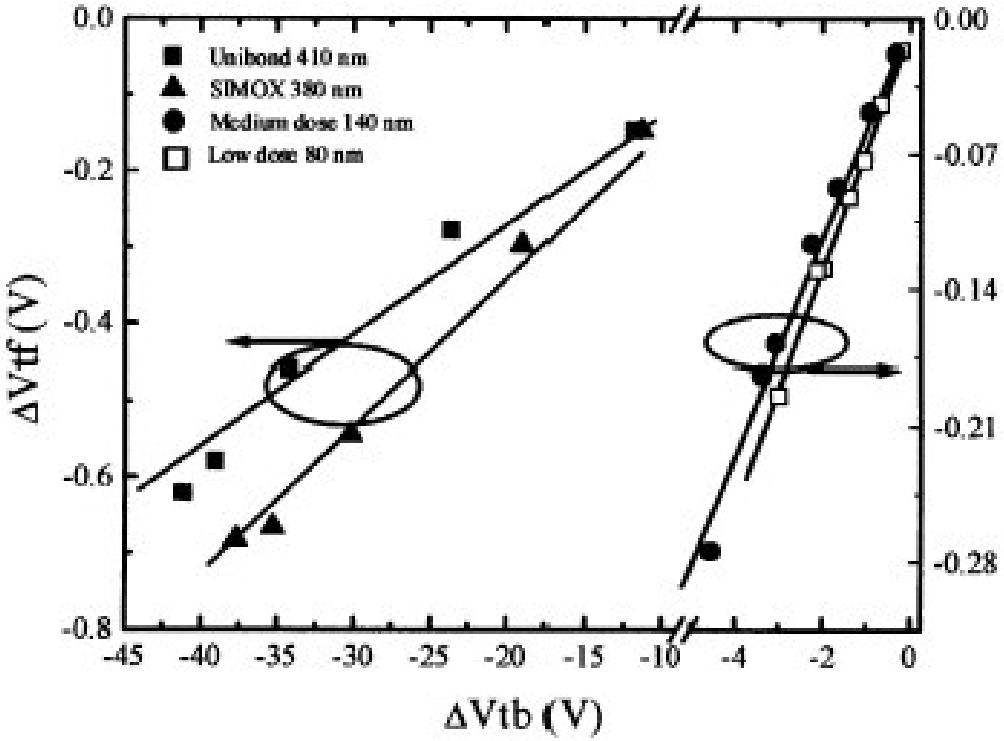
Coupling Effect (Data)



after Paillet et al., IEEE TNS 2005

- **Fully depleted SOI devices *<u>with body contact</u>* can exhibit front-gate threshold voltage shift due to electrostatic coupling from back gate**

Coupling Effect (Model)



after Flament et al., IEEE TNS 2003

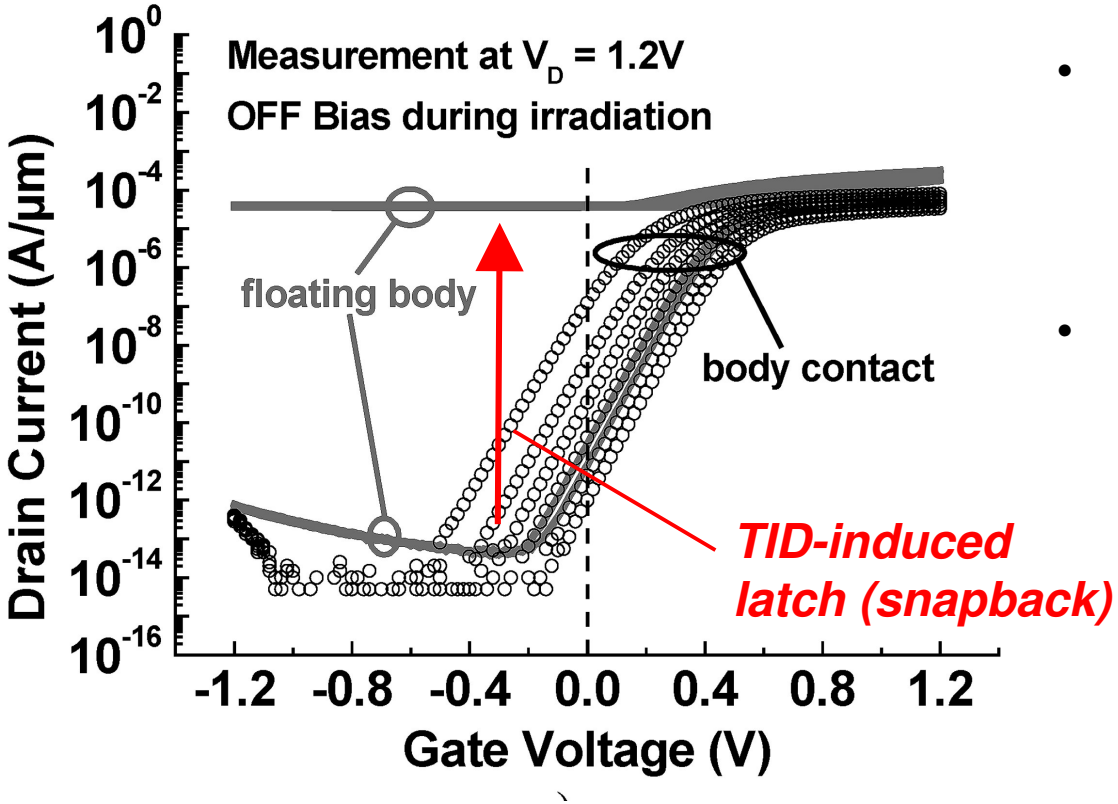
- **Charge buildup in the B_{ox} shifts the back gate V_t and the front gate V_t via the coupling coefficient (k)**

$$k = \frac{\Delta V_{Tf}}{\Delta V_{Tb}} \approx \frac{t_{ox}}{t_{box}}$$

tradeoff

The thinner the B_{OX}, the less defect buildup but greater coupling

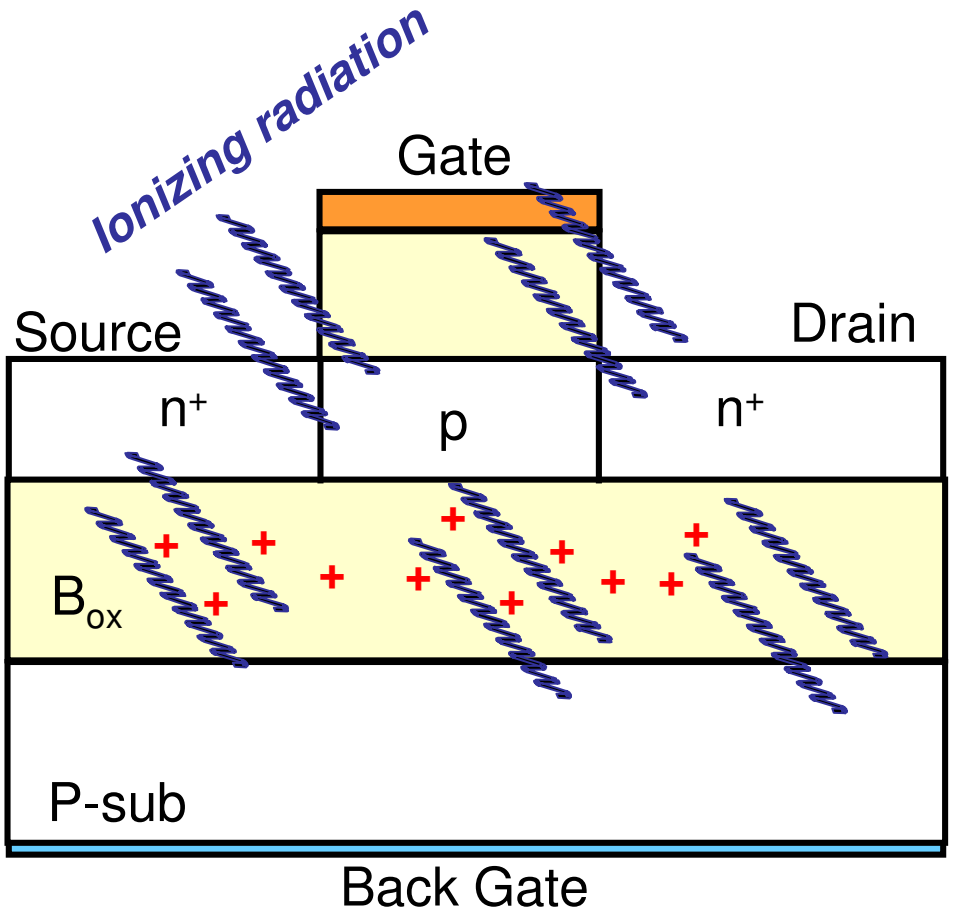
Total Dose Latch



after Paillet et al., IEEE TNS 2005
after Schwank et al., IEEE TNS 2003

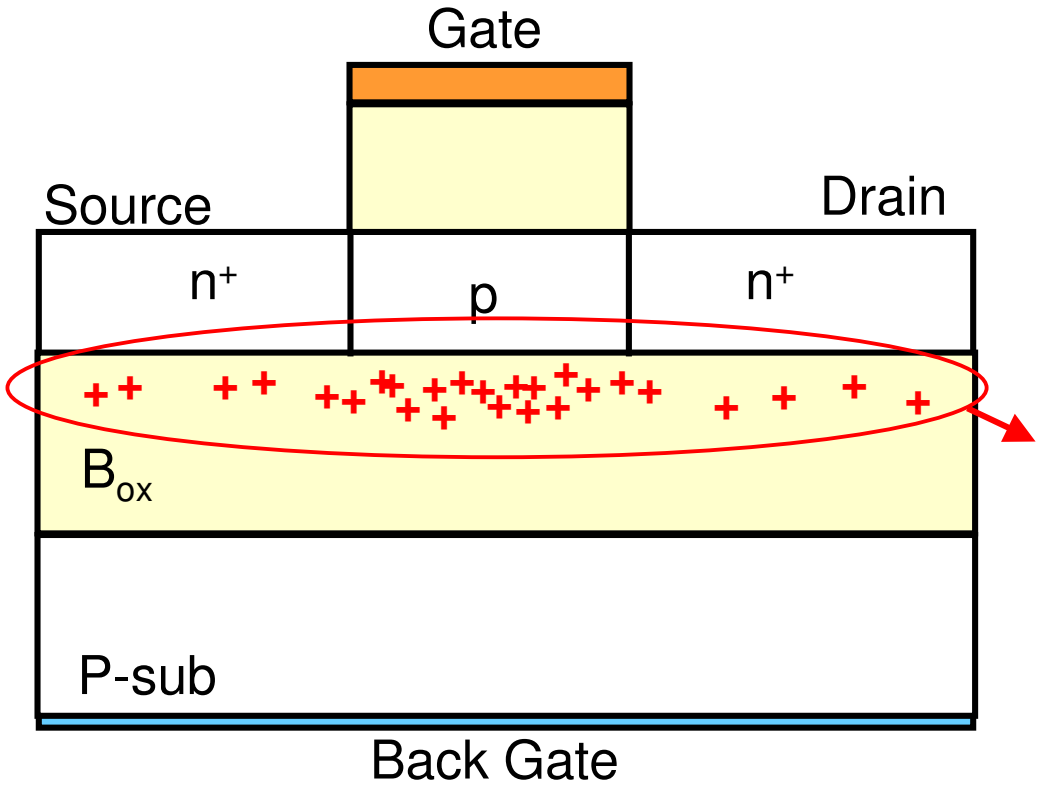
- **Without body contact, drain current can "jump" to a high current regime for negative gate voltages**
- **In some SOI technologies this effect seems to be caused by a single transistor latch effect**

Latch Mechanism



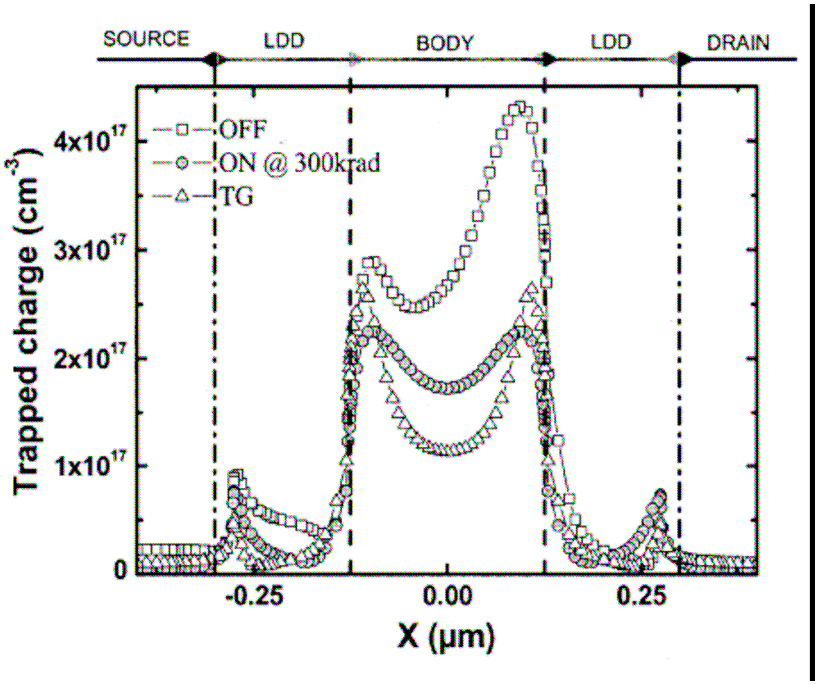
- **Ionizing radiation generates charge in the thick buried oxide**

Latch Mechanism

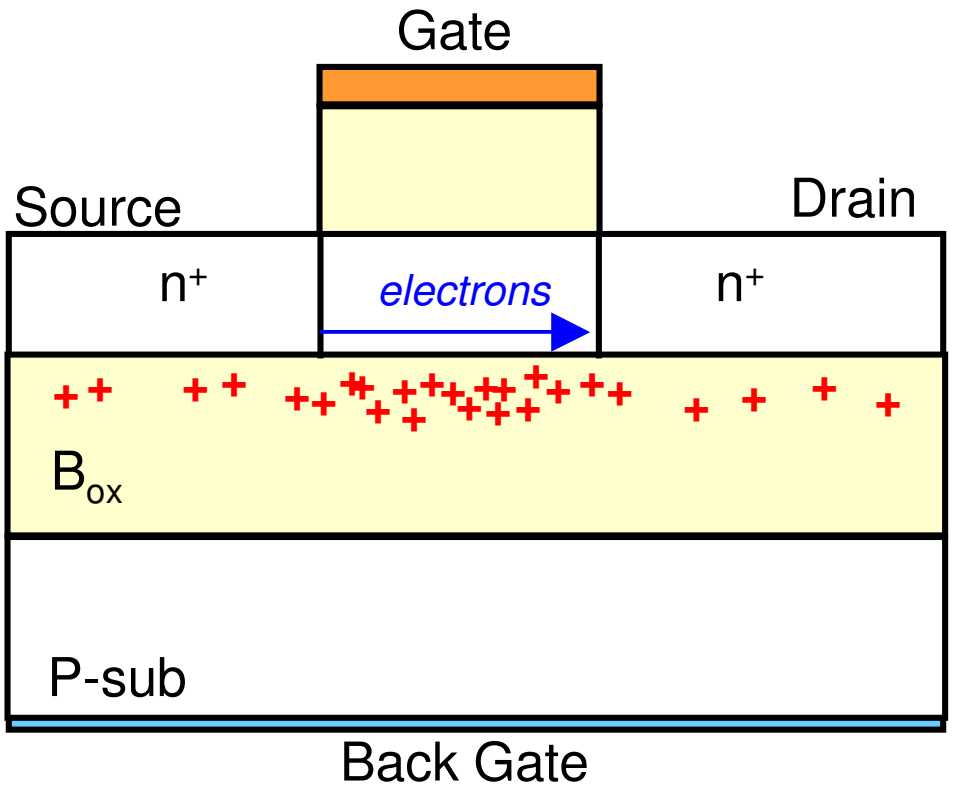


after Flament et al., IEEE TNS 2003

- **Charge is trapped charge primarily near the Box-body interface**



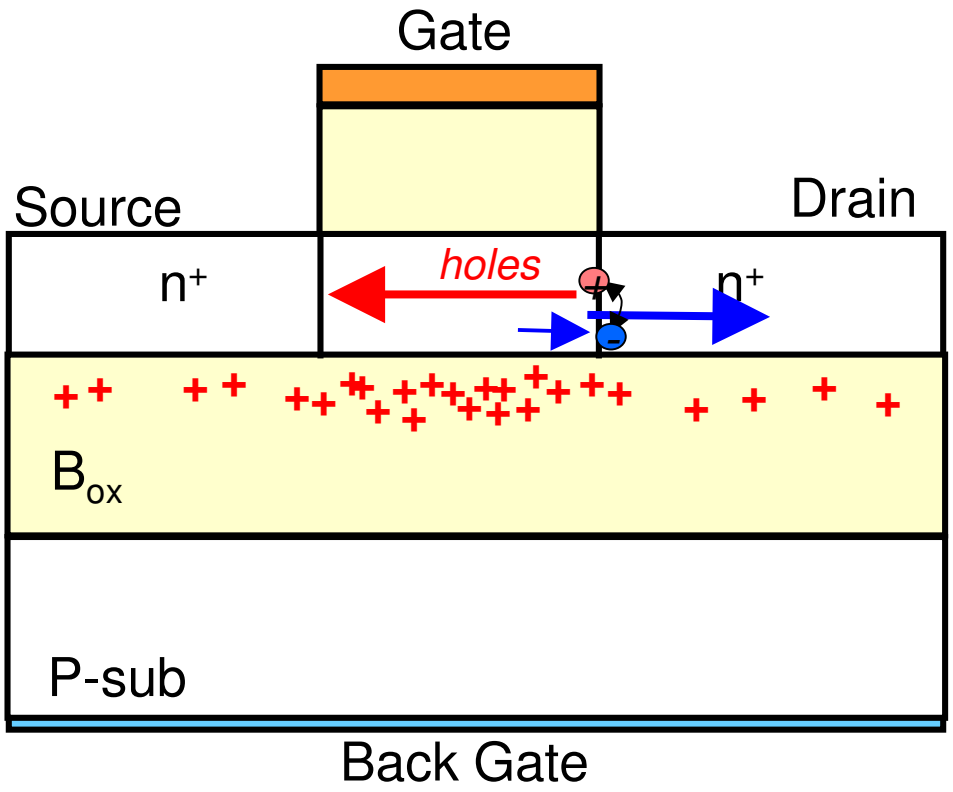
Latch Mechanism



after Schwank et al., IEEE TNS 2003

- **Charge below body lowers body to source barrier height, inducing electron flow across the body**

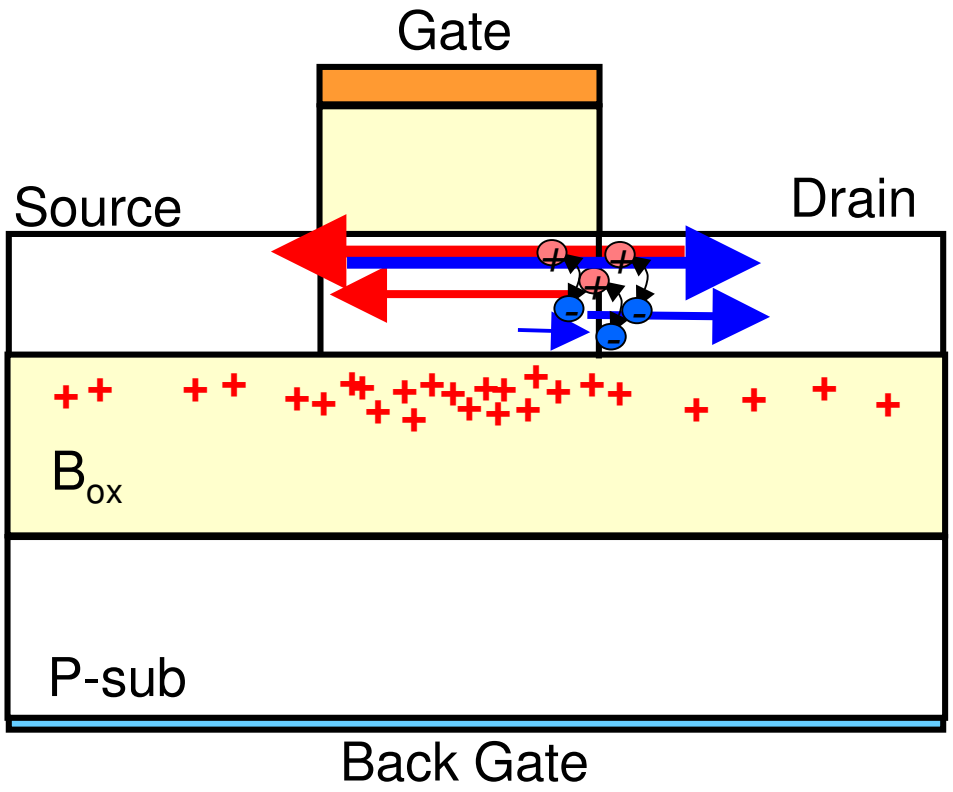
Latch Mechanism



after Schwank et al., IEEE TNS 2003

- **Charge below body lowers body to source barrier height, inducing electron flow across the body**
- **Electrons entering high field drain body region generate additional carriers via *impact ionization***

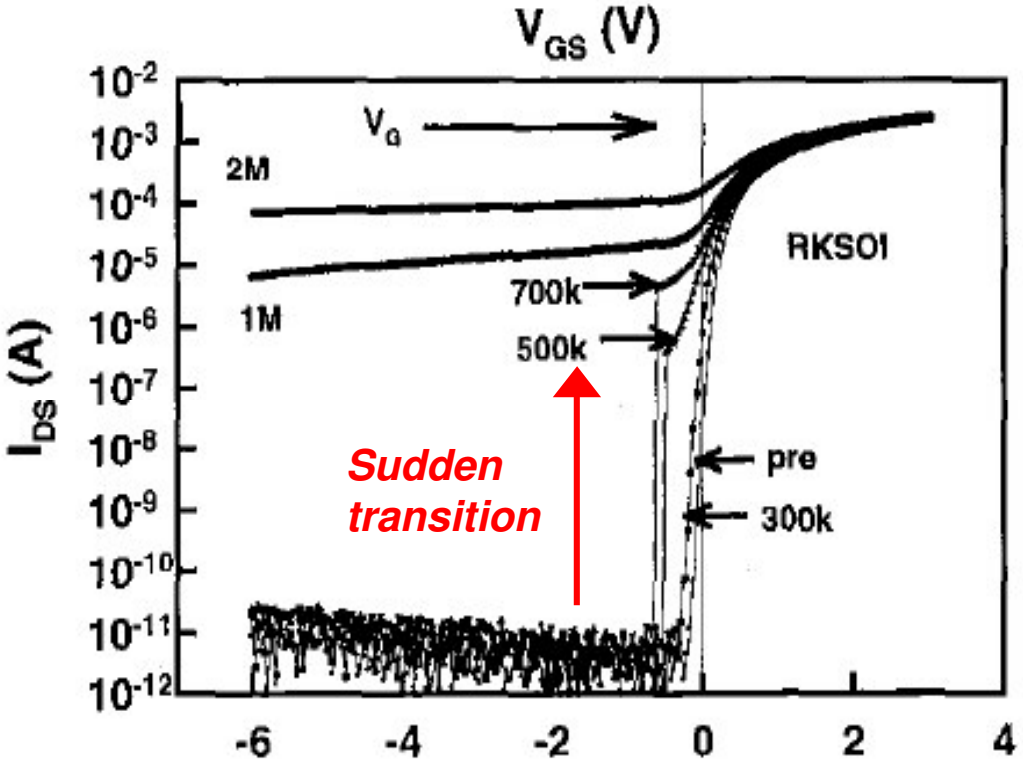
Latch Mechanism



after Schwank et al., IEEE TNS 2003

- **Charge below body lowers body to source barrier height, inducing electron flow across the body**
- **Electrons entering high field drain body region generate additional carriers via *impact ionization***
- **Back-injected holes induce a self sustaining single transistor latch condition and high current regime**

Latch Mechanism

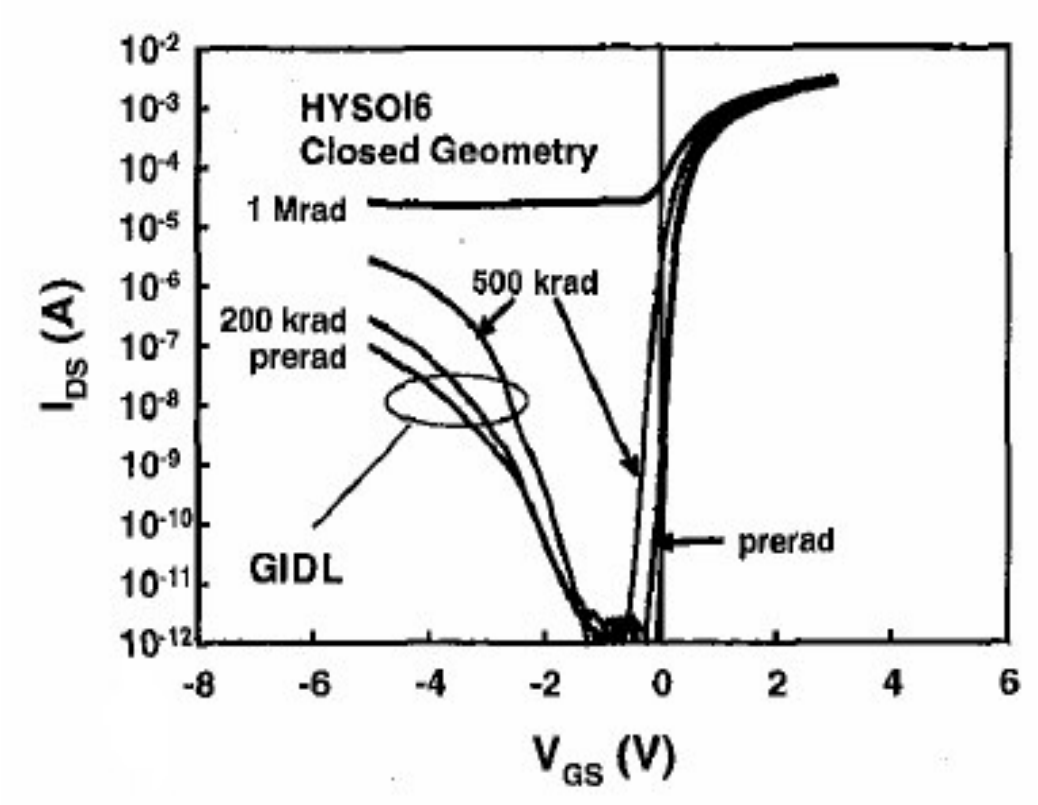


after Schwank et al., IEEE TNS 2000

- **For some SOI technologies, "latch effect" is evidenced by sudden transitions in response characteristics**
- **Effect is most likely observed at high drain biases and devices with high drain doping**

Not all SOI technologies exhibit latch type behavior

GIDL Enhanced Back-Channel Leakage

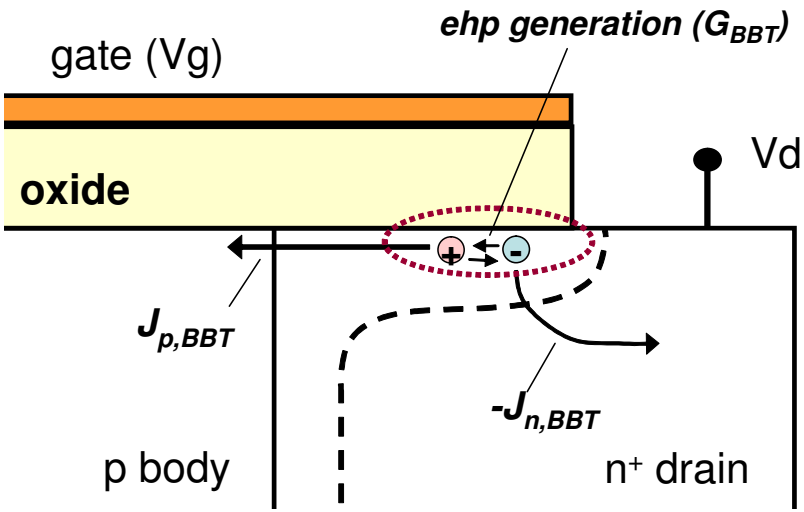


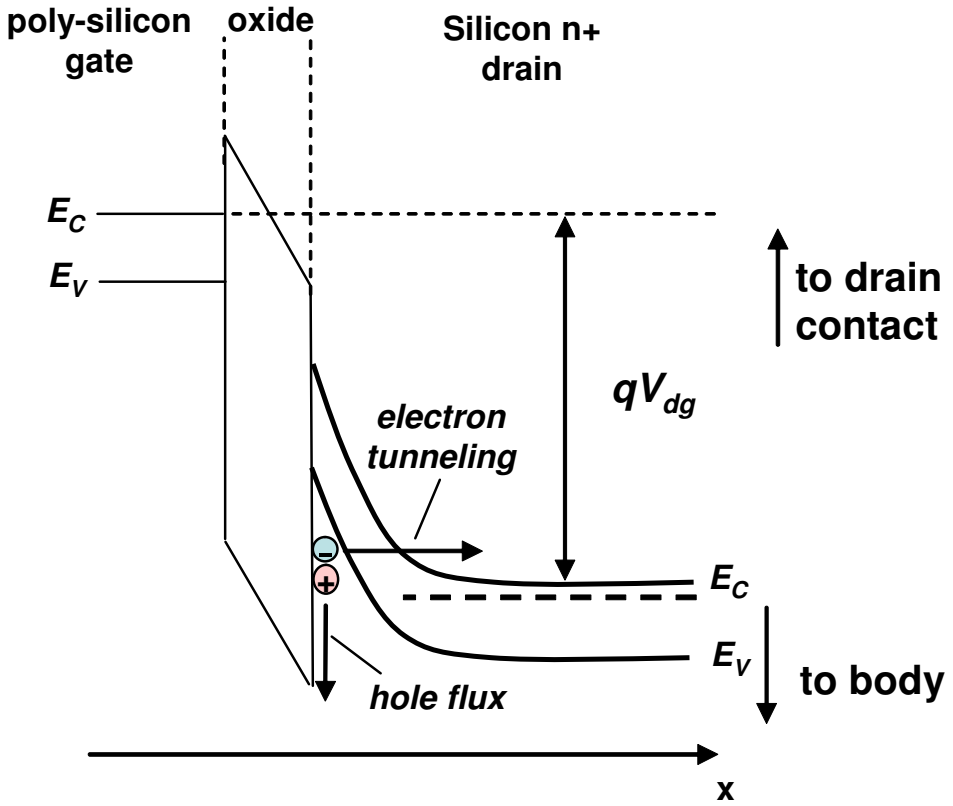
after Schwank et al., IEEE TNS 2000

- **High current at high total dose**
- **No sudden transitions**
- **Drain current increase with negative gate bias via gate induced drain leakage (GIDL) enhancement**

Mechanism for GIDL: band-to-band tunneling (BBT)

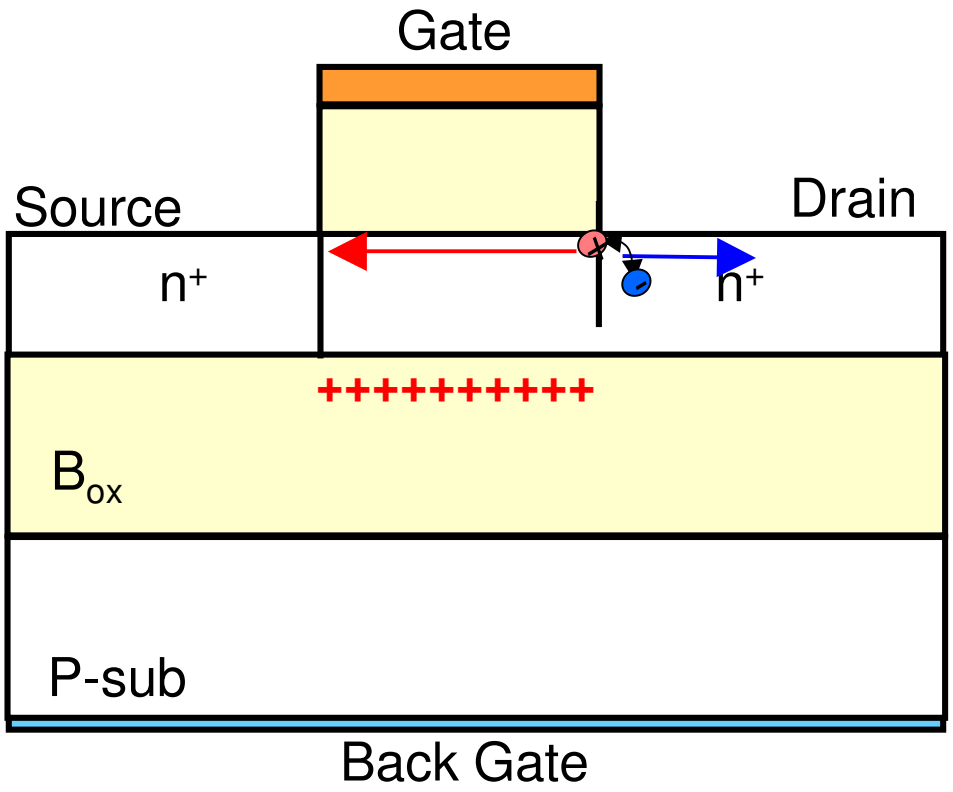
- **Local band-bending in high field drain-body region generates free carriers via electron tunneling**





After J-H Chen, IEEE TED 2001

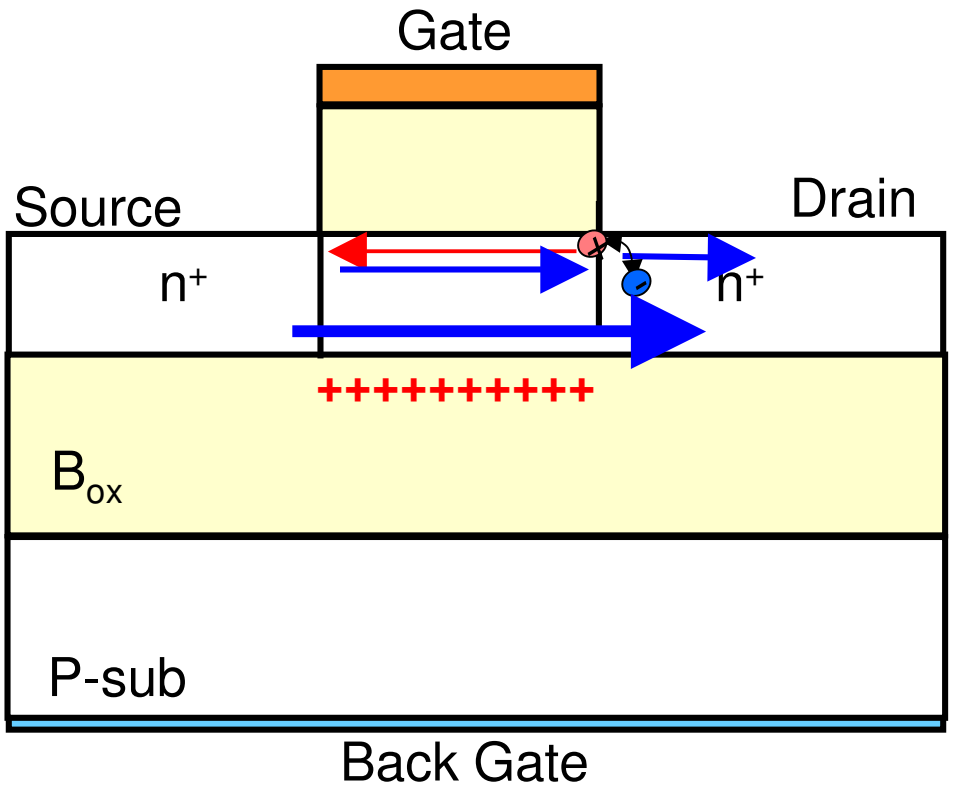
GIDL Enhancement Mechanism



after Adell et al., IEEE NSREC 2007

- **Holes generated by BBT transport to source, forward biasing the source-body junction**

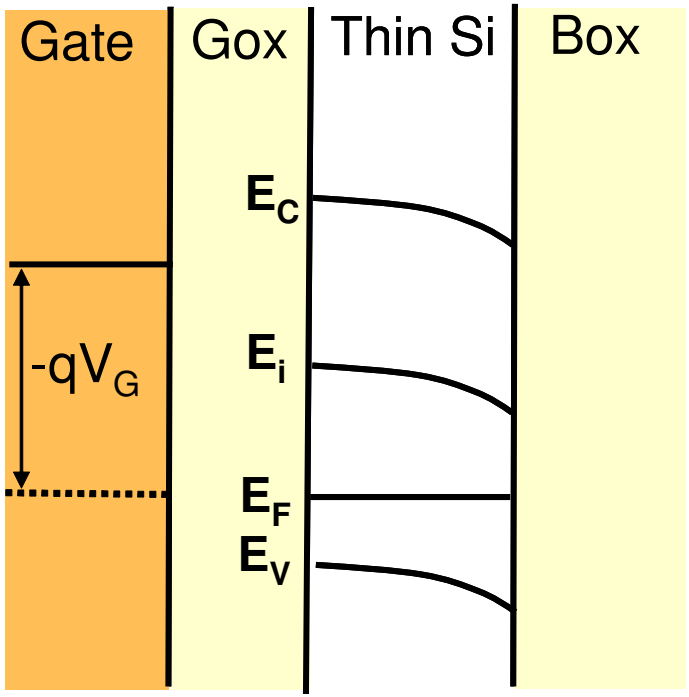
GIDL Enhancement Mechanism



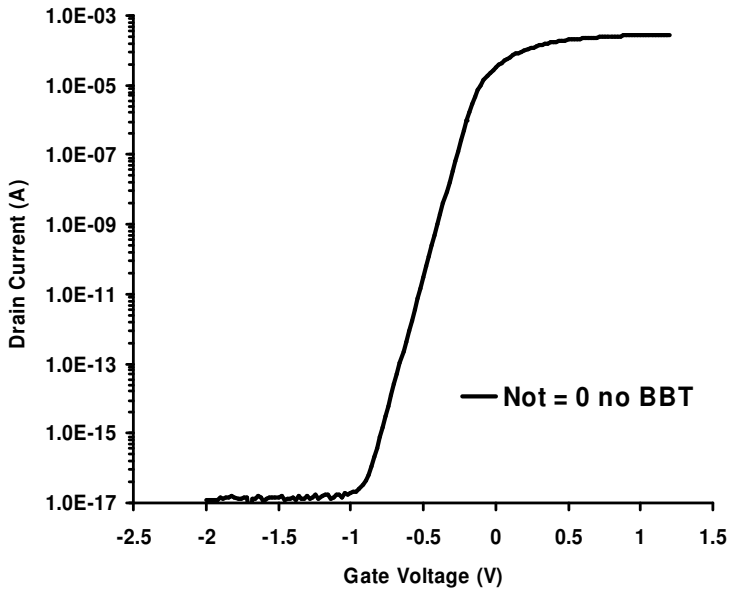
after Adell et al., IEEE NSREC 2007

- **Holes generated by BBT transport to source, forward biasing the source-body junction**
- **Electrons back-injected into body increase electron concentration along back gate, enhancing back channel leakage**

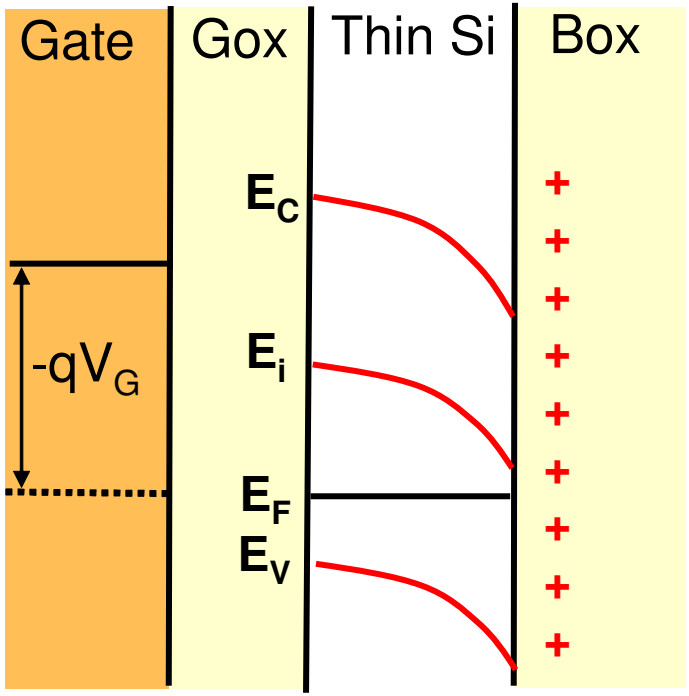
GIDL Enhancement Mechanism: Band Effects



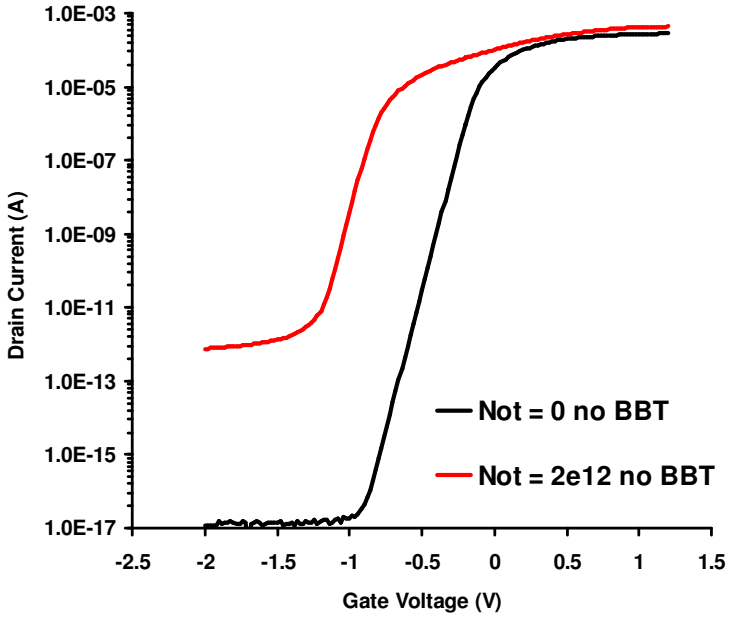
- **Prior to radiation exposure and without BBT, back side interface is weakly depleted**



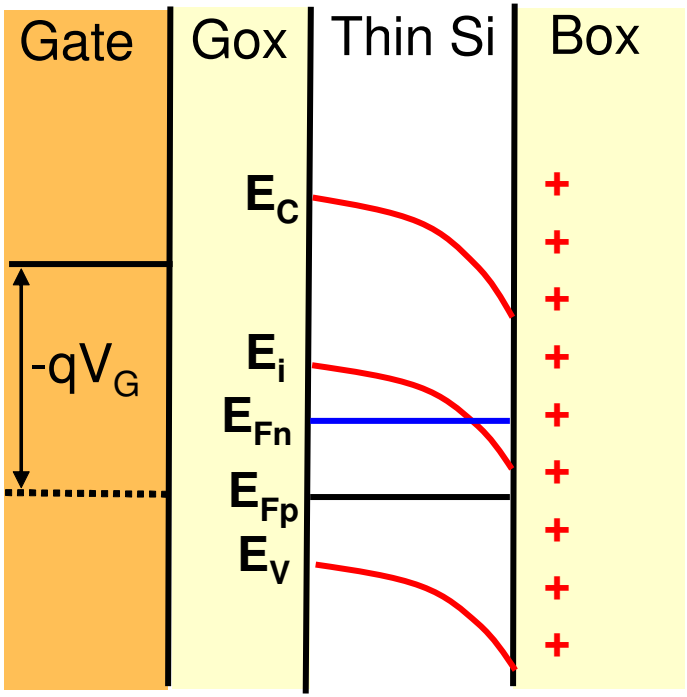
GIDL Enhancement Mechanism: Band Effects



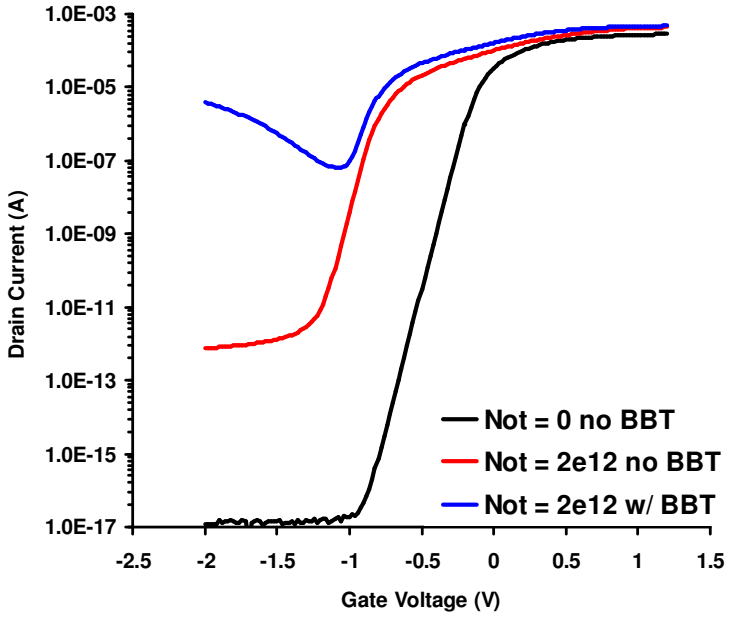
- **Trapped charge increases back-side surface potential, back channel concentration and current**



GIDL Enhancement Mechanism: Band Effects



- **GIDL current increases electron Fermi level further raising back channel density and current**



TID Effects in SOI Technologies:
The BAD News

- Charge buildup in the buried oxide continues to be a significant total ionizing dose threat in SOI technologies
- The threats include:
  - Front gate threshold voltage reduction due to electrostatic coupling form the back gate.
  - Drain-to-source leakage caused by back-side inversion enhanced by impact ionization (latch) and/or GIDL
- Traditional radiation-hardening-by-design techniques do not address the effects caused by damage to the B_{ox}

TID Effects in SOI Technologies:
The GOOD News

- Commercial manufacturers typically increase doping along the back channel to reduce static power in CMOS circuits. This may mitigate the impact of charge buildup in the B_{ox}
- The use of body ties not only improves SEE effects in SOI parts but there is strong evidence that they also suppress latching and GIDL enhancement
- Some commercial manufacturers reduced body lifetime thereby reducing diffusion lengths, which suppresses bipolar action, a principle mechanism in latching and GIDL enhancement