Military and Aerospace FPGA and Application Meeting

Nov. 27 – 29, 2007
Palm Beach, FL

Intermittency Detection and Mitigation in FPGAs

James P. Hofmeister
Ridgetop Group, Inc.

Innovative Detector:

Faults in Solder-Joint Pins of Fully Programmed and Operational Field Programmable Gate Arrays (FPGAs)

SJ BIST™

Verilog softcore in FPGA

SJ Monitor™

IC Chip on Same Board as FPGA

(Patents pending)

Topics:

1. State of the Art: packaging, mounting and soldering, cracks and fractures, intermittency, high stress areas, I/O ports

2. SJ BIST: description, cap-R-freq, test results, HALT experiments, demonstration box

3. SJ Monitor: description, signals, tests: temperature, voltage, power, detectable fault resistance

4. SJ BIST deliverables

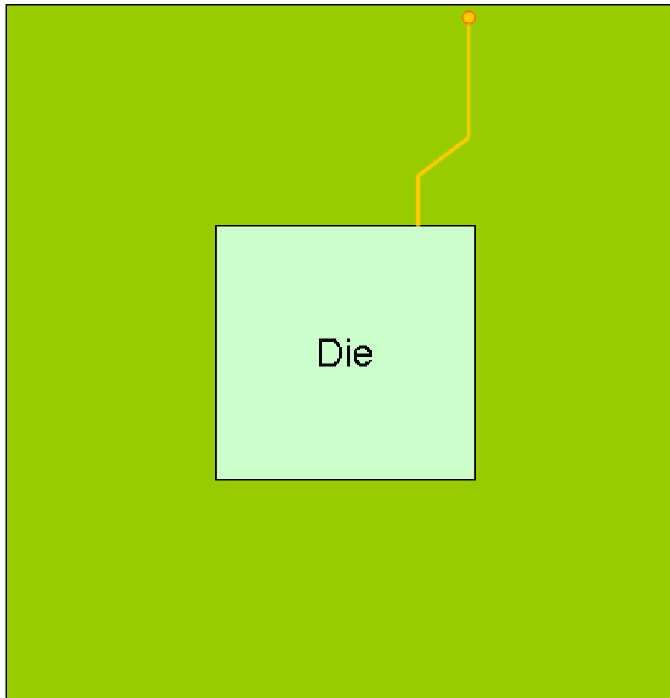
5. SJ Monitor status

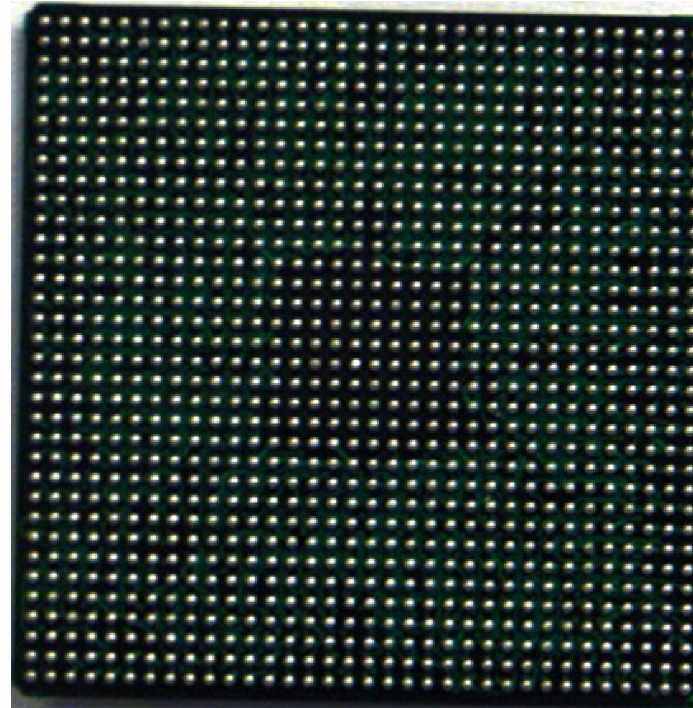
State of the Art: Packaging

- Problematic visual, optical, x-ray ... inspection techniques
  - small pitch, small ball sizes

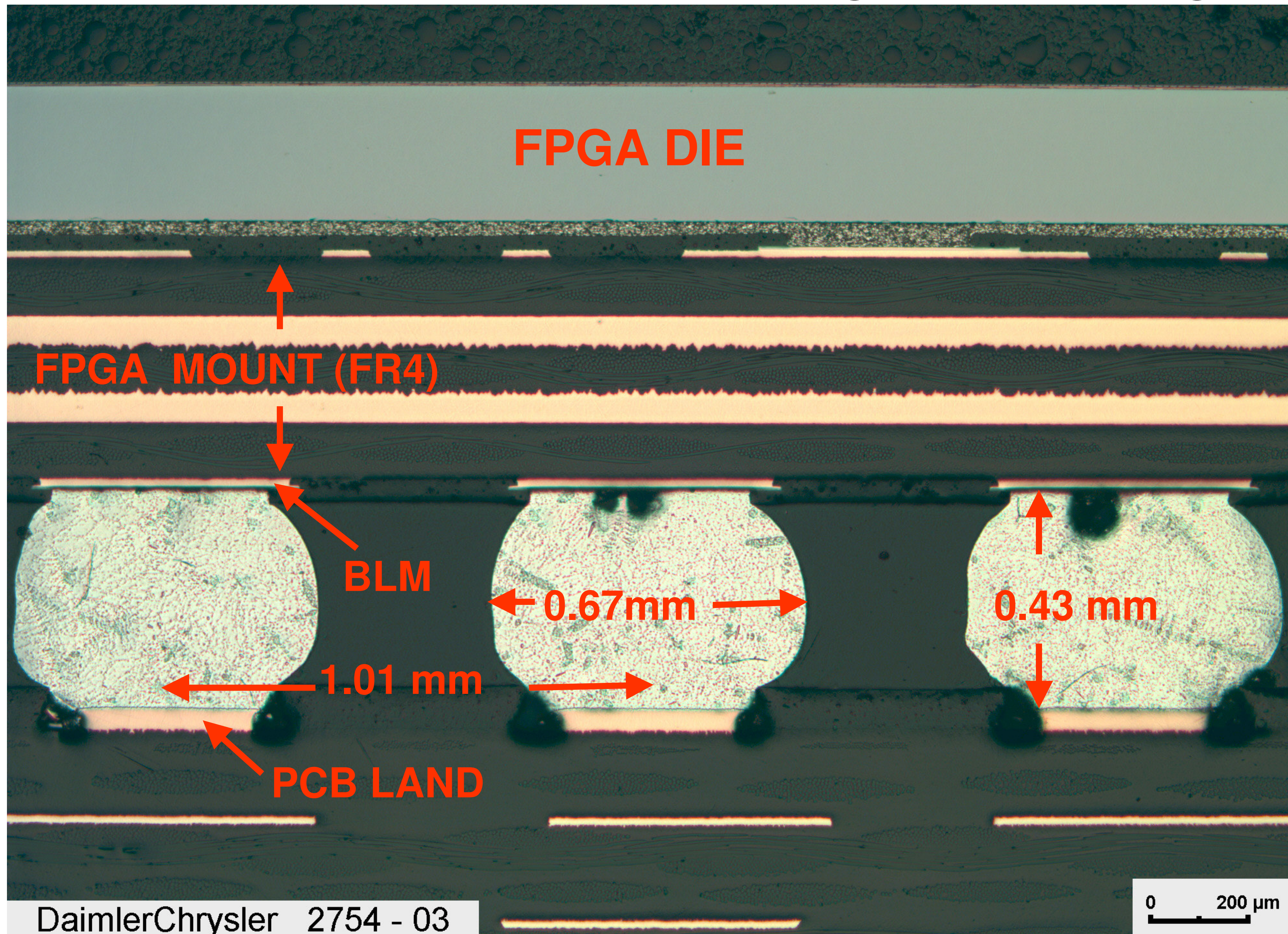
XILINX® FG1156
Die on mounting base

34x34 array of pins
35mm square – bottom of the base (package)





State of the Art: BGA Mounting and Soldering

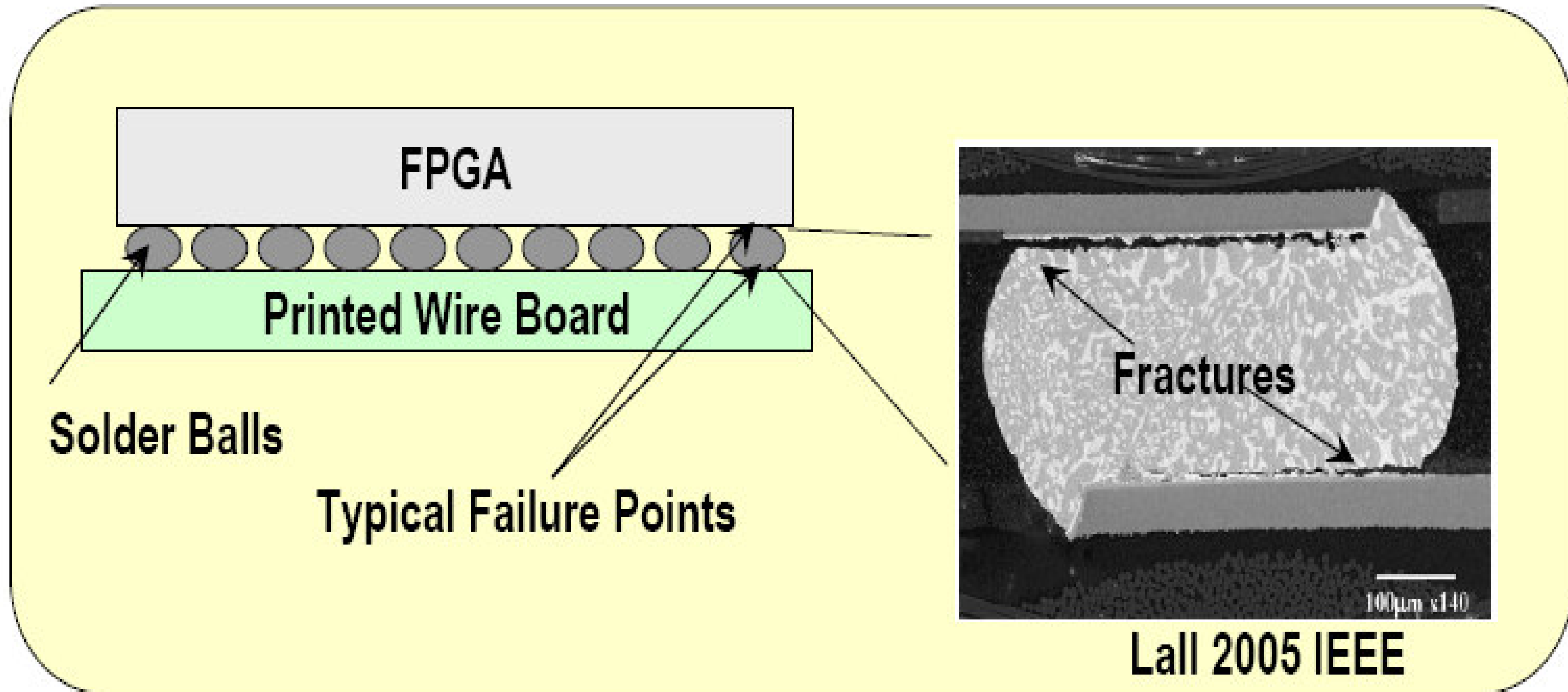


www.Ridgetop-Group.com

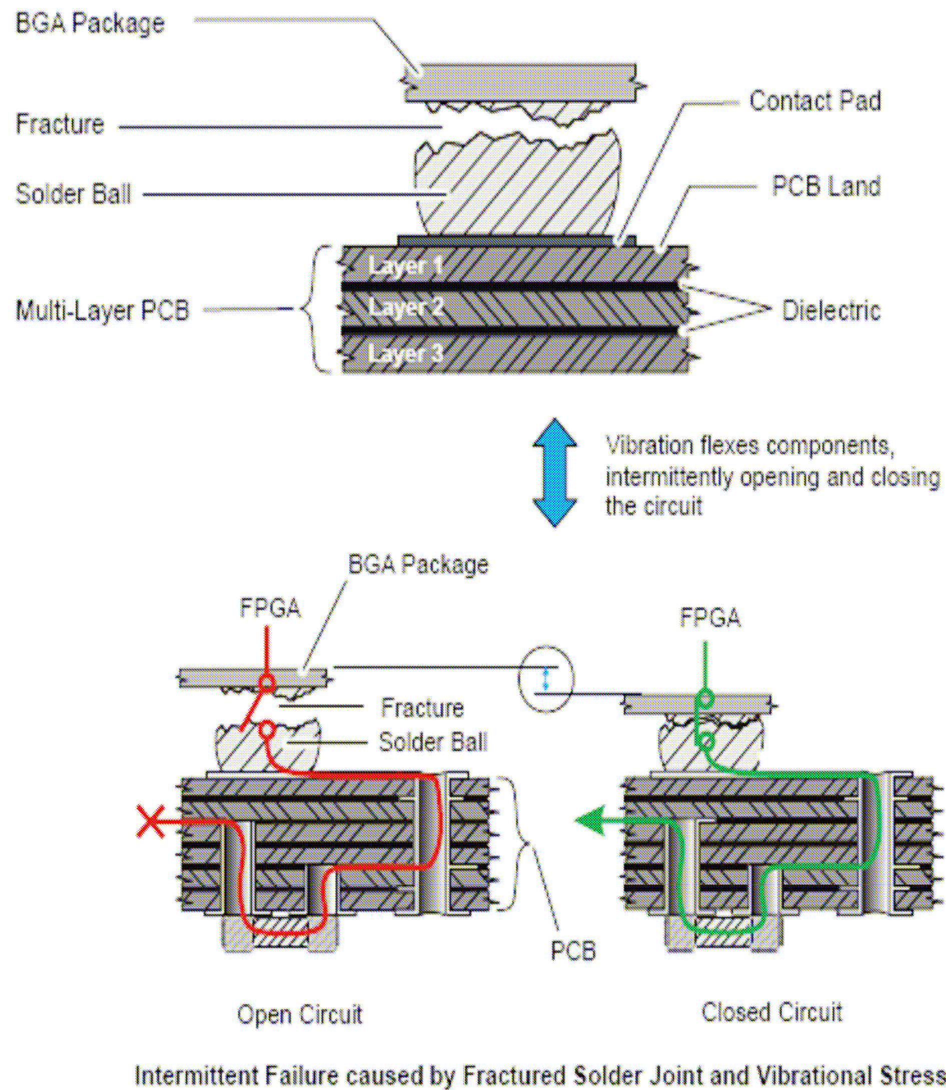
Ridgetop Group Inc

State of the Art: Solder Balls, Cracks and Fractures

- Detects faults in solder-joint networks of FPGAs



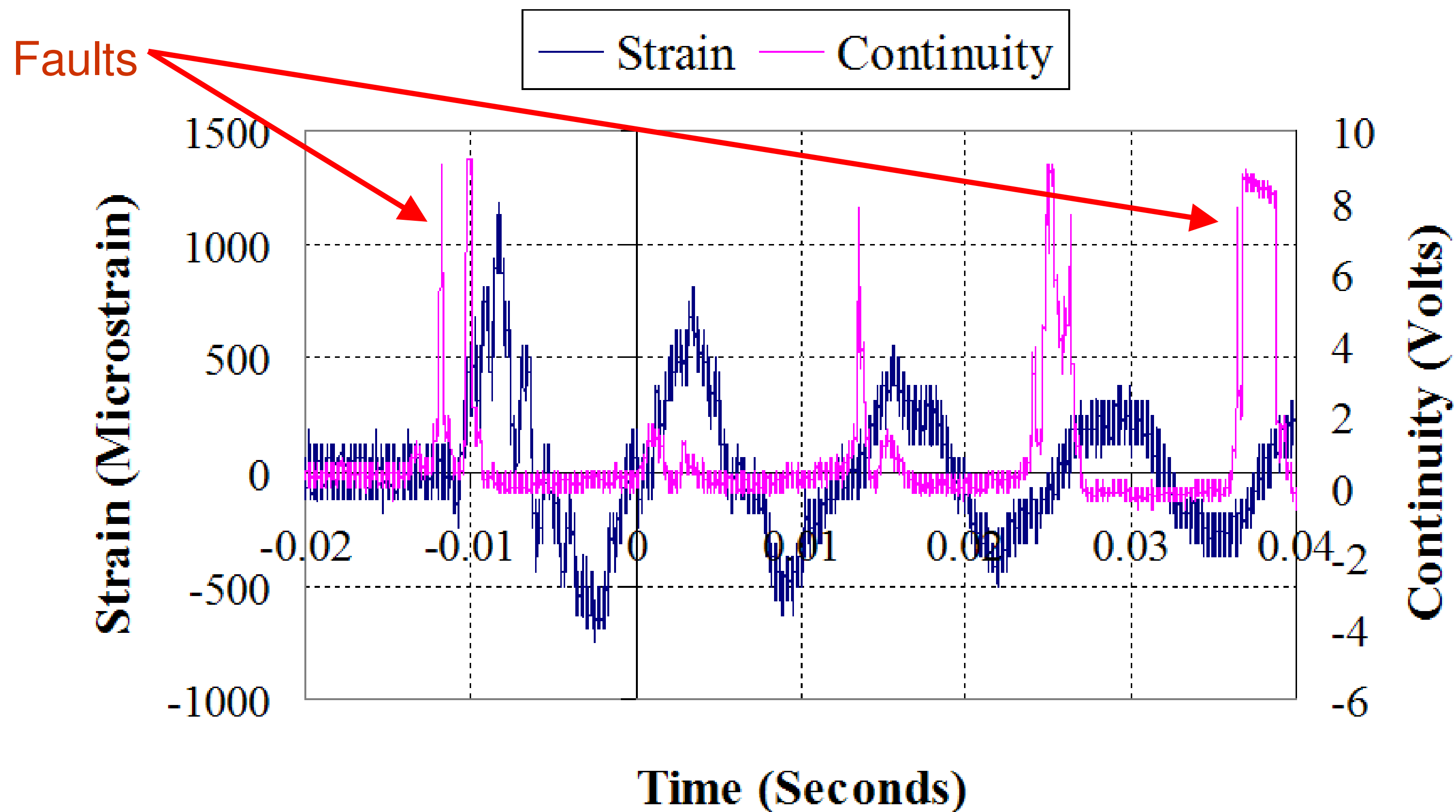
State of the Art: Fractures and Intermittency



Intermittent Failure caused by Fractured Solder Joint and Vibrational Stress

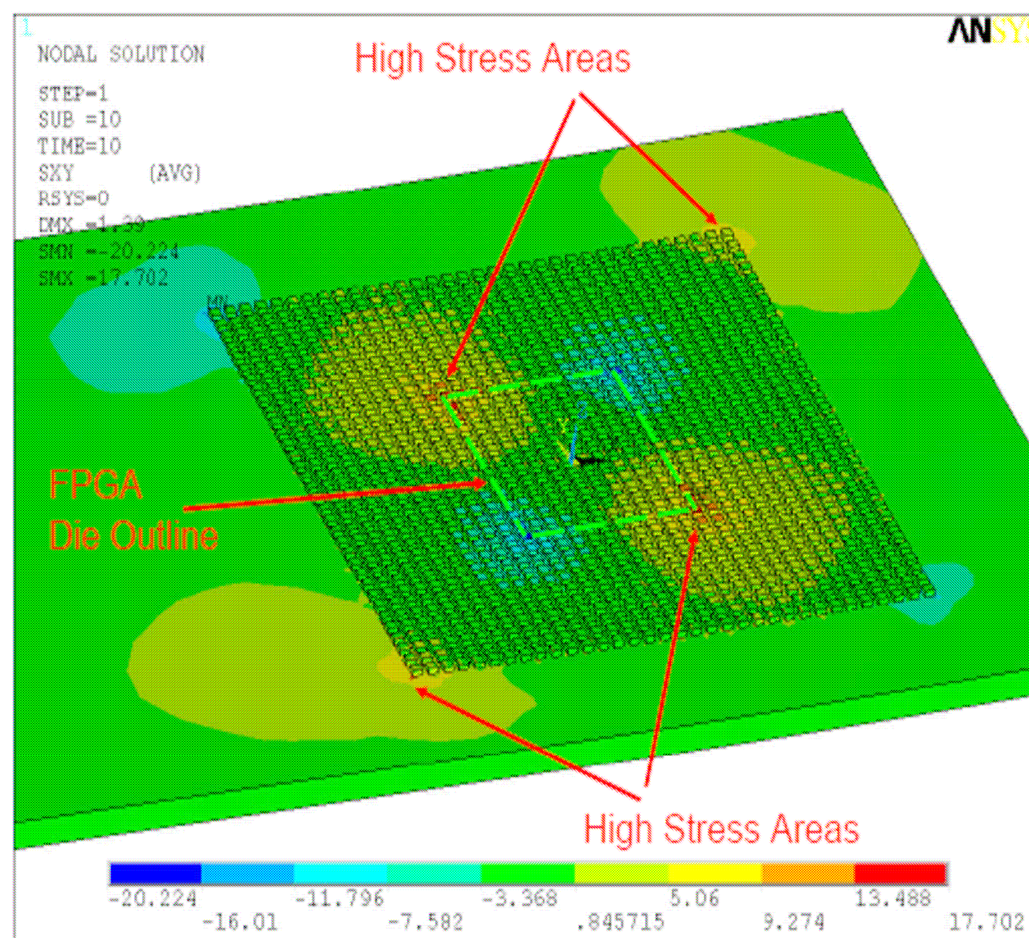
State of the Art: Intermittent Faults in FPGAs

- Faults are intermittent (drop test, CAVE, Auburn Univ.)
  - Occur during periods of increasing strain
  - Multiple occurrences per cycle
  - Industry standard: 200 ⌽ +, 200 ns +



State of the Art: High Stress Areas

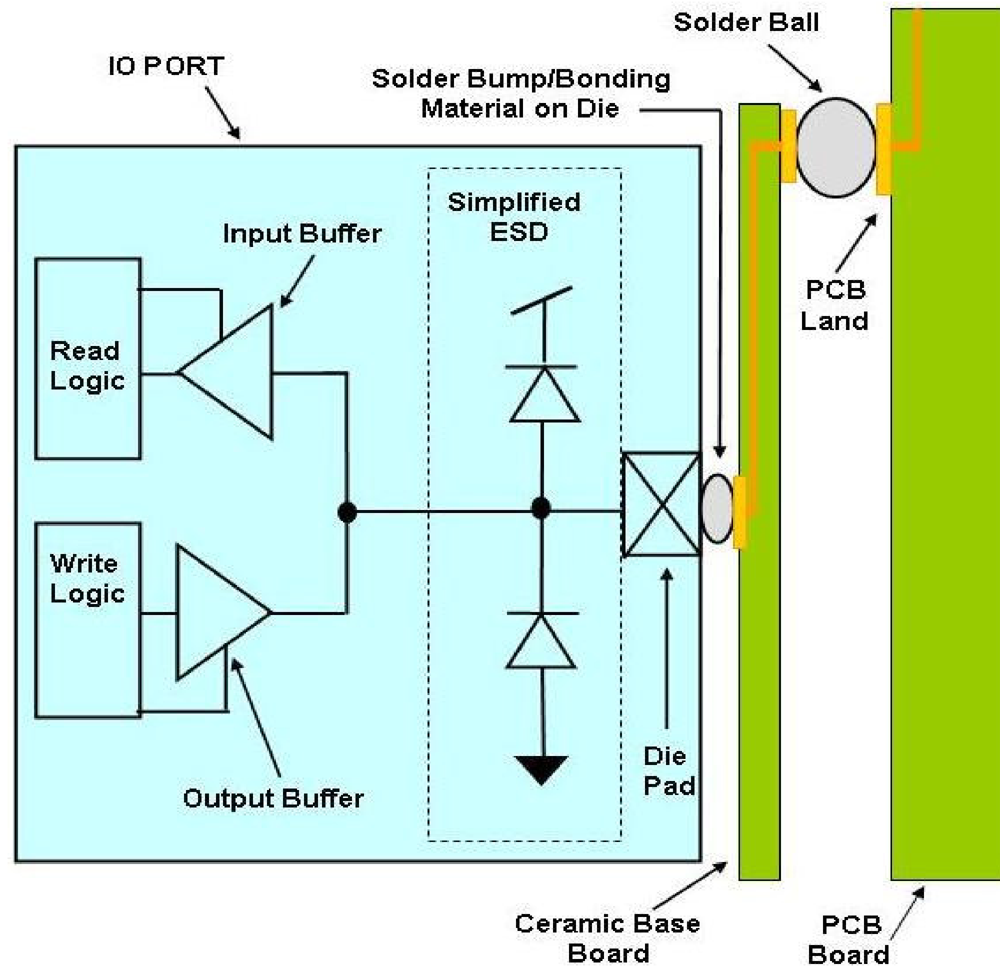
- Corner pins likely to fail first
  - High stress areas
  - Corners of the FPGA package and the FPGA die



Ridgetop Group Inc

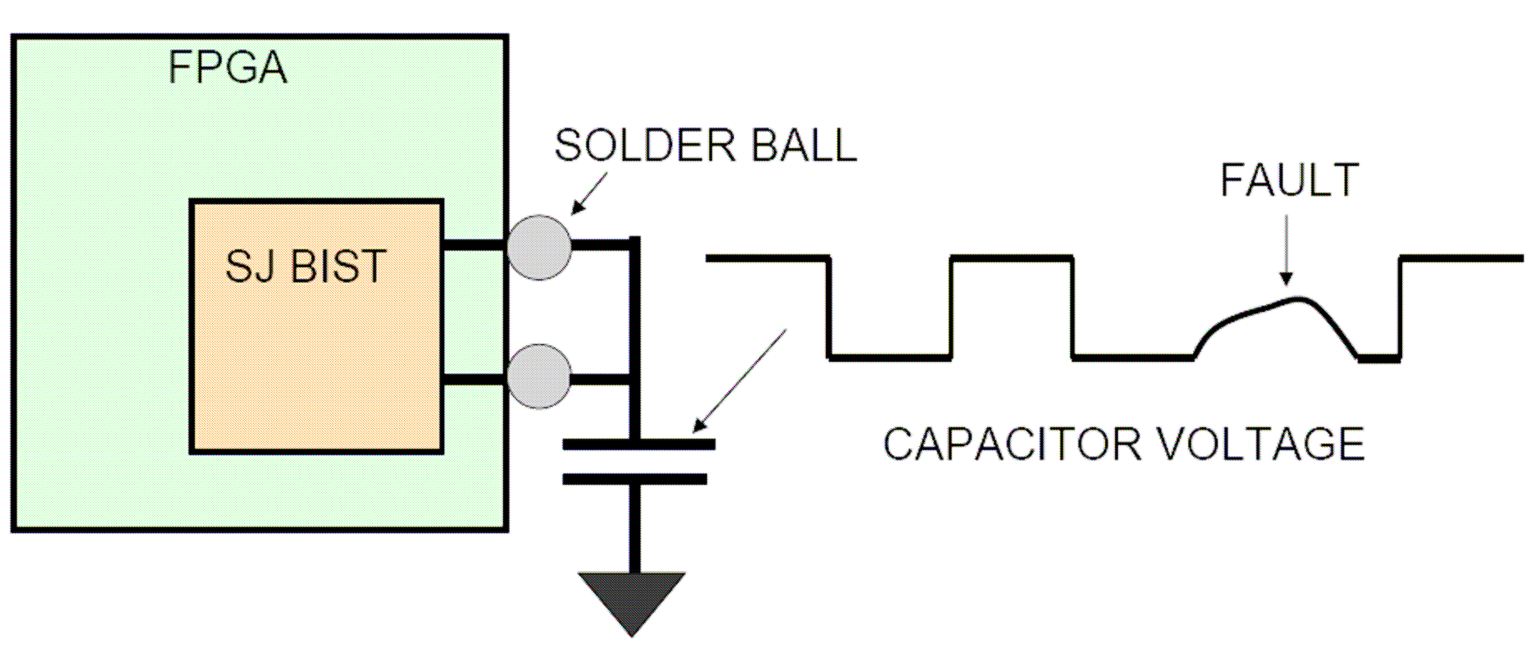
State of the Art: FPGA I/O Ports

- I/O ports are not amenable to direct measurement
  - No direct path to ground
  - Ports are powered



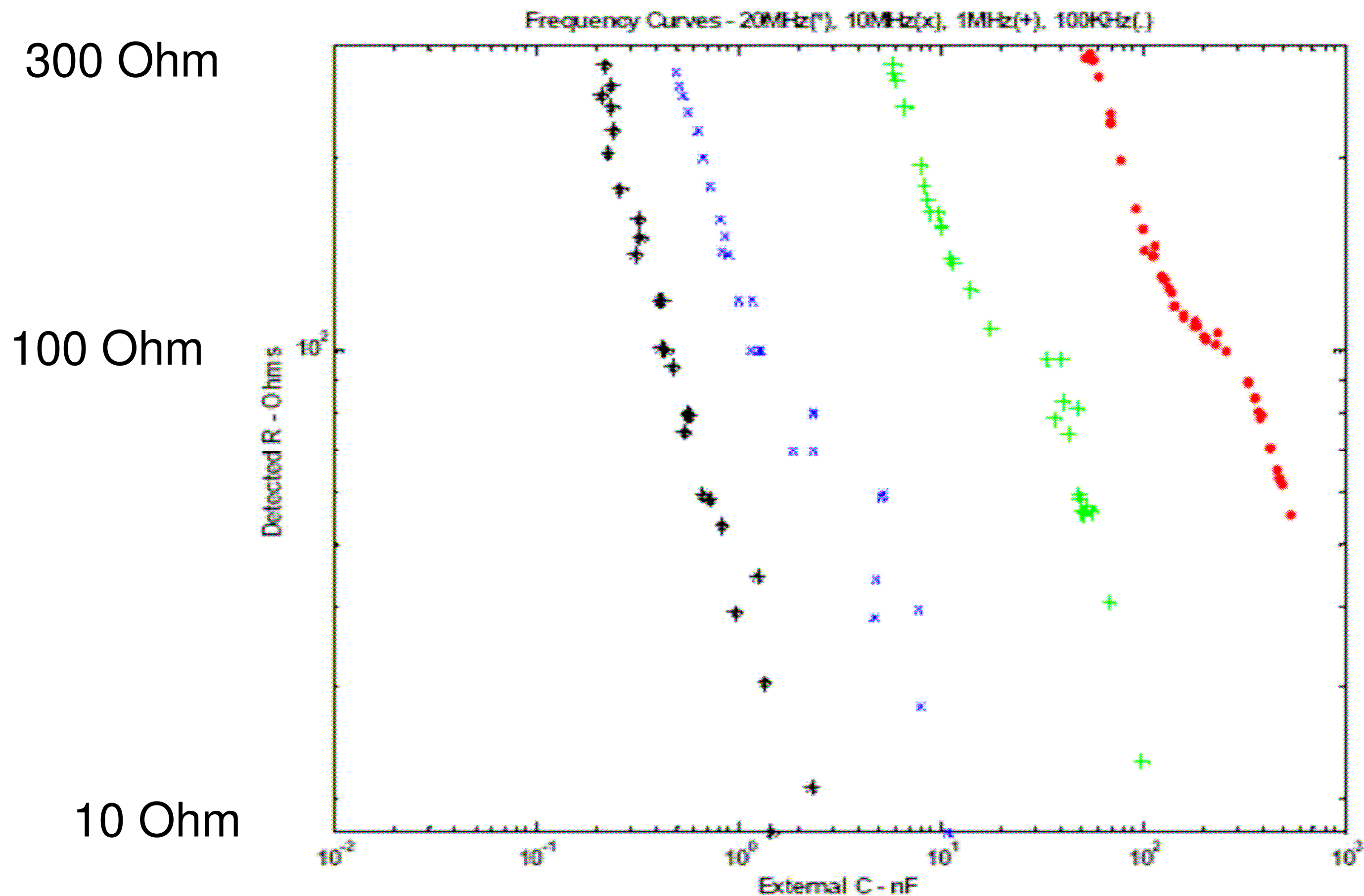
SJ Built-in-Self Test™ (SJ BIST™) - Fault Sensor

- Verilog firmware core (patent pending)
  - Each core tests two I/O pins
  - Pins are externally wired together
  - Small capacitor connected to the two pins



SJ BIST™ - CLK, Capacitor, Detectable Fault Resistance

- No false alarms, detection dependent on
  - Operating clock frequency and capacitor value
  - Desired sensitivity

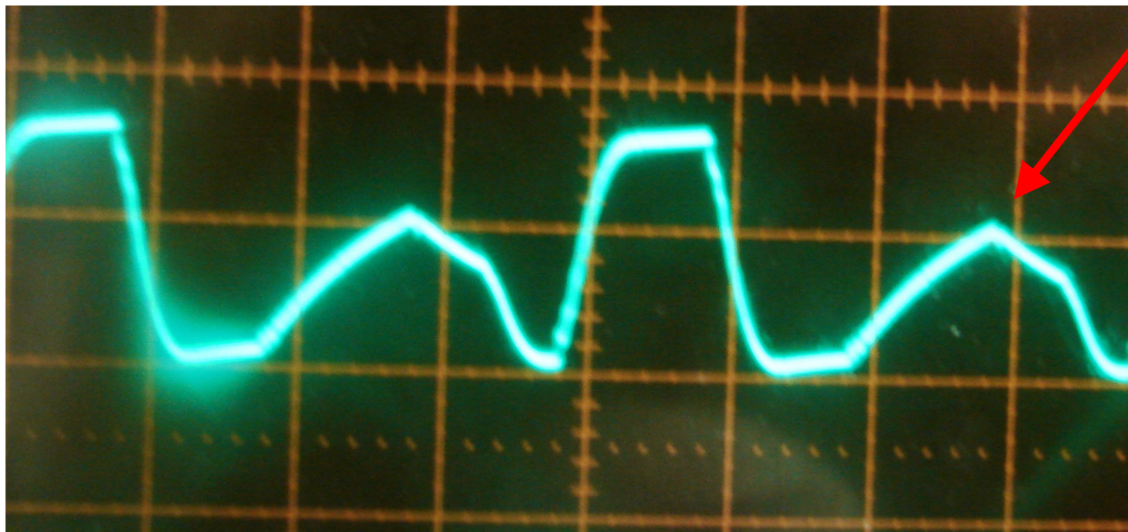


Ridgetop Group Inc

SJ BIST™ - Ridgetop Group Test Result

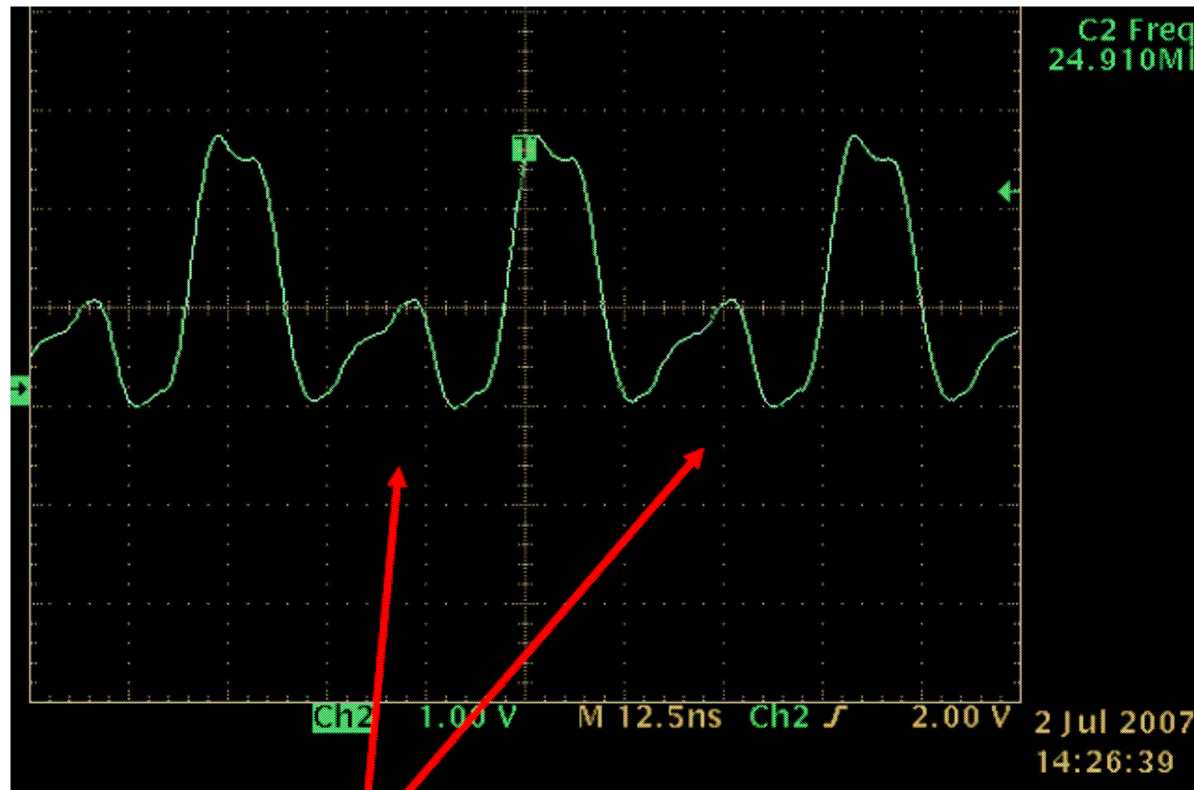
- SJ BIST specifications
  - Sensitivity: as least as low as 100 ⌖
  - Resolution: guaranteed two clock periods
  - Detectable as short as ½ of a clock period
  - 50 MHz clock
    - o 40-ns guaranteed detection
    - o 10-ns detection possible

100 ⌖ fault
1 MHz clock



SJ BIST™ - Daimler and CAVE Test Result

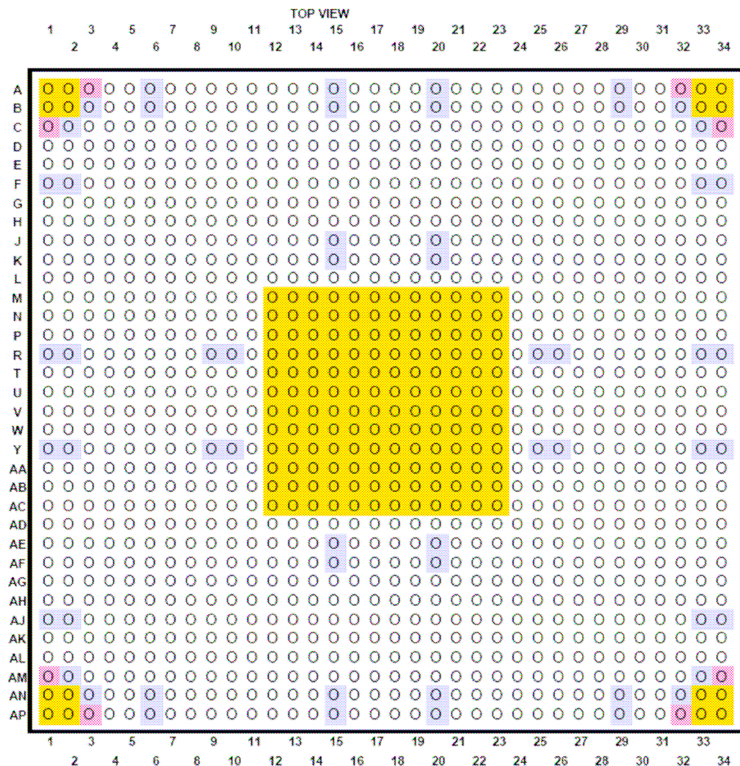
- Independent test results
  - Same as obtained by Ridgetop Group
  - No false alarms

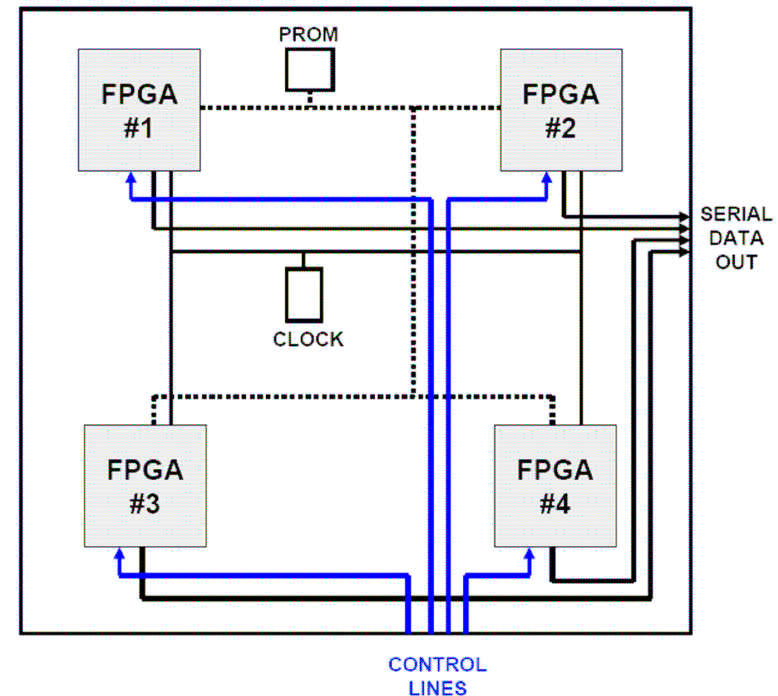


300 Ohm Fault

SJ BIST™ - HALT Design of Experiment

- HALT test boards
  - 32 core groups, 64 test pins per FPGA (shaded pins)
  - 4 FPGAs on each board
  - 4 boards
  - Orange: reserved use by XILINX

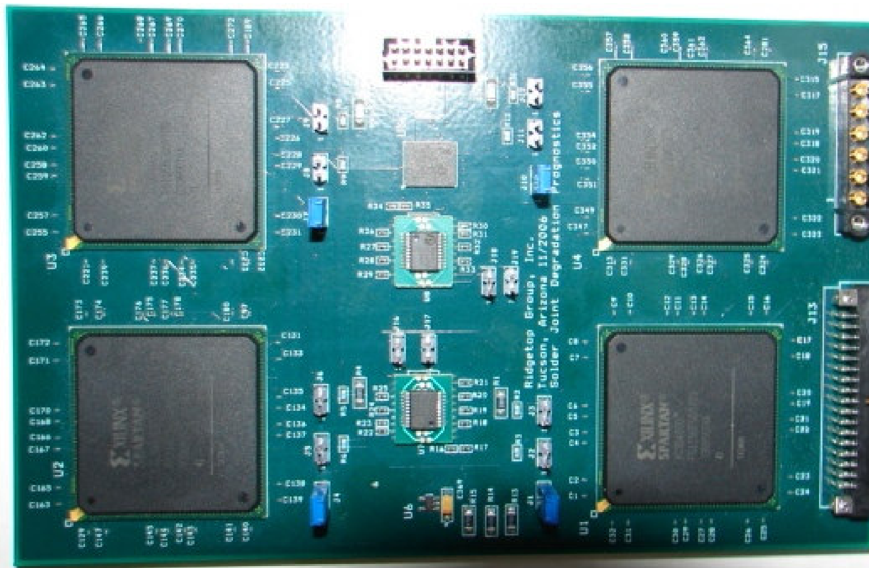




Ridgetop Group Inc

SJ BIST™ - HALT Board, Demo Box

- TRL 7 – Licensing Ts & Cs are available
  - HALT testing at 2 non-Ridgetop locations
  - Demonstration box for evaluation by missile manufacturer

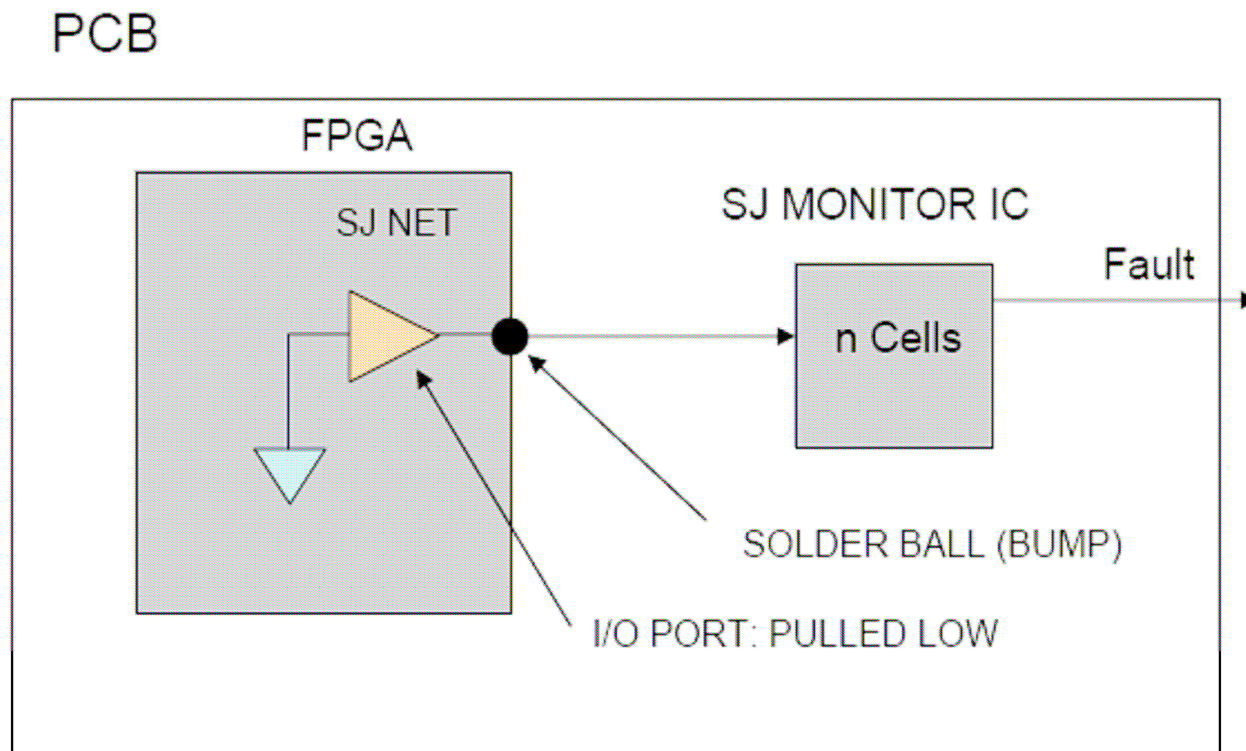


HALT board

Demonstration box

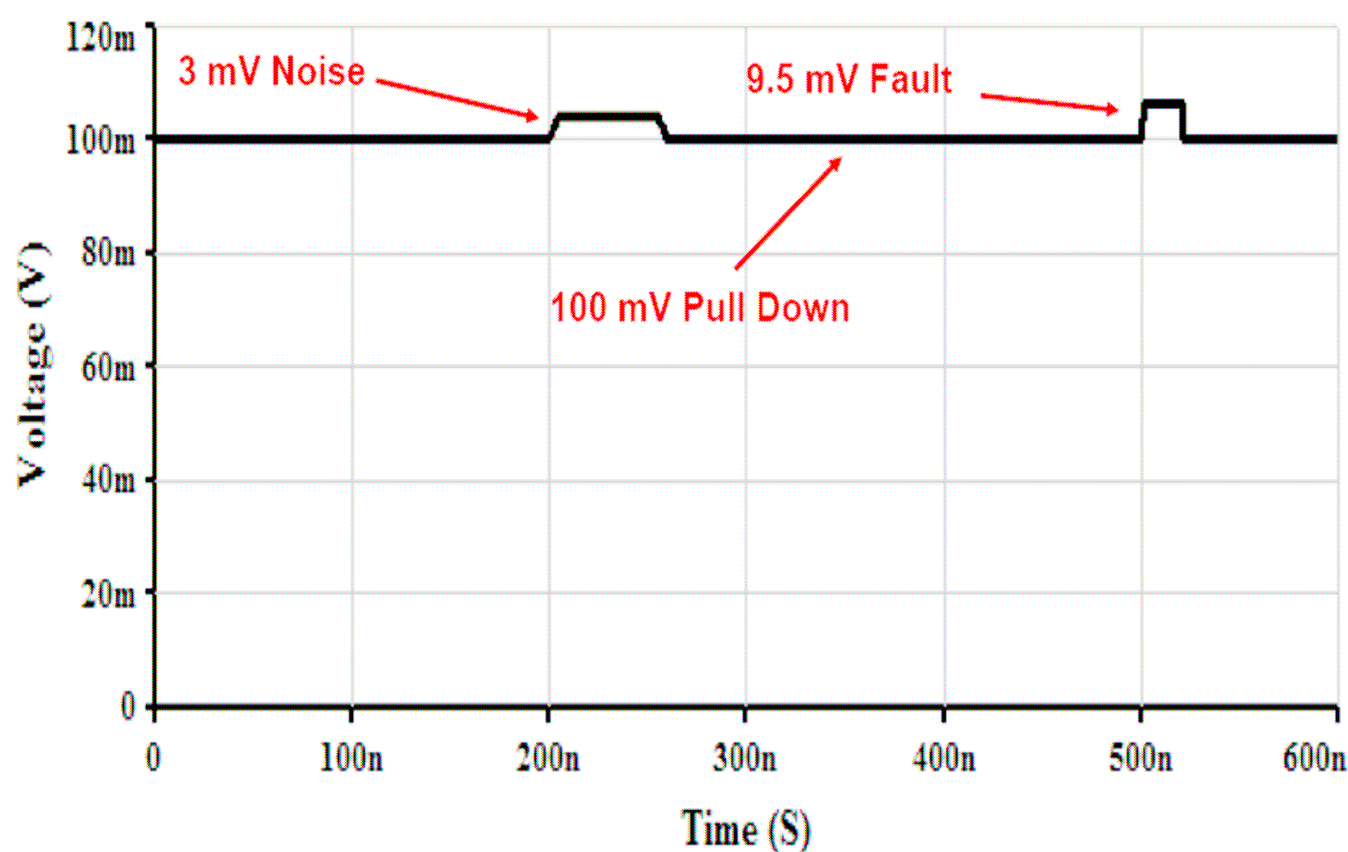
SJ Monitor™

- SJ Monitor™ block diagram (patent pending)
  - Faults in solder-joint pins of FPGAs are intermittent in nature
  - Low power design for use as a 24x7 monitor
  - IC chip on same board as FPGA
  - Complementary circuit will test powered off FPGA



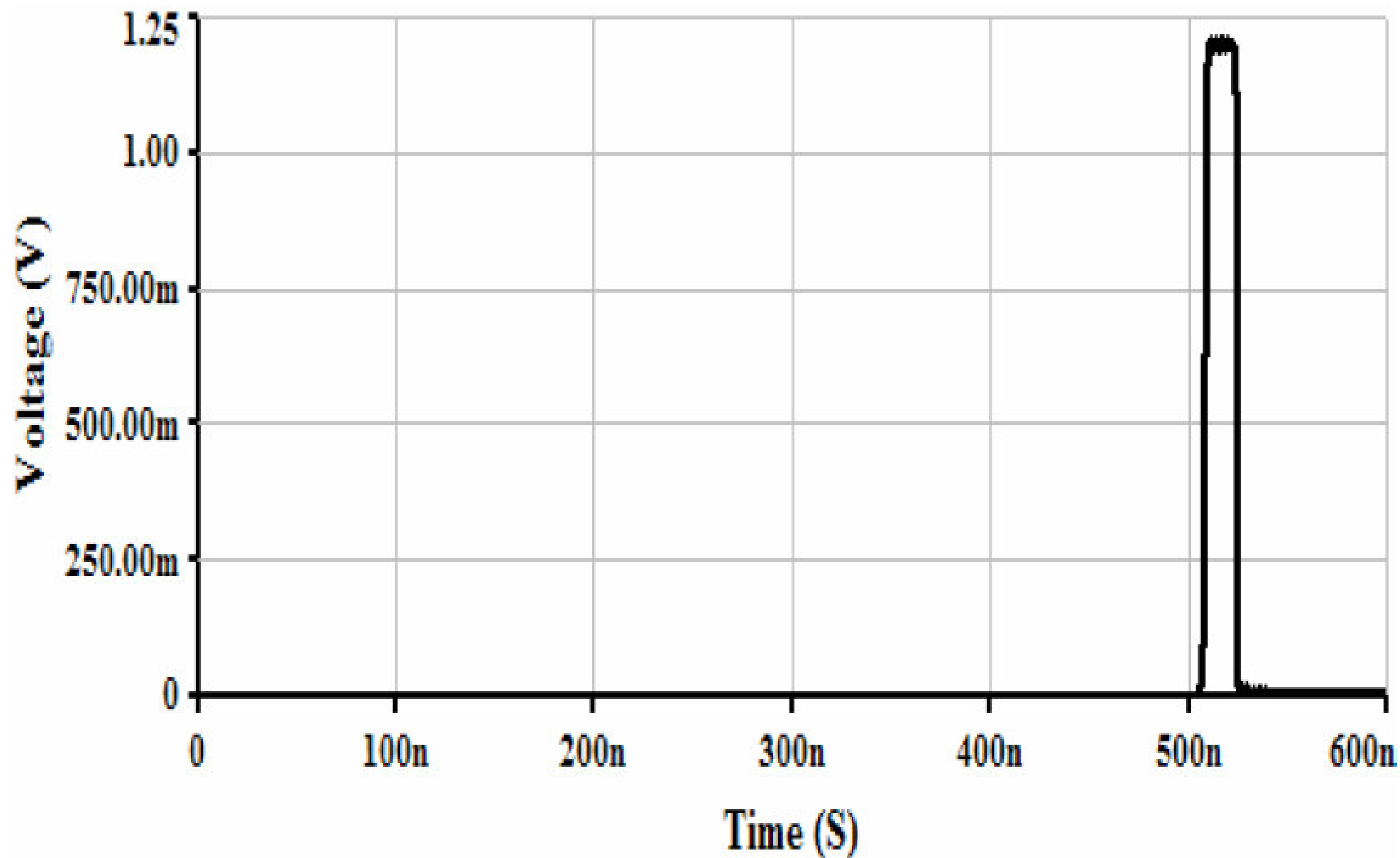
SJ Monitor™

- I/O pin signals
  - Insensitive to pull-down Voltage: 0 to 300 mV
  - Input signal-to-noise ratio: 3.2



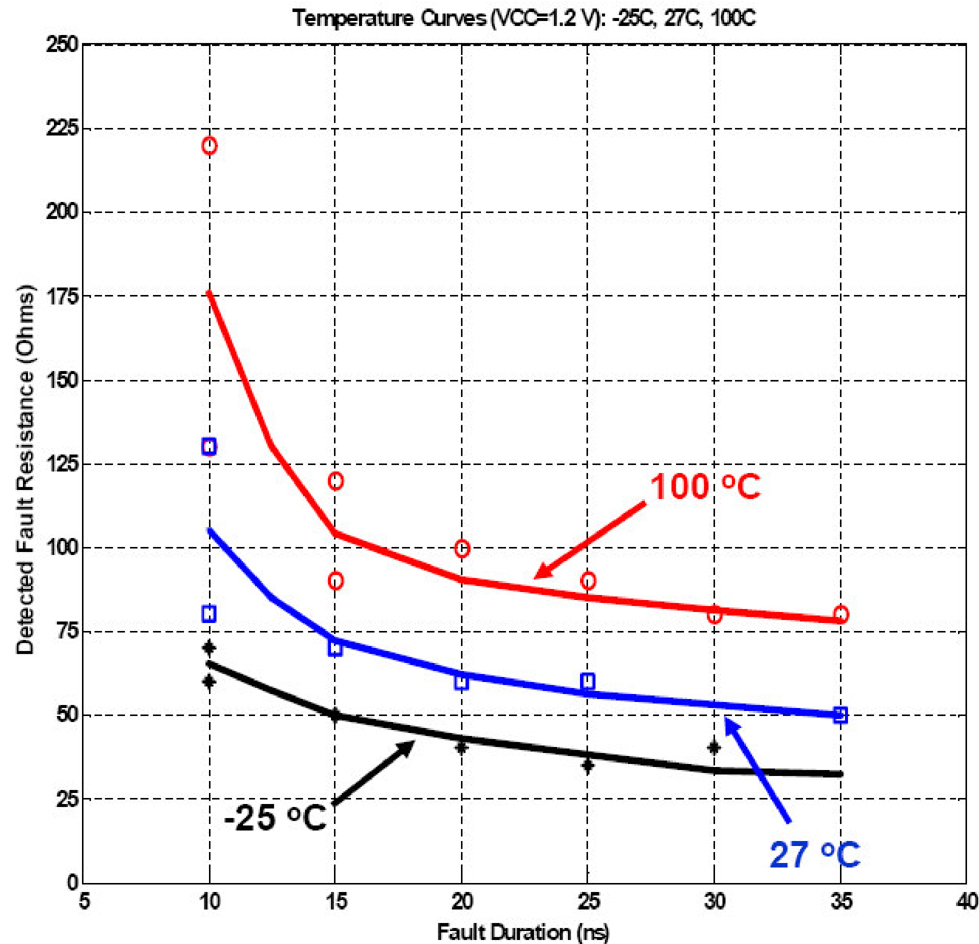
SJ Monitor™

- Signal conditioned
  - Digital ‘1’ when fault is detected
  - Noise suppressed to less than 1mV



SJ Monitor™

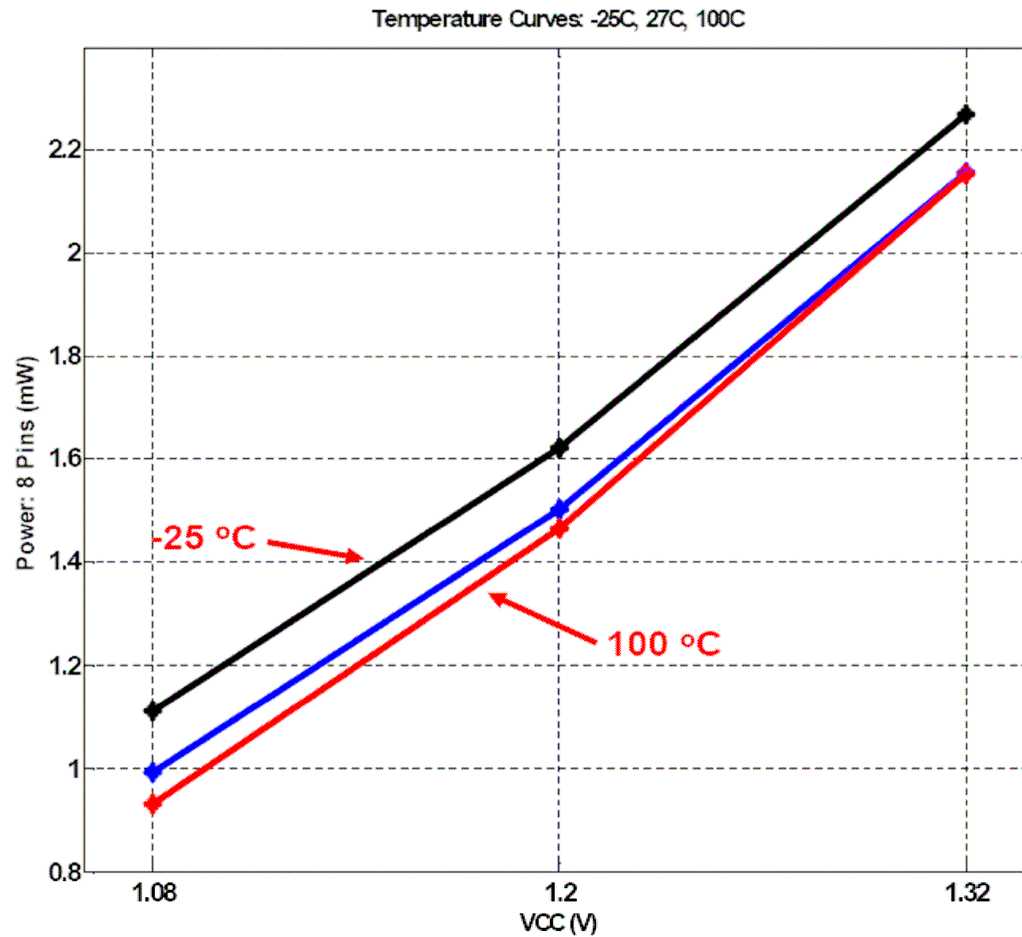
- Fault detection
  - At least as low as 100 Ohm
  - At least as short as 15 ns



Ridgetop Group Inc

SJ Monitor™

- Low power IC:
  - Between 0.9 and 2.4 mW



SJ BIST™ - Deliverables

Sales Fact Sheet: NC, available now
Data Sheet: NC, available now
Installation and Use Guide: Licensed material
Limited support and engineering service hours

per license agreement
and/or negotiated agreement

Demonstration Box – Purchase

part of price can be applied to license
user manual
does not include Installation and Use Guide

SJ Monitor™ - In Development and Test

Design and Development

- IBM 130-nm 8RF bulk CMOS, 1.2 V
- Analog circuit design: complete
- Digital circuit building blocks: complete
- Simulations: complete (corner, temp, power)
- Digital subset
  - IC Layout and Masks
  - DRC, LVS complete – taped out Sep. 2007

Required Tasks to Reach TRL 6 (Phase II Option)

- Layout and mask entire sensor
- Layout and pad IC chip (4 or 8 sensors/chip)
- Fabricate, package and perform verification testing
- Characterization and HALT testing
- Silicon Validation, Data Sheet, License Ts & Cs