# Flexible Fault Tolerance Using the ARTEMIS Reconfigurable Payload Processor

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*Military and Aerospace FPGA and Applications (MAFA) Meeting*
*Palm Beach, FL*
*November 27-29, 2007*

# Responsive Space Mission



- "Responsive Space refers to the ability to rapidly achieve a specific objective through the use of space with rapidly being the operative word. The AFRL Office of Force Transformation suggested that the goal for fielding a new payload is weeks and months and not decades." [1]
- Tactical Satellite (TacSat) program building competency to achieve the Responsive Space challenge [2]
  - Joint AFRL and NRL demonstration program
  - Goal to develop capability to field inexpensive space systems in time of crisis to augment and reconstitute existing capabilities or perform entirely new tactical theater support missions
  - Key success criteria include
    - Develop low cost ($20 million or less) mission-specific spacecraft
    - Rapid deployment with on orbit activation within six days of call up
    - Provide between six to twelve months of reliable mission operations

[1] Lanza, et. al., "Responsive Space Through Adaptive Avionics, Responsive Space Conference, Los Angeles, CA, April 19-22, 2004.
[2] J. Raymond, et. al., "A TacSat Update and the ORS/JWS Standard Bus," Responsive Space Conference, Los Angeles, CA, April 25-28, 2006.

# TacSat-3
## Tactical Ops – Real Time Downlink & C2

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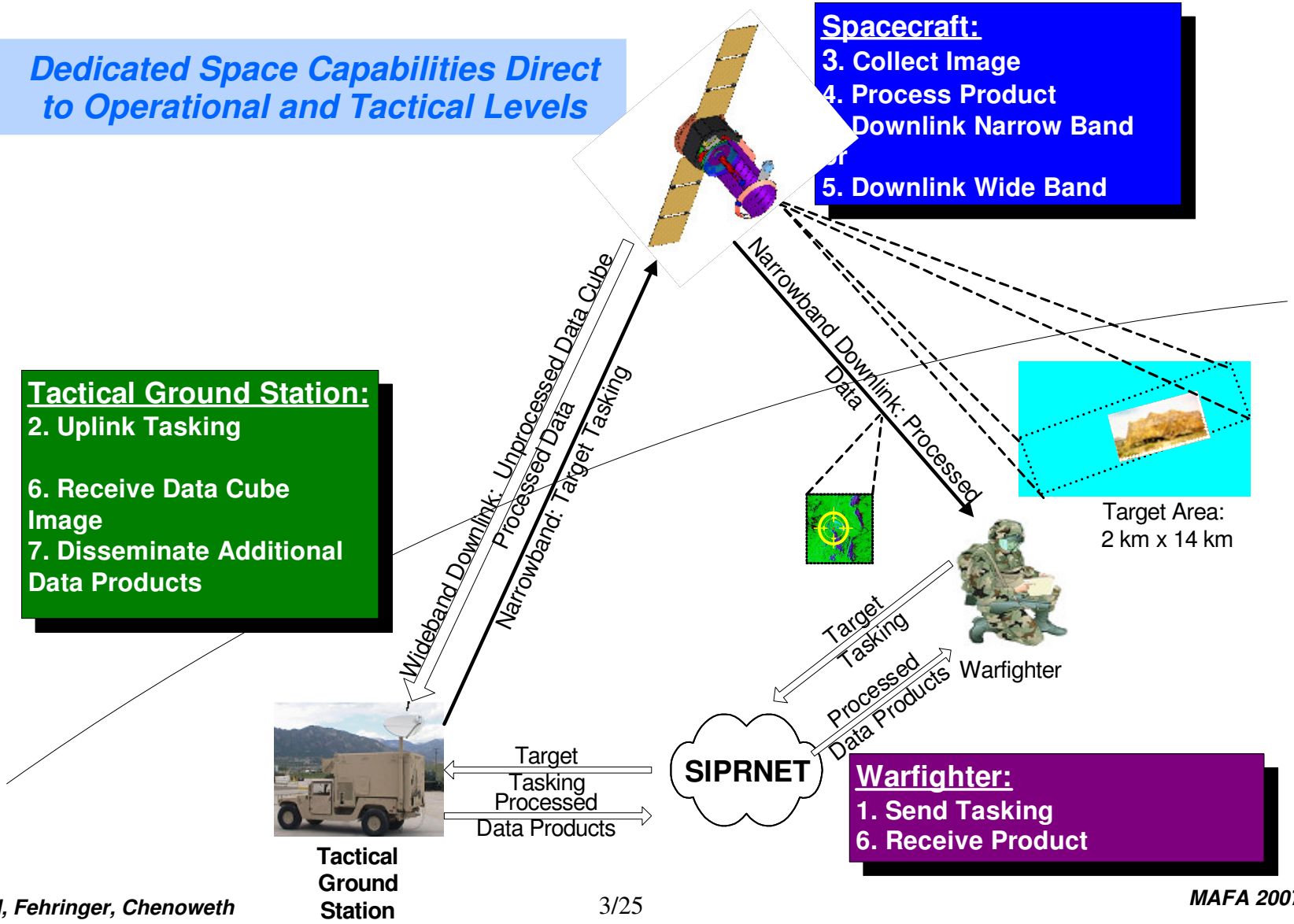
***Dedicated Space Capabilities Direct to Operational and Tactical Levels***



# Display and Target Cue Products Generated by On-Board Processor

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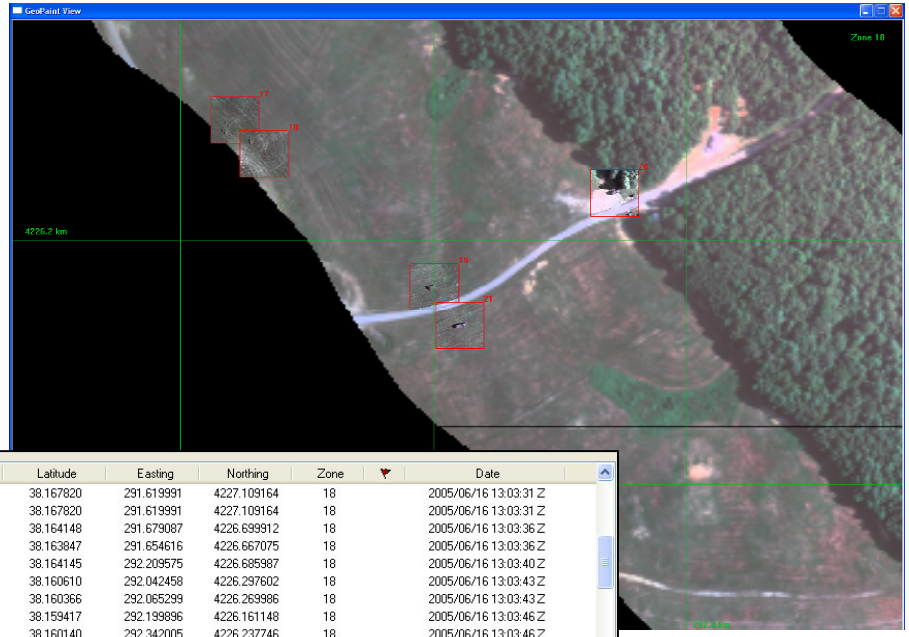
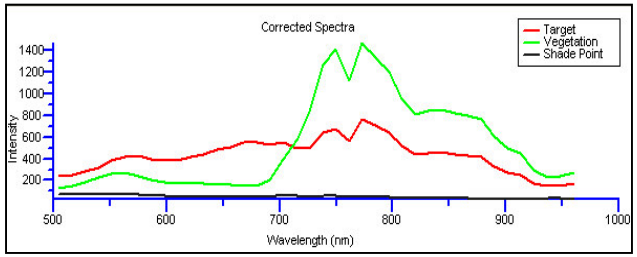
- **Geo-registered false color HSI**
  - **Supports GeoPaint™ display**




- **Target cue reports (text data)**
  - **Date, time, filter ID**
  - **Scan, frame, pixel indices**
  - **Lat,Lon and UTM geolocation**

| ID | Source | HSI Frame # | HSI Pixel # | HRI Line # | HRI Pixel # | Score | Longitude | Latitude | Easting | Northing | Zone | Date |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 | MF Green-tan-net1-... | 236593 | 313 | 2839116 | 3787 | 91.5 | -77.378689 | 38.167820 | 291.619991 | 4227.109164 | 18 | 2005/06/16 13:03:31 Z |
| 13 | Anomaly | 236593 | 313 | 2839116 | 3787 | 67.2 | -77.378689 | 38.167820 | 291.619991 | 4227.109164 | 18 | 2005/06/16 13:03:31 Z |
| 14 | MF Green-tan-net1-... | 236891 | 60 | 2842692 | 844 | 44.6 | -77.377895 | 38.164148 | 291.679087 | 4226.699912 | 18 | 2005/06/16 13:03:36 Z |
| 15 | MF Truck-GreenCan... | 236898 | 18 | 2842776 | 355 | 36.3 | -77.378165 | 38.163847 | 291.654616 | 4226.667075 | 18 | 2005/06/16 13:03:36 Z |
| 16 | MF Truck-GreenCan... | 237178 | 479 | 2846136 | 5718 | 38.6 | -77.371841 | 38.164145 | 292.209575 | 4226.685987 | 18 | 2005/06/16 13:03:40 Z |
| 17 | MF Green-tan-net1-... | 237323 | 33 | 2847876 | 530 | 46.7 | -77.373633 | 38.160610 | 292.042458 | 4226.297602 | 18 | 2005/06/16 13:03:43 Z |
| 18 | MF Green-tan-net1-... | 237350 | 33 | 2848200 | 530 | 44.0 | -77.373365 | 38.160366 | 292.065299 | 4226.269986 | 18 | 2005/06/16 13:03:43 Z |
| 19 | MF Green-tan-net1-... | 237492 | 93 | 2849904 | 1228 | 44.3 | -77.371798 | 38.159417 | 292.199896 | 4226.161148 | 18 | 2005/06/16 13:03:46 Z |
| 20 | MF Green-tan-net1-... | 237524 | 277 | 2850288 | 3368 | 39.9 | -77.370200 | 38.160140 | 292.342005 | 4226.237746 | 18 | 2005/06/16 13:03:46 Z |
| 21 | MF Truck-GreenCan... | 237520 | 92 | 2850240 | 1216 | 37.6 | -77.371563 | 38.159138 | 292.219712 | 4226.129667 | 18 | 2005/06/16 13:03:46 Z |
| 22 | MF Green-tan-net1-... | 238456 | 240 | 2861472 | 2938 | 43.5 | -77.361036 | 38.153202 | 293.125337 | 4225.447295 | 18 | 2005/06/16 13:04:02 Z |

- **Target chips**
  - **ROI centered on detection**
  - **Georegistered and fused false-color HSI and HRI**
  - **Target spectra**



# ARTEMIS Goals



- **ARTEMIS designed for Responsive Space**
  - Low cost
  - High Performance
  - Rapid deployment through adaptability

- **Key System Development Requirements**
  - Scalable processing from 9 to over 400 GFLOPS
  - Reconfigurable, on-orbit
  - Support Multi-Terabit Data Storage
  - Usage of open standards
  - SEE Tolerant system
  - Flexible I/O architecture
  - Provide user interface for rapid development

- **The Application Independent Processor fulfills ARTEMIS goals**

# Application Independent Processor (AIP)

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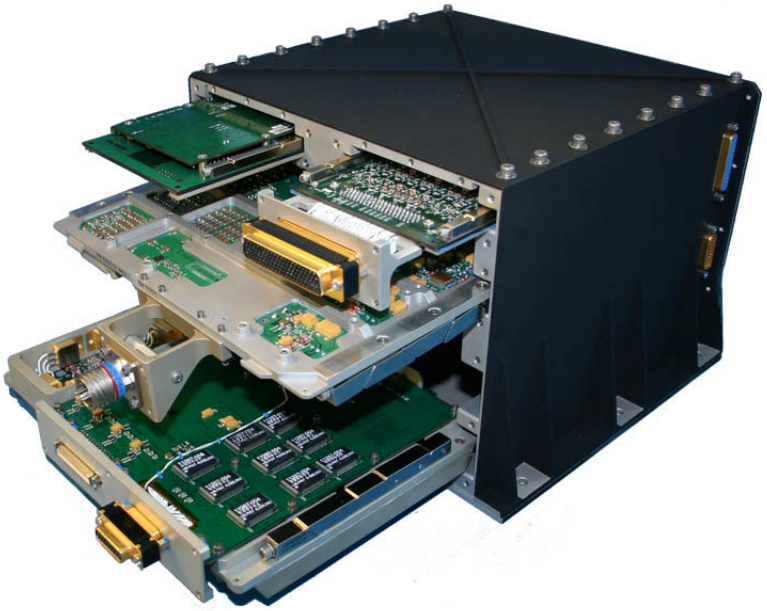
*Aerospace Data Storage and Processing Systems*

- Space Qualified On-Board Processor System
  - Based on both scalar and reconfigurable computing
  - AFRL TacSat 3 flight program
- (Up to two) Reconfigurable Computer(s)
  - V4 based RCC with 256 MB DDRII SDRAM per Coprocessor (COP)
  - High speed SERDES backplane bus
  - Over 450,000 logic cells (500 MHz)
  - 15.6 Mb of embedded block RAM (500 MHz)
  - 288 18x18 multipliers (500 MHz)
  - 20 Watts
- G4 PowerPC SBC
  - 600 DMIPs, 1.2 GFLOP
  - VxWorks Based
  - Gigabit Ethernet and Spacewire
  - 16 Watts
- Memory and I/O Mezzanine (ARTEMIS Personality Mezzanine)
  - 16 GBytes flash memory
  - Camera link, analog, digital
- Payload Power Switching
  - 28V switched power to payload
- DC/DC – 82% efficient supply
- SWaP (estimate)
  - Mass: EM 18 lbs (no conformal coat)
  - Size: 7.82H x 11.41W x 10.0D inches
  - Power: 40 Watts (EM measured)
  - -10 to +50°C



# AIP System Architecture

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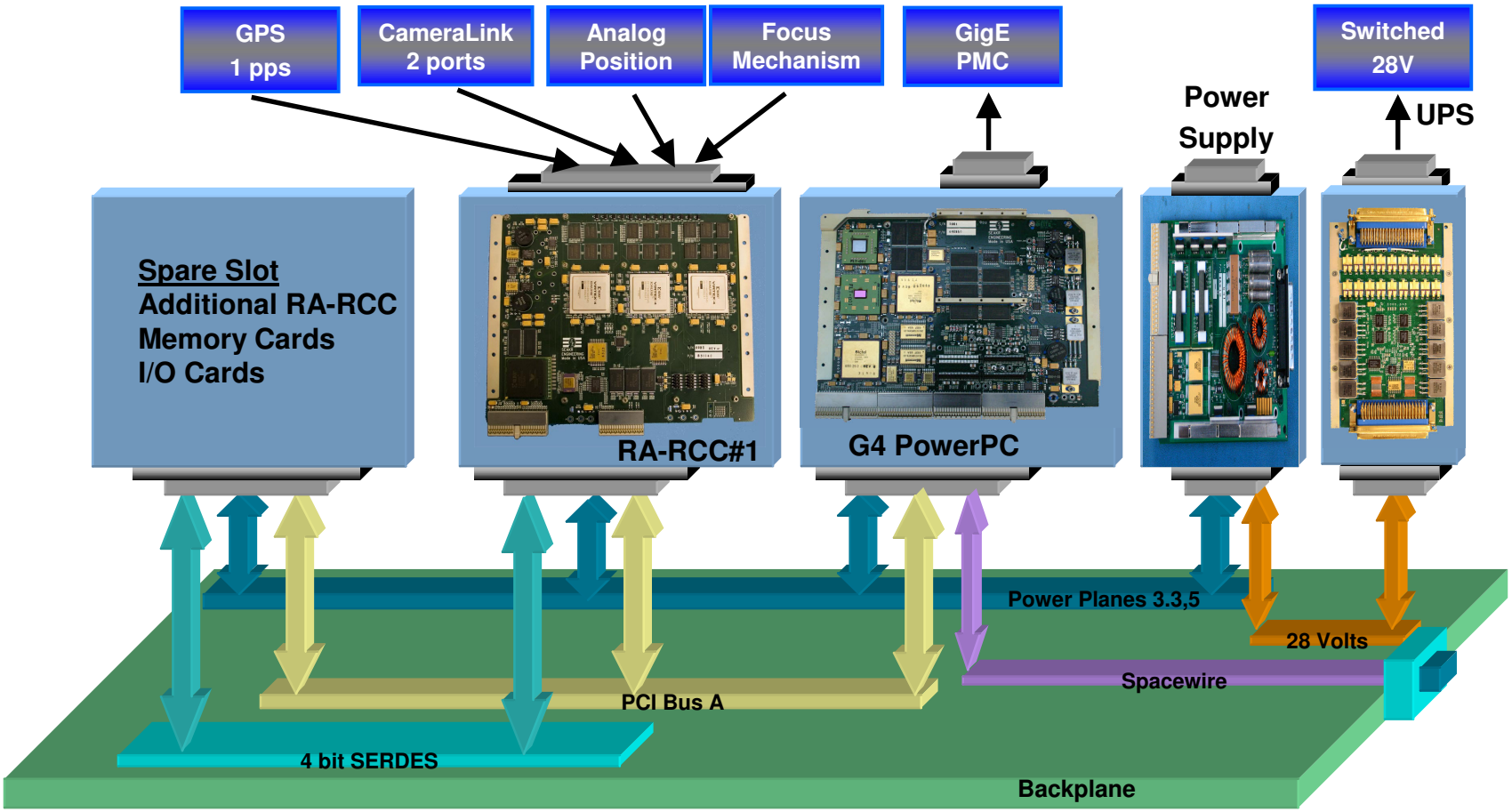
**Shown in the TacSat3 ARTEMIS configuration**



# G4-SBC (PowerPC)

SEAKR Engineering, Inc.

*Aerospace Data Storage and Processing Systems*

- **6u cPCI (32b/33MHz) – PCI**
- **Flash**
  - 512 Mbytes user-available memory
  - Reed Solomon EDAC with Single symbol correct
  - 56Mbytes/sec for single beat transfers
- **SDRAM**
  - 256Mbytes user-available with full chip correct EDAC
  - Mode register refresh on command
- **EEPROM**
  - 128kbytes user-available with Hamming EDAC
  - Single bit correct & Double bit detect Cache
- **Processor Cache**
  - 32kbyte Level 1
  - 256kbyte Level 2
- **PMC**
  - Local PCI bus (PCI/PCI)
  - Ethernet signals routed to backplane on J3
- **Mass and Power**
  - Mass: 0.55 kg, 1.22 lbs
  - Power: 3.3V/1A, 5V/2A, +12V/0.135A, -12V/0.014A

- **I/O**
  - Spacewire (2 ports)
  - RS422 (2 ports)
  - Temperature Sensor
  - Emulator Signals
  - Ethernet via PMC Mezzanine
  - GPIO (16 bits input, 16 bits output)
  - Boot-status and error indication (4 bits)

**G4 Prototype cPCI**

# Low Voltage High Current DC/DC Converters

SEAKR Engineering, Inc.

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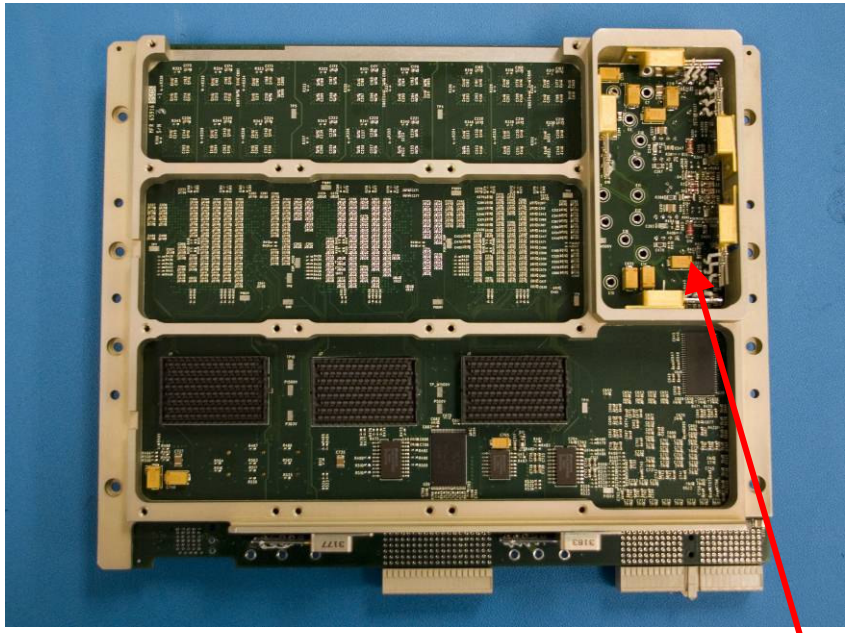
- Devices require low voltage and high current.
- Must use Point Of Load POL power supplies for proper regulation
- Developed Radiation tolerant POL mezzanine
  - Programmable voltage down to 1.0V at 12A
  - 85% efficiency
  - Mezzanine card for design reuse and flexibility

POL DC/DC Converter Mezz



RA-RCC Back View

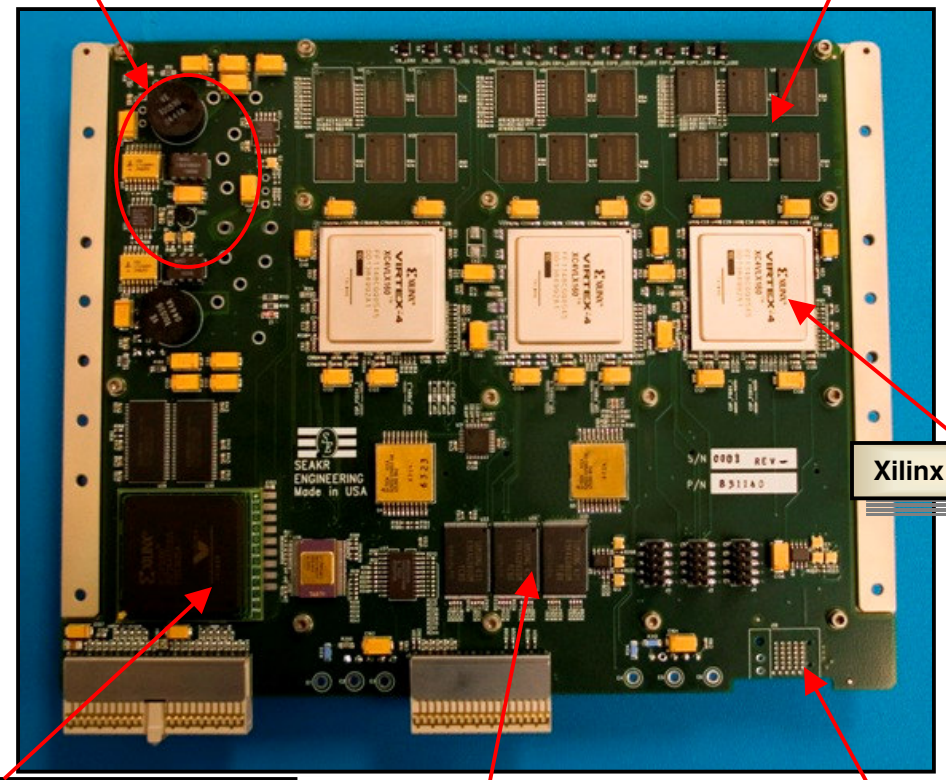
POL Power Supply

# RA-RCC (Virtex 4)

SEAKR Engineering, Inc.



- 3 V4LX160 FPGAs
- TID tolerant to >40krad
  - Higher levels available
- 256MBytes DDRII SDRAM per FPGA
- 170 user defined I/O per FPGA via high-speed Mezz
- Extended 6U cPCI
- Symmetrical Design
- High speed serial I/O
- 62 configuration files stored on-board
- Supports full device level TMR with external majority voting
- Autonomous FPGA scrubbing with SEFI protection and recovery
- High Speed Serial Backplane Interface
- 2.6 lbs with mezzanine
- 9.2 x 7.3 x 1.43”



# Thermal Management

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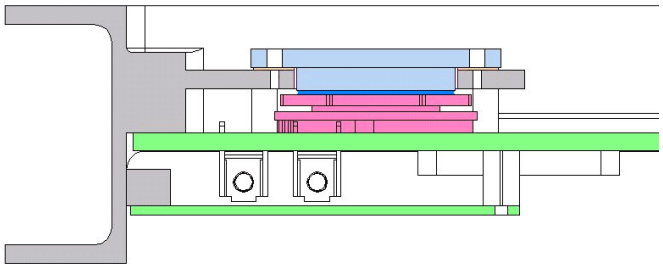
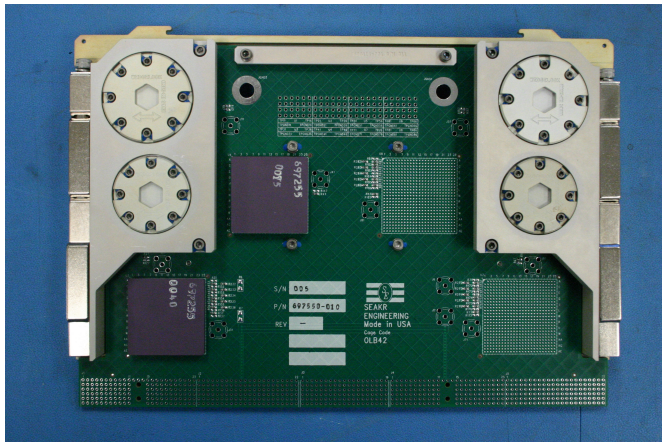
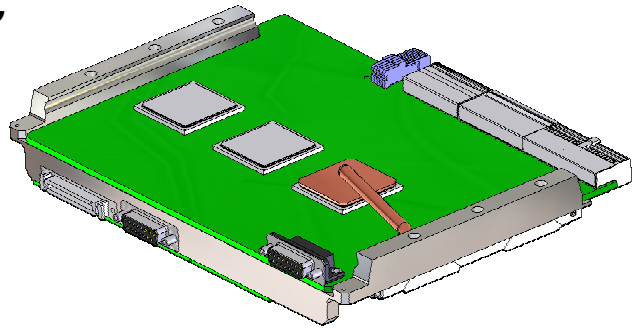
*Aerospace Data Storage and Processing Systems*

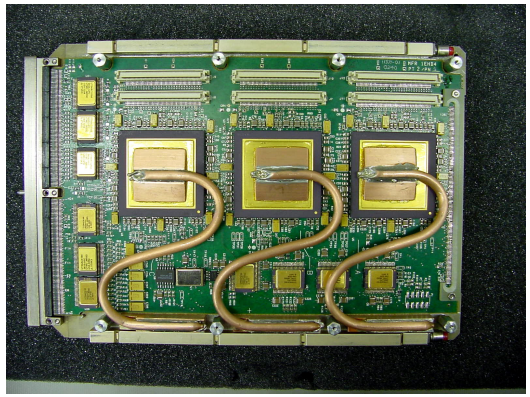
- **Passive Conduction Cooling**
  - Processors can dissipate up to 8 Watts/device
  - Thermal plates
  - Very exact spacing
- **G4-SBC, Athena, PST**





- **Active Conduction Cooling**
  - Processors can dissipate more than 8 Watts/device
  - Heat pipes for high power applications
- **RA-RCC**



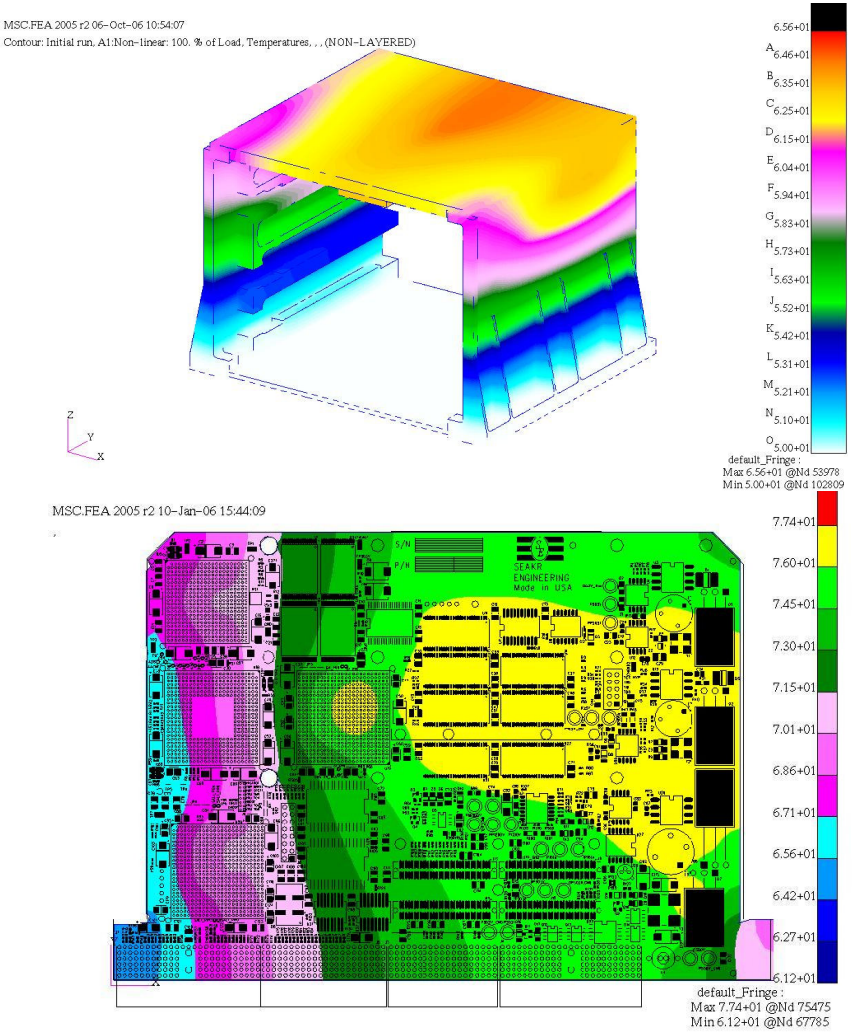


**LANL Cibola**

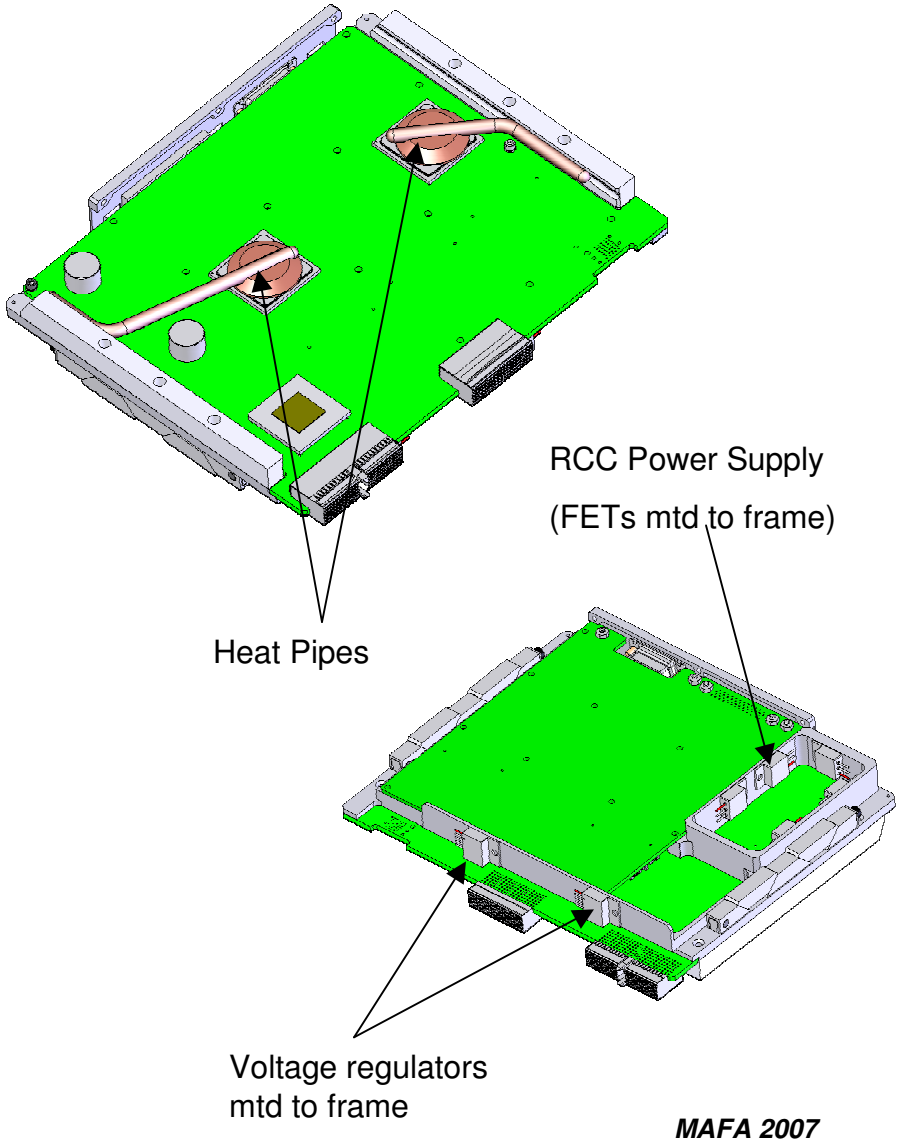
# Thermal Management

SEAKR Engineering, Inc.

*Aerospace Data Storage and Processing Systems*




**G4 Thermal Analysis**



# RCC Heat Pipe Qual Board

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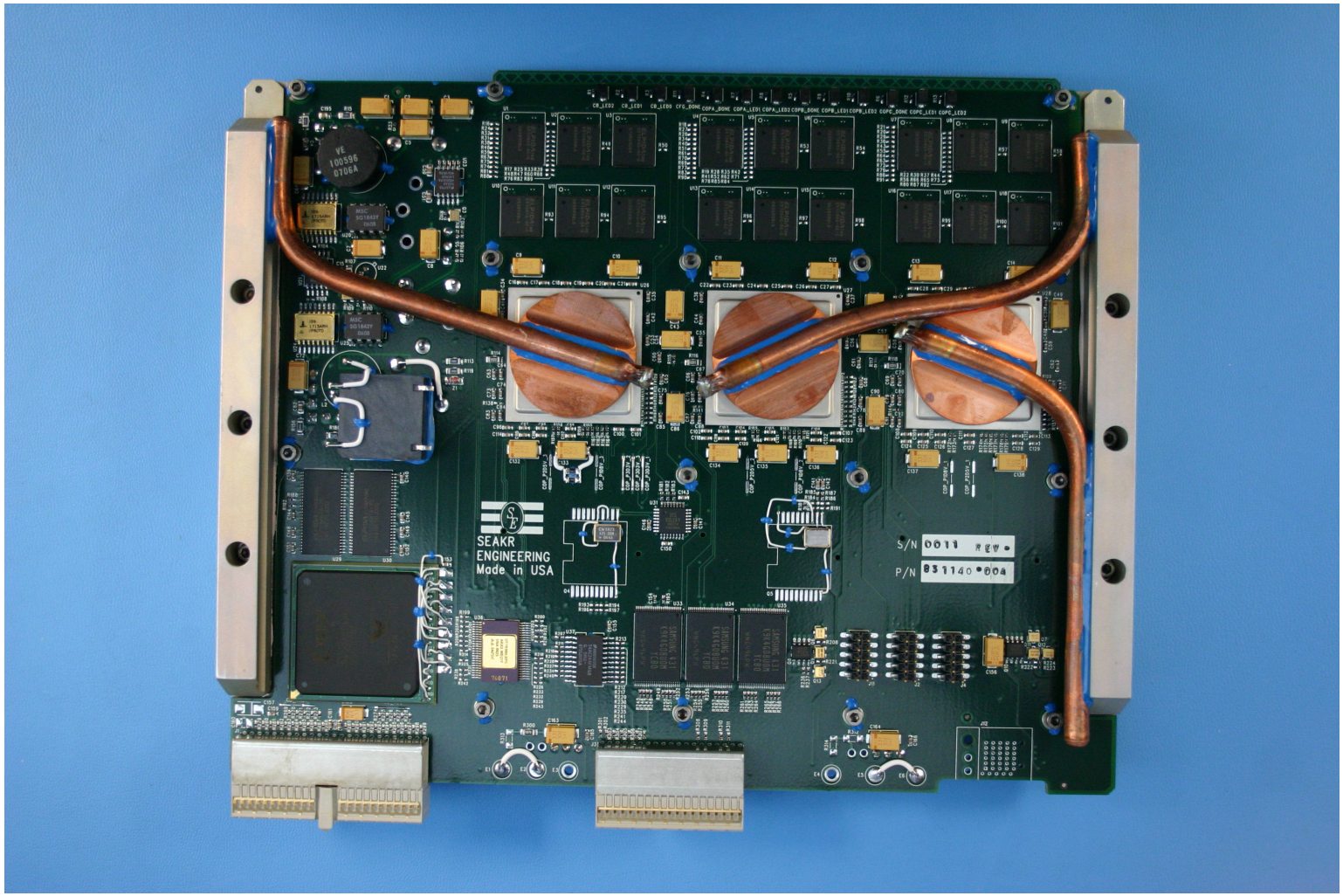

# RA-RCC Block Diagram

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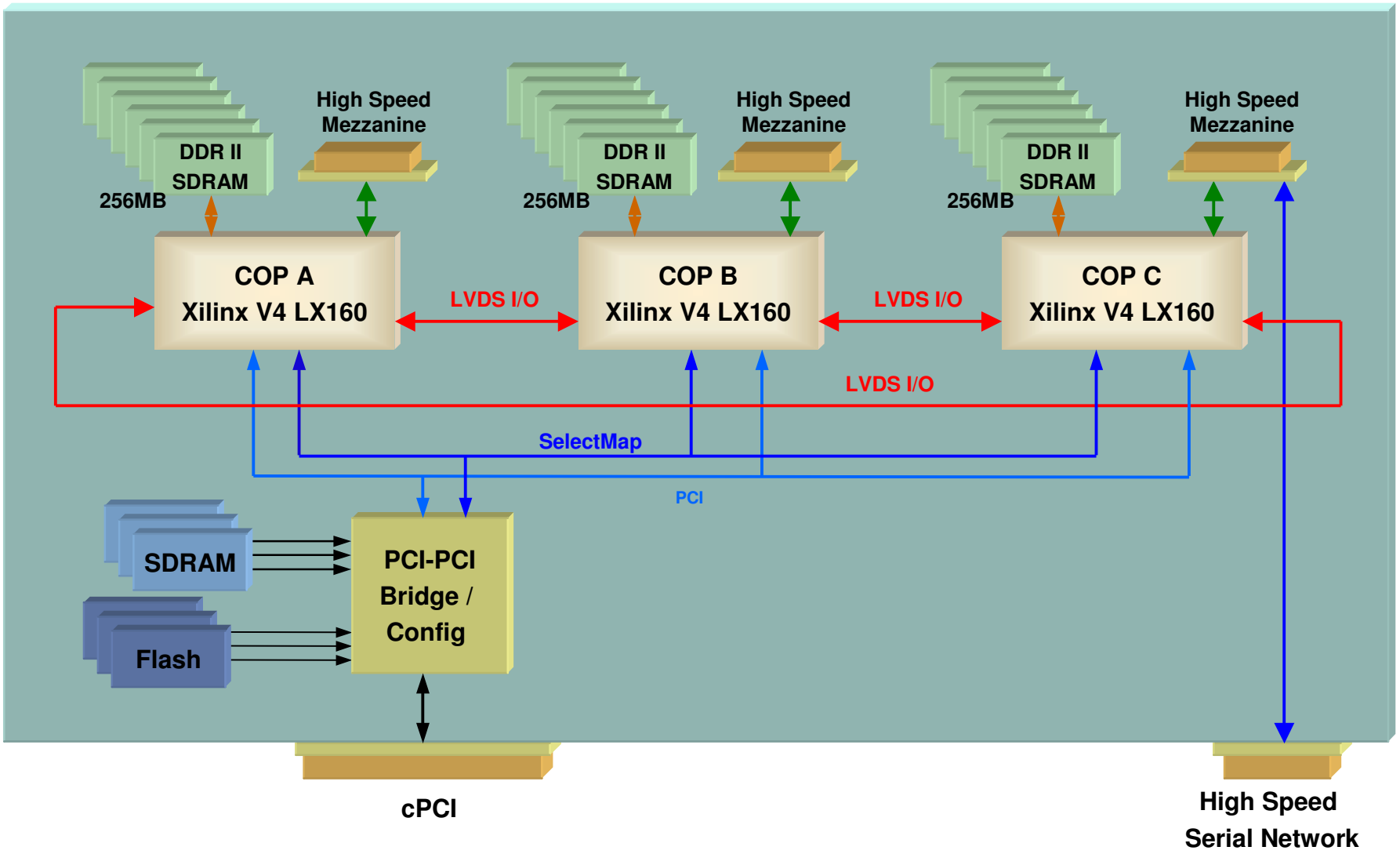

# RA-RCC Personality Mezzanine Card

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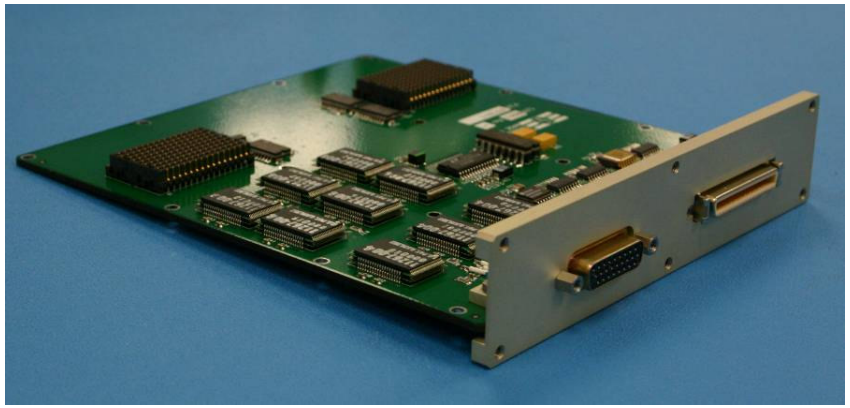
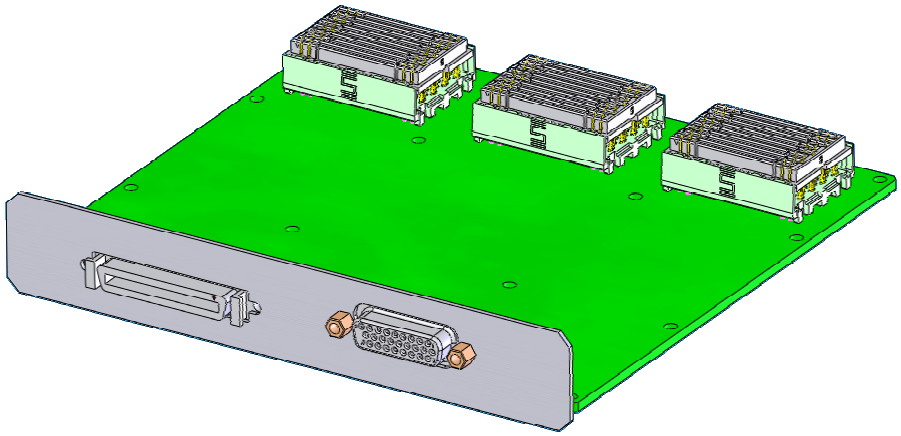
- **Personality Mezzanine for application specific functionality**
  - Lower risk, quick development, lower costs
  - I/O and unique I/O connectors
  - Memory
  - Logic
  - TMR mitigation hardware
  - Analog circuitry ADC/DAC
- **High speed mezzanine connectors**
  - 170 high speed I/O
    - LVDS
    - High speed serial
    - TMR'd signals
  - Symmetrical Design to all Xilinx FPGAs
- **ARTEMIS Personality Mezzanine**
  - 16 GBytes of flash memory
    - EDAC protected
    - 800 Mbps aggregate datarate
  - Two high speed camera link ports
  - Analog control and telemetry
- **Size: 6.1 x 6.88 inches**



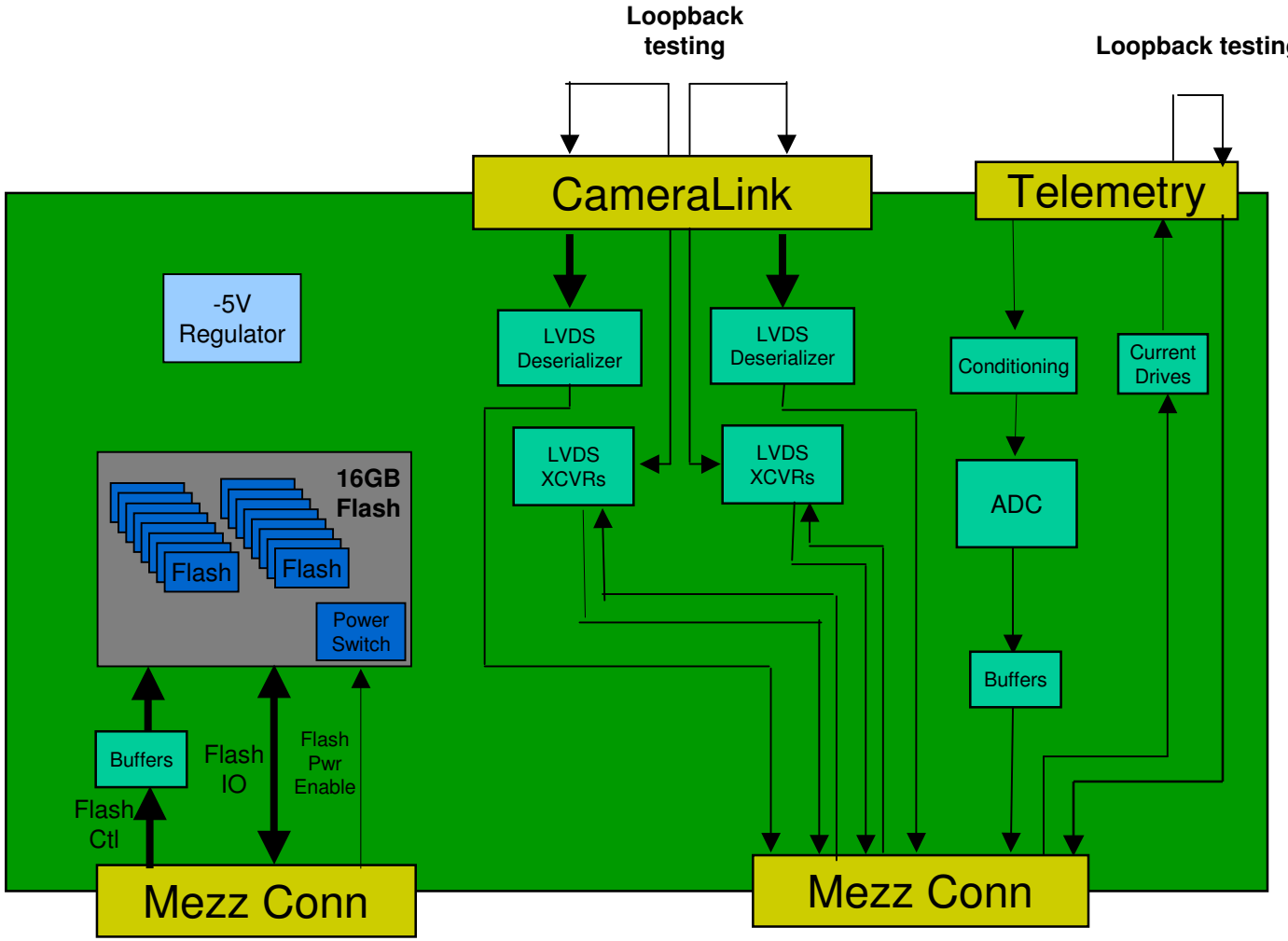
**ARTEMIS Mezzanine**



# ARTEMIS Personality Mezzanine

SEAKR Engineering, Inc.

*Aerospace Data Storage and Processing Systems*



# SEE Mitigation
# One Size Does Not Fit All

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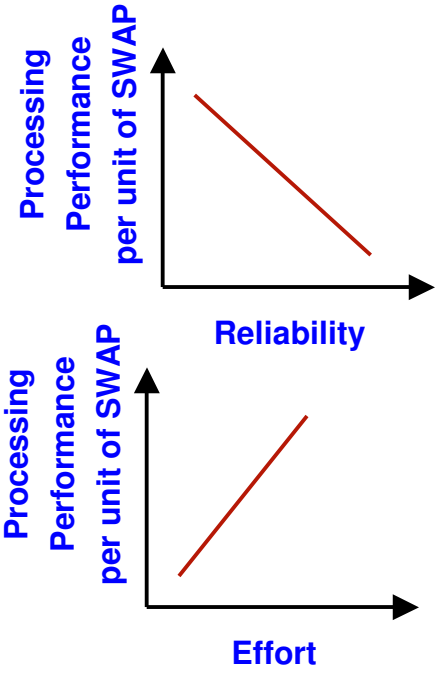
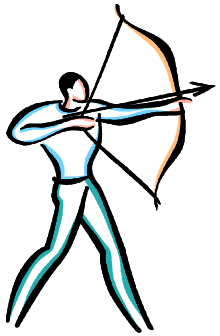
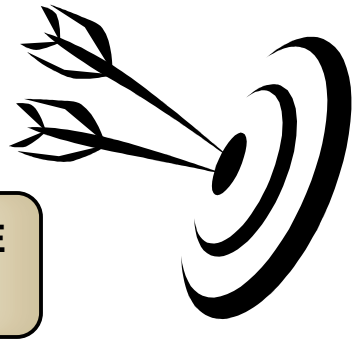
- Neither does one SEE mitigation method…
- Mitigation methods are VERY application dependant.
  - SWAP constraints
  - Processing performance
  - Reliability requirements
  - Design schedule
  - Type of data and peripherals
  - Latency constraints
- Factors need to be weighed before an approach can be implemented.
- Optimum designs may use a quiver of mitigation methods
  - Combination of HW and SW



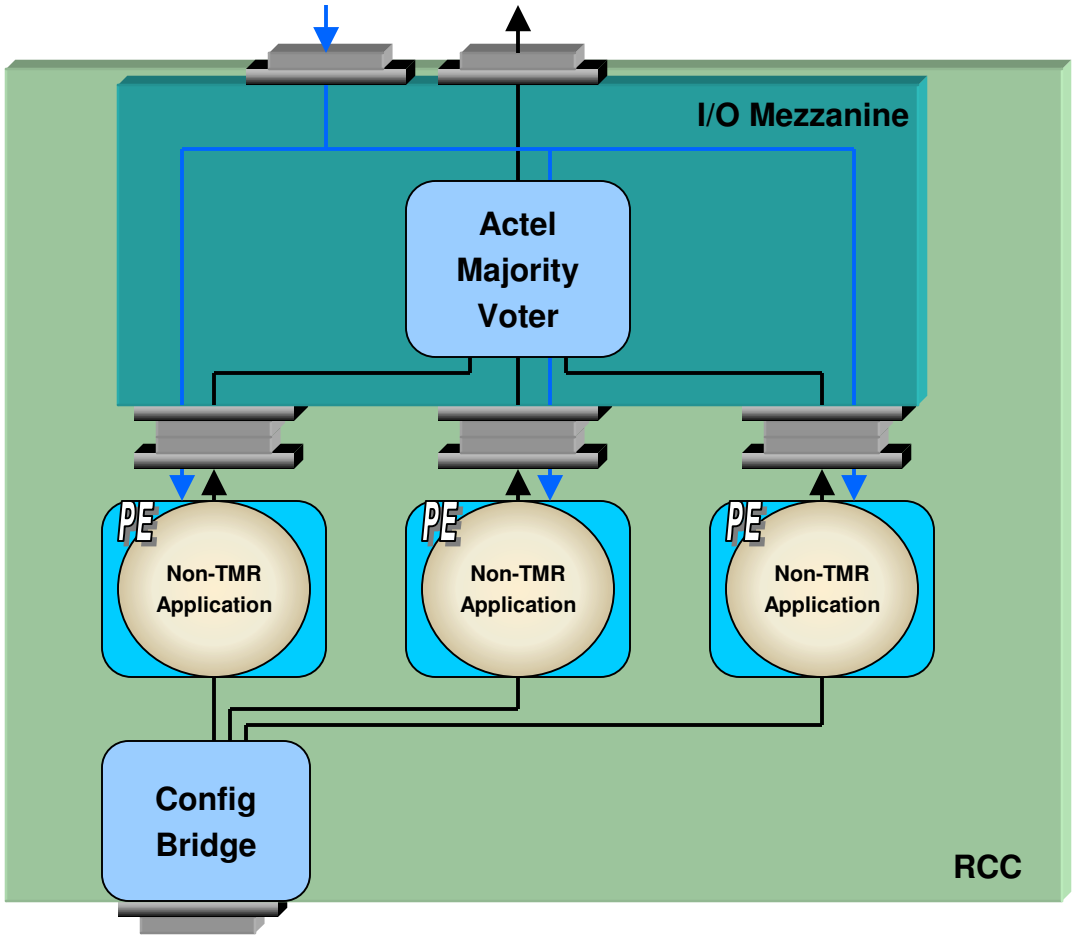


**V4-RCC Supports Wide Range of SEE Mitigation Approaches**

# SEE Mitigation, External TMR



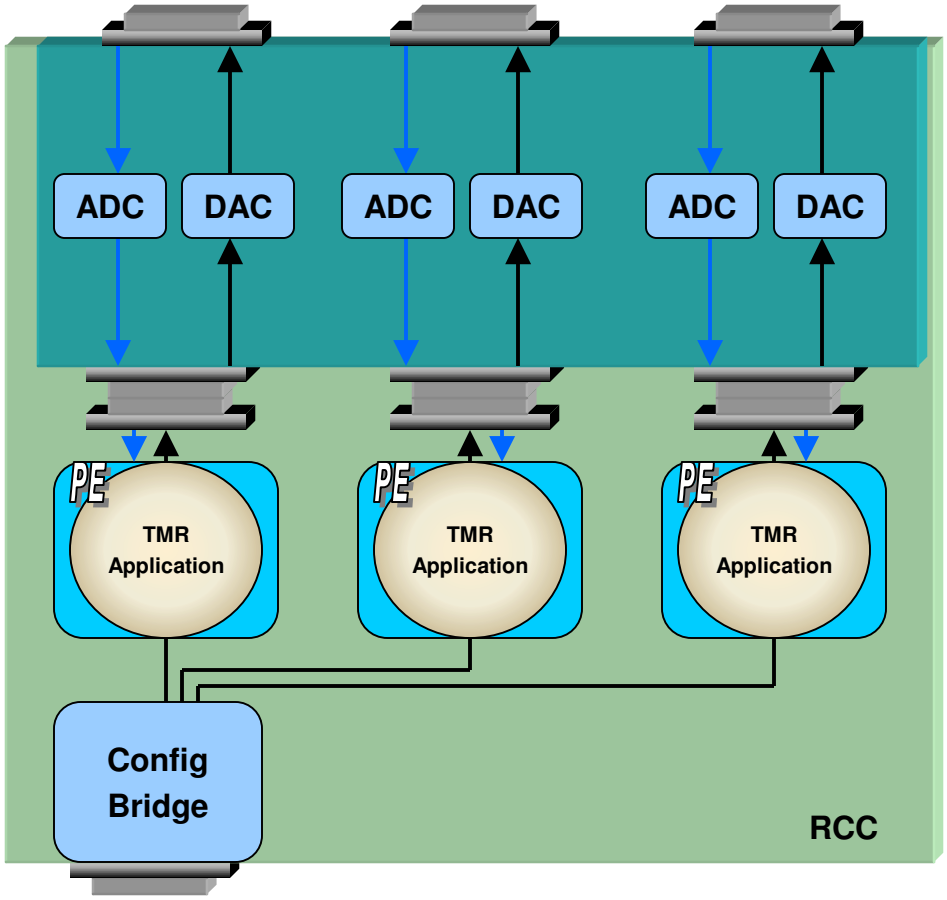
- **Pros:**
  - SEFI Immune
  - SEU Immune (or very low)
  - "Brute force" approach, easy to implement at the FPGA level
  - Protection for all internal resources (macos, dcms, I/O)
- **Cons:**
  - Requires external device for majority voting
  - Large SWAP increase
  - Requires design mods to eliminate persistence and provide resynchronization logic



# SEE Mitigation, Internal TMR Configuration



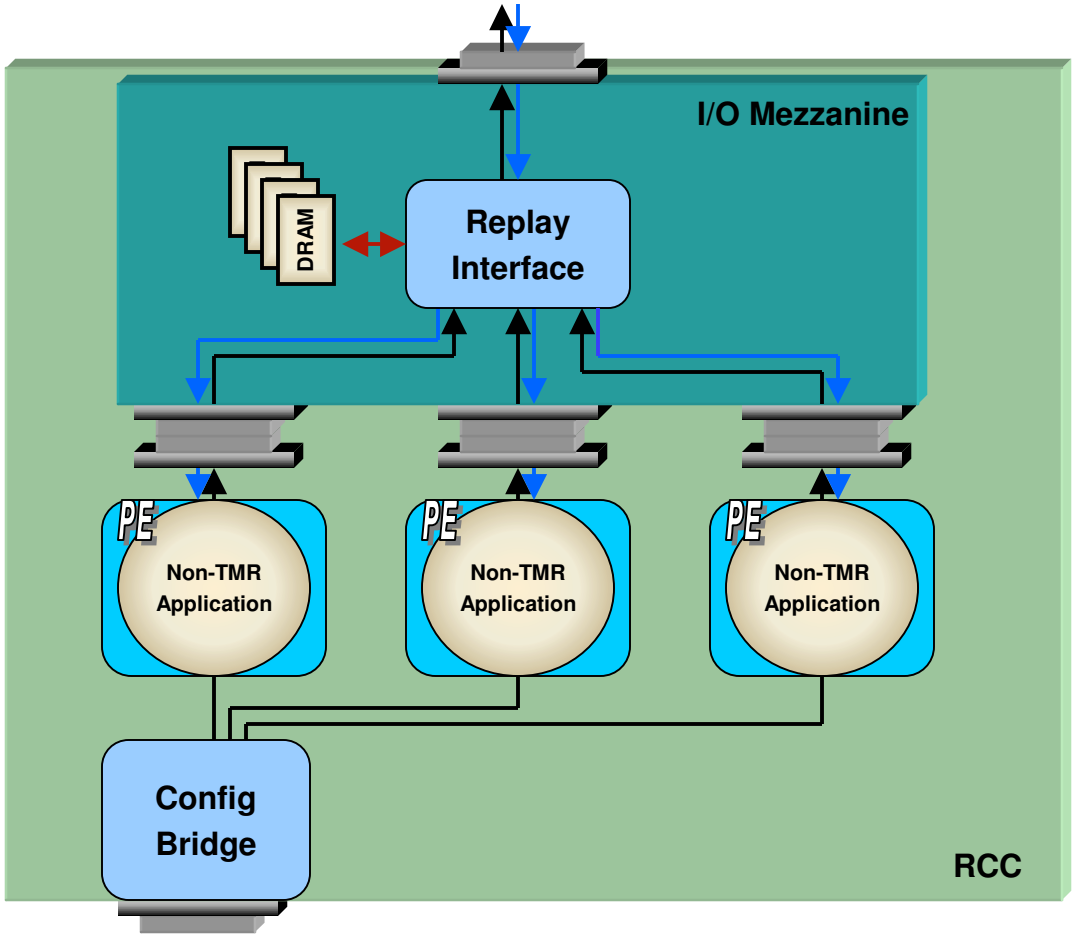
- **Pros:**
  - Fault tolerant design can be implemented in a single FPGA
    - Reduce system SWAP
- **Cons:**
  - Difficult to implement
  - Design grows 3.4 to 6x
  - Speed decrease 5% to 20%
  - Power increase > 3x
  - Difficult/impossible to TMR some embedded elements (PPC 405, SERDES)
  - Not immune to SEFI's
  - Has susceptible cross-section
  - MBUs may break internal TMR



# SEE Mitigation, Replay



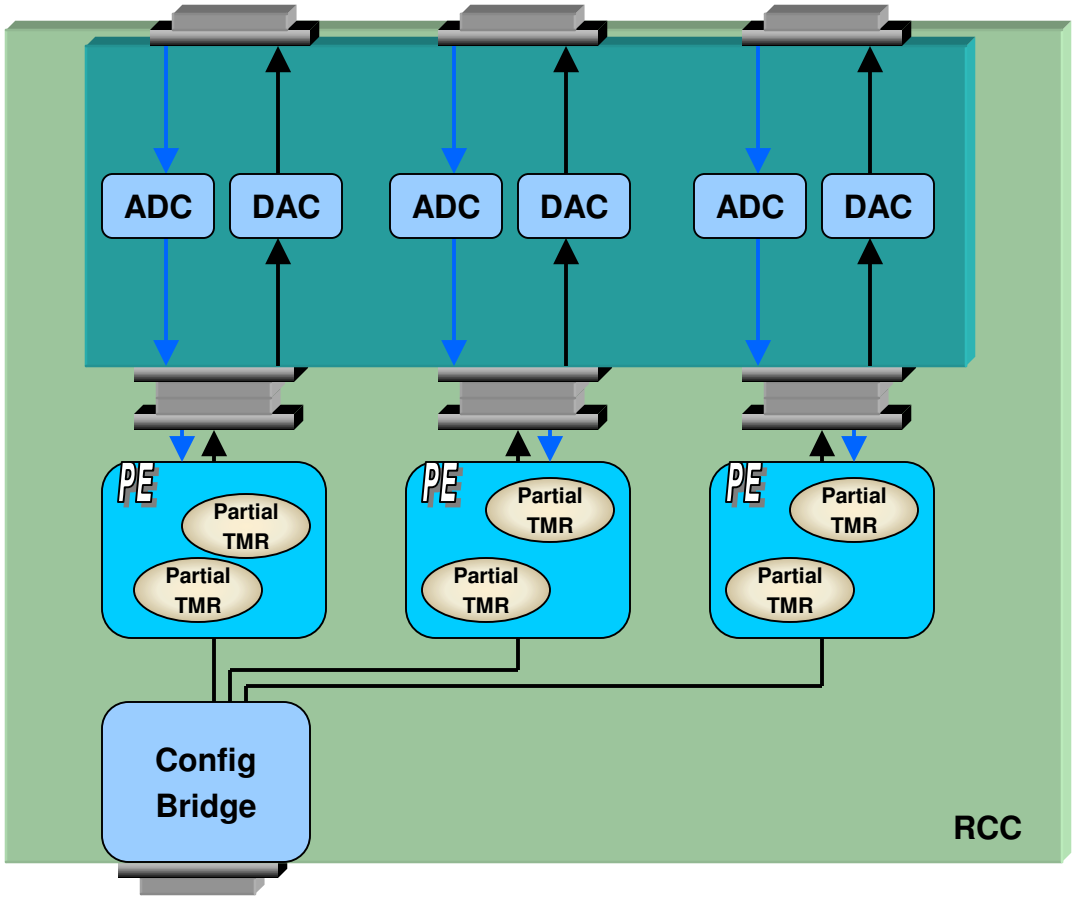
- Little to no TMR
- Increased performance
- Very Small SEU cross-section
- SEFI immune
- Use commercial development tools
  - System gen, Celoxica, Simulink, commercial cores…
- Network interfaces to front panel or backplane
- SEAKR Patent #7263631



# SEE Mitigation, Partial TMR



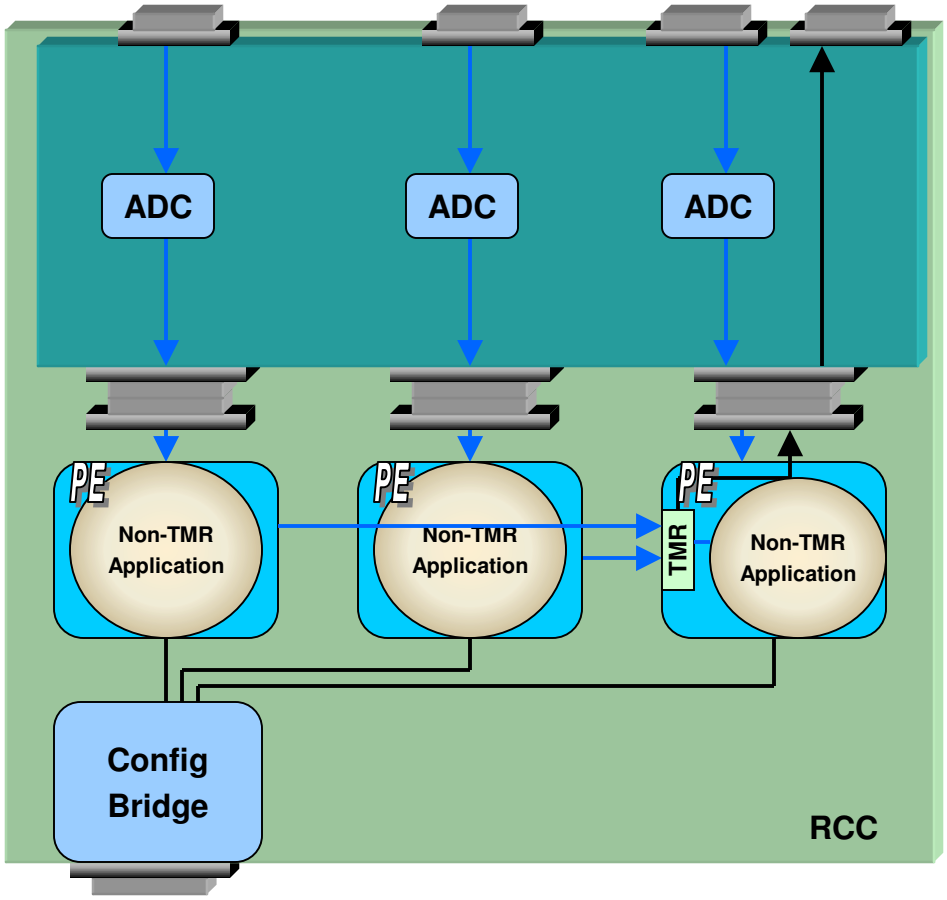
- Use selective TMR to remove persistence
- Data comes in through PCI or Mezzanine
- High processing performance
- Use commercial development tools
  - System gen, Celoxica, Simulink, commercial cores…
  - Designs require modification to remove persistence



# SEE Mitigation, Hybrid TMR Configuration



- Non-TMR applications in all three FPGAs
- Third FPGA has a TMR'd Voter and TMR output
- Very small SEU cross-section



# Conclusions



- An Application Independent Processor for space has been developed using Xilinx Virtex 4 FPGAs and PowerPC processor
- The platform enables the rapid development and deployment of missions requiring high performance on-board processing.
- Core technologies developed include
  - SEE mitigation
  - Point of Load supplies
  - Thermal and structural management
  - IP cores
  - User interface GUI
  - Package qualification testing
- The application independence has been demonstrated by porting a build to print processor to multiple space applications
  - Hyperspectral Image Processor
  - Software defined radio
  - MODEMS with programmable waveforms
  - Real time image compression
  - Real time EO processing

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# Questions?

*Military and Aerospace FPGA and Applications (MAFA) Meeting*
*Palm Beach, FL*
*November 27-29, 2007*