A 650Mb/s (8158,7136) Low-Density Parity-Check Decoder Utilizing a Virtex 4 LX200 FPGA

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Coding Basics

- Channel code
  - Set of binary vectors - c
  - Easily distinguished in presence of noise
- $c = uG$
  - u is the k-bit message
  - G is an k x n generator matrix
- $cH^T = 0$
  - H is the (n-k) x n parity check matrix

Low Density Parity Check Codes

- Linear Block Code
- Gallager (1962)
- Approaches the Shannon Limit
  - Closer for long code lengths
  - Closer for higher iteration count
- Complexity
  - Transistor count
  - Interconnect

LDPC Code Basics

- Parity check matrix H
  - Low density of 1's
  - Decoding properties
- Generator matrix
  - Derived after determining H
    - Gauss-Jordan reductions
    - Structure
      - Cyclic
      - Quasi-cyclic

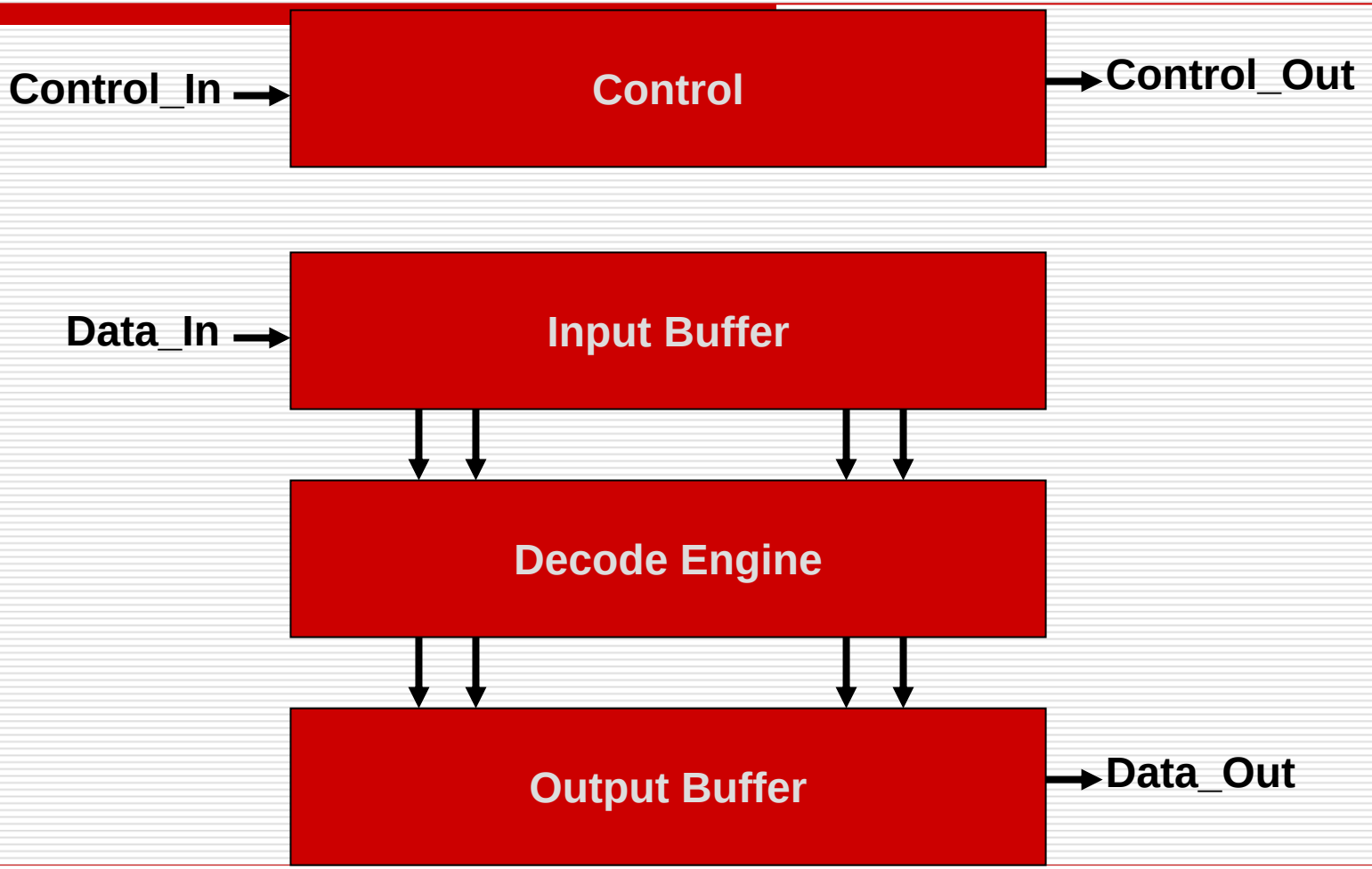
Code Specifications

- Quasi-Cyclic (8176,7154)
- Shortened for easy interface
  - (8158,7136)

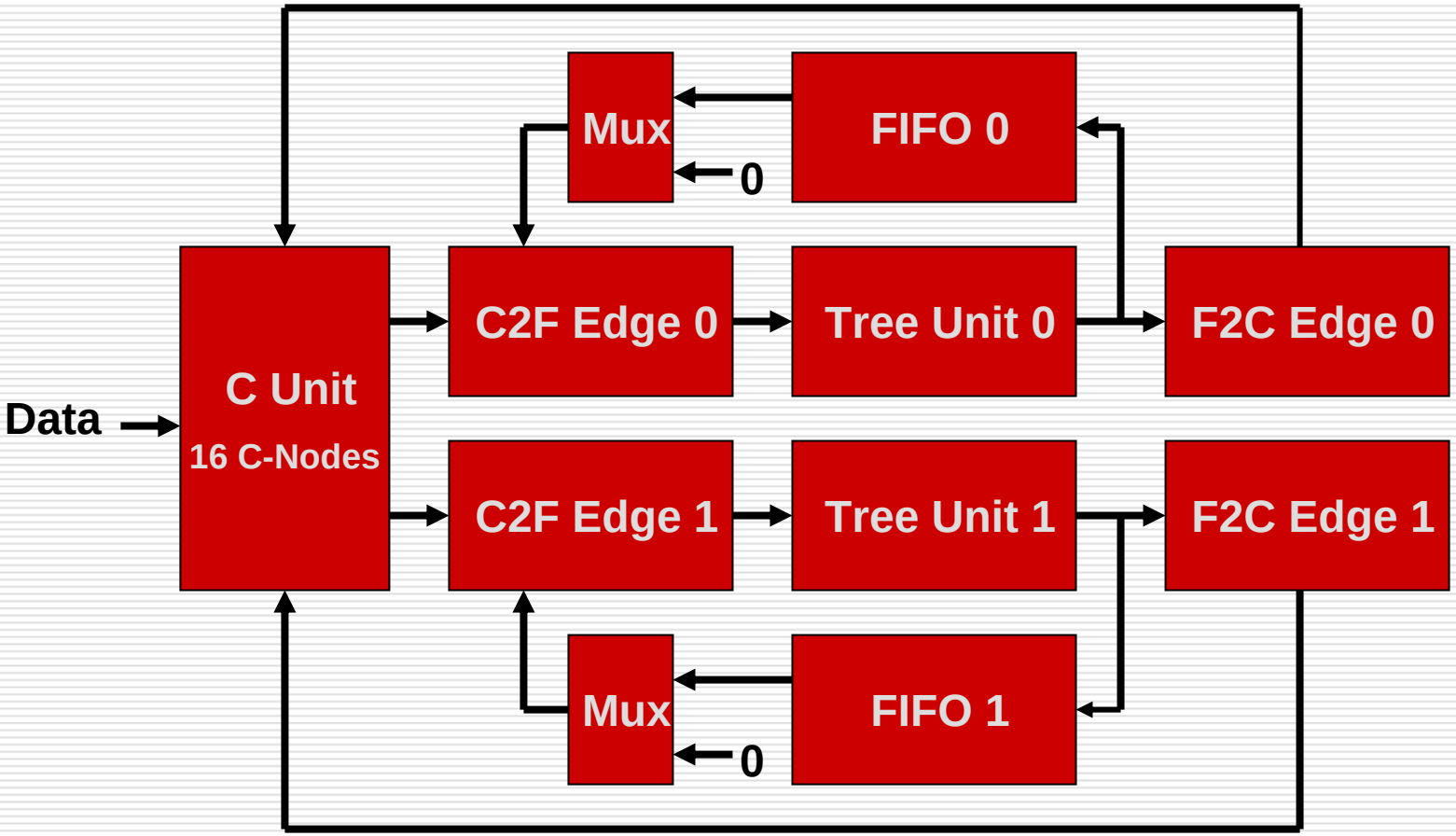
H-matrix

$$H = \begin{vmatrix} C_{1,1}\ C_{1,2}\ C_{1,3} \ldots C_{1,14}\ C_{1,15}\ C_{1,16} \\ C_{2,1}\ C_{2,2}\ C_{2,3} \ldots C_{2,14}\ C_{2,15}\ C_{2,16} \end{vmatrix}$$

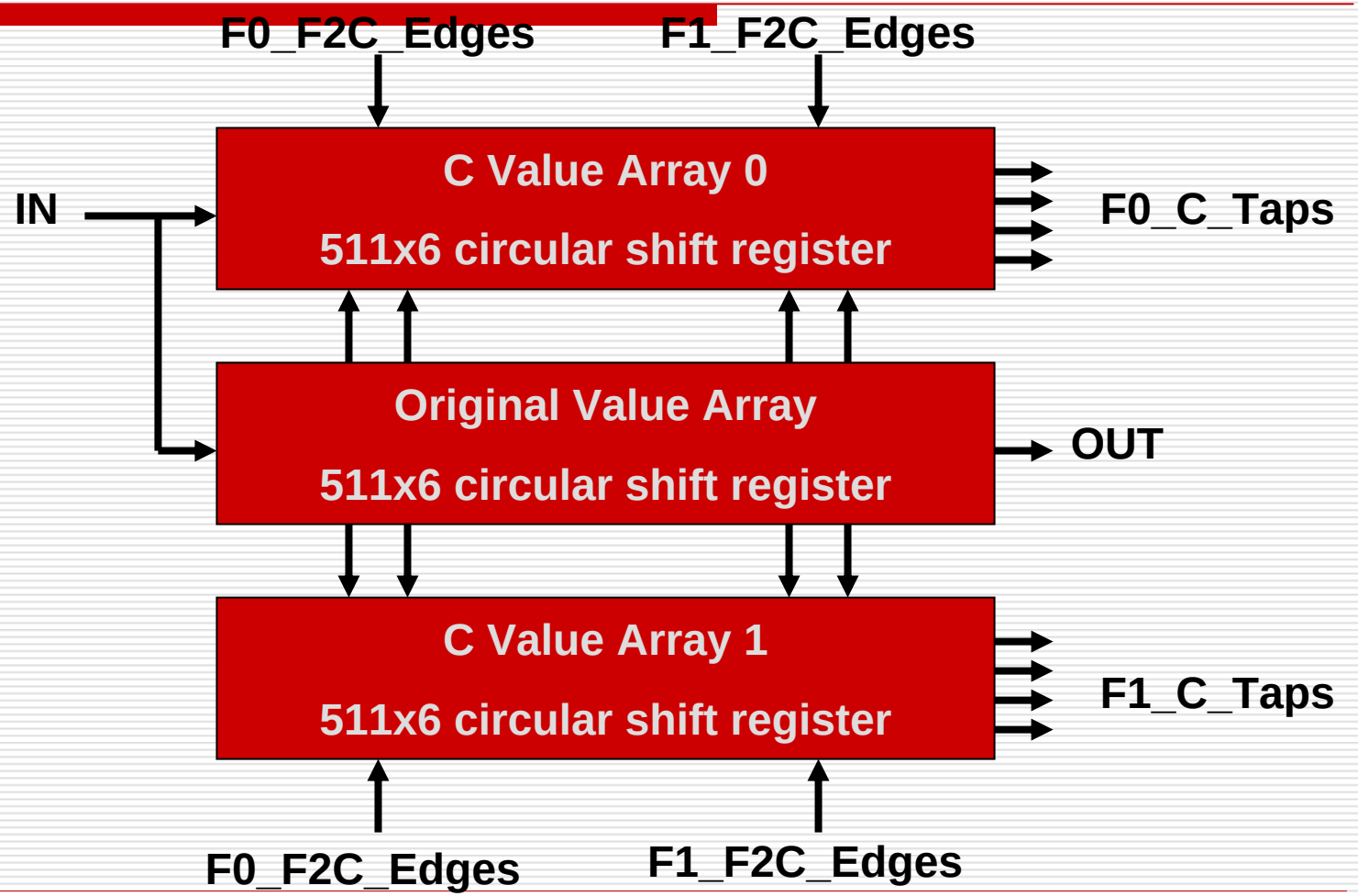
Decoder Block Diagram



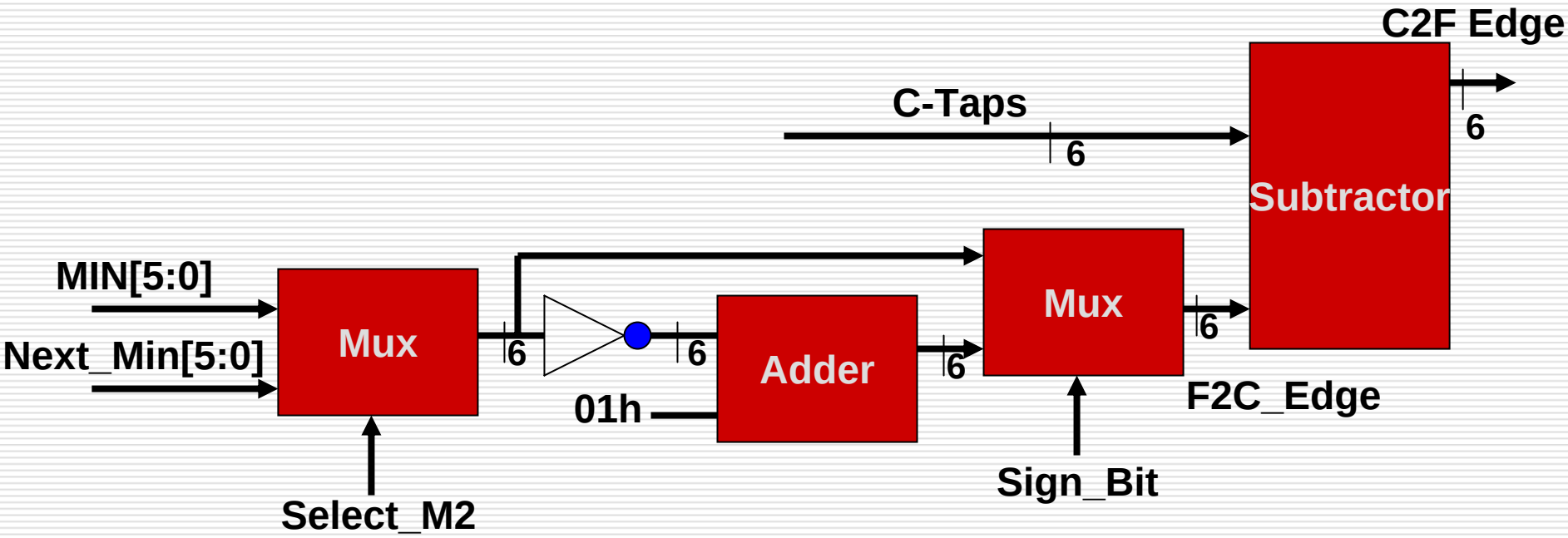
Decode Engine Block Diagram



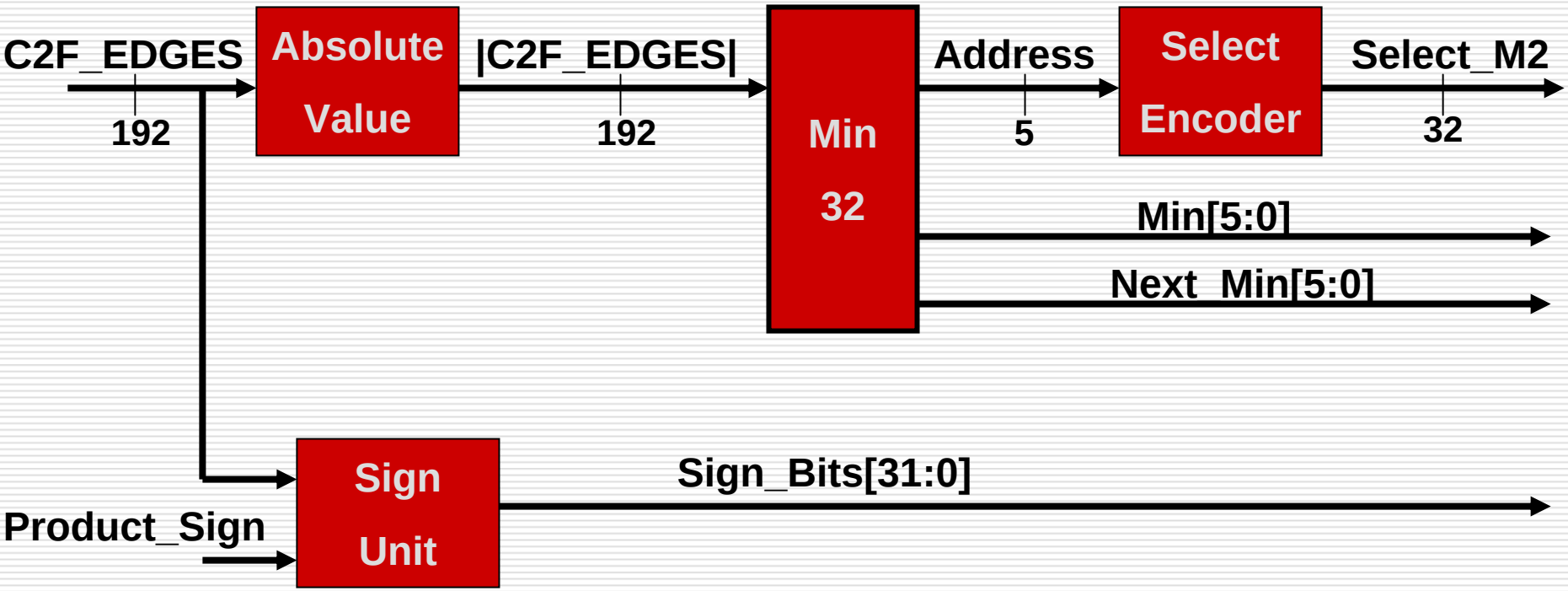
C-Node Block Diagram



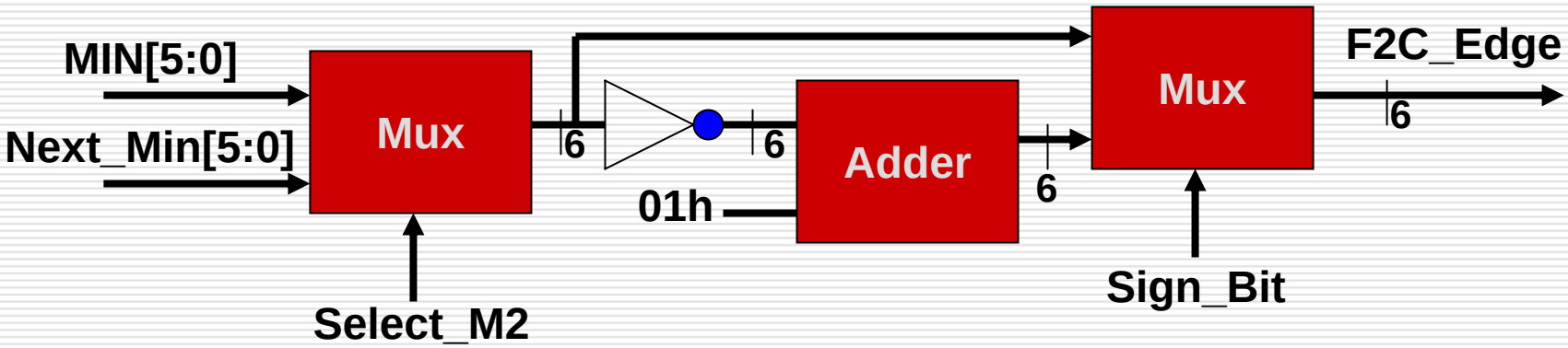
C2F Edge Block Diagram



Tree Unit Block Diagram



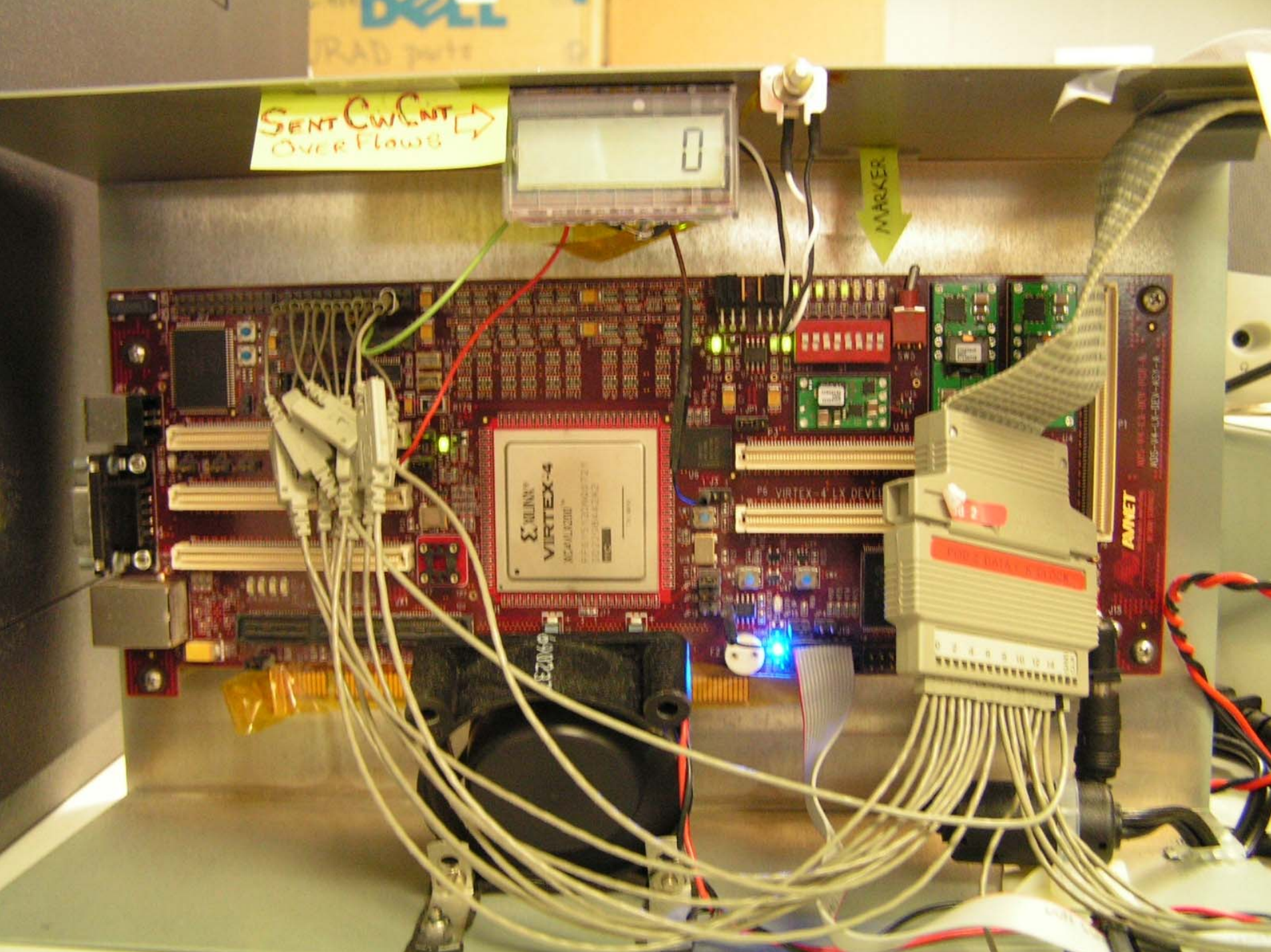
F2C Edge Block Diagram



GSFC LDPC Decoder Test Setup

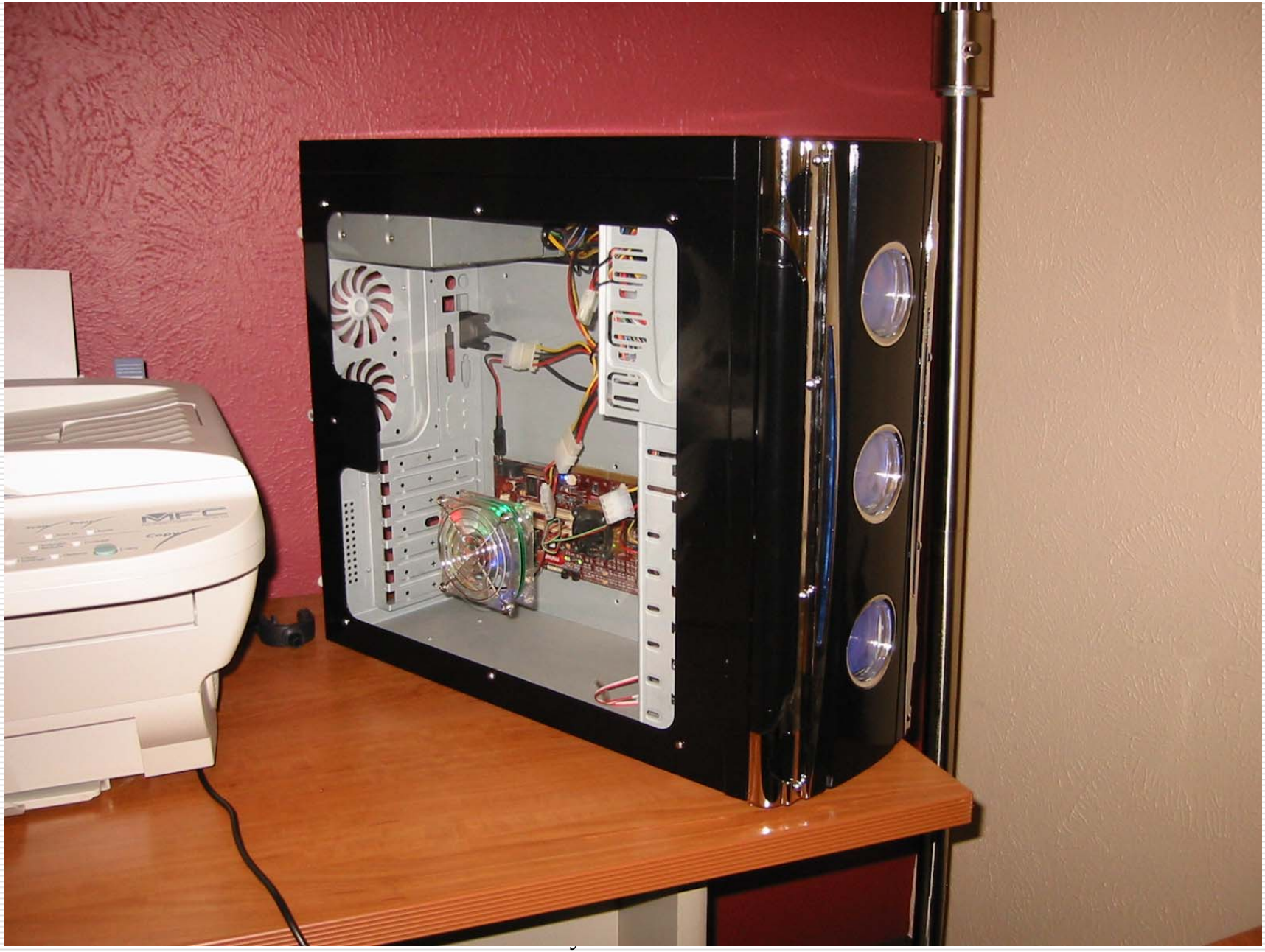
- Various signal to noise
  - Functional testing
- Long duration 4.4dB Eb/No
  - 8.84 $x10^{-15}$ BER
  - $1.18x10^{-11}$ FER
  - 15 iterations
    - No erroneous decodes yet detected


CAUTION
TEST IN PROGRESS
DO NOT DISTURB


SENT CW CNT
OVERFLOW
0
MARKER
XILINX
VIRTEX-4
AMCC

CAMBR LDPC Decoder Test

- Same FPGA board used
- Random nonzero code words
  - Functional verification
- High Noise tests
  - Uncorrectable in 15 iterations
  - CRC to verify functionality versus software



GSFC System Test

- System test
  - LDPC encoder
    - CAMBR custom chip
  - High Rate Baseband Modulator
    - CAMBR semicustom chip
  - Demodulator
  - LDPC decoder
    - CAMBR FPGA

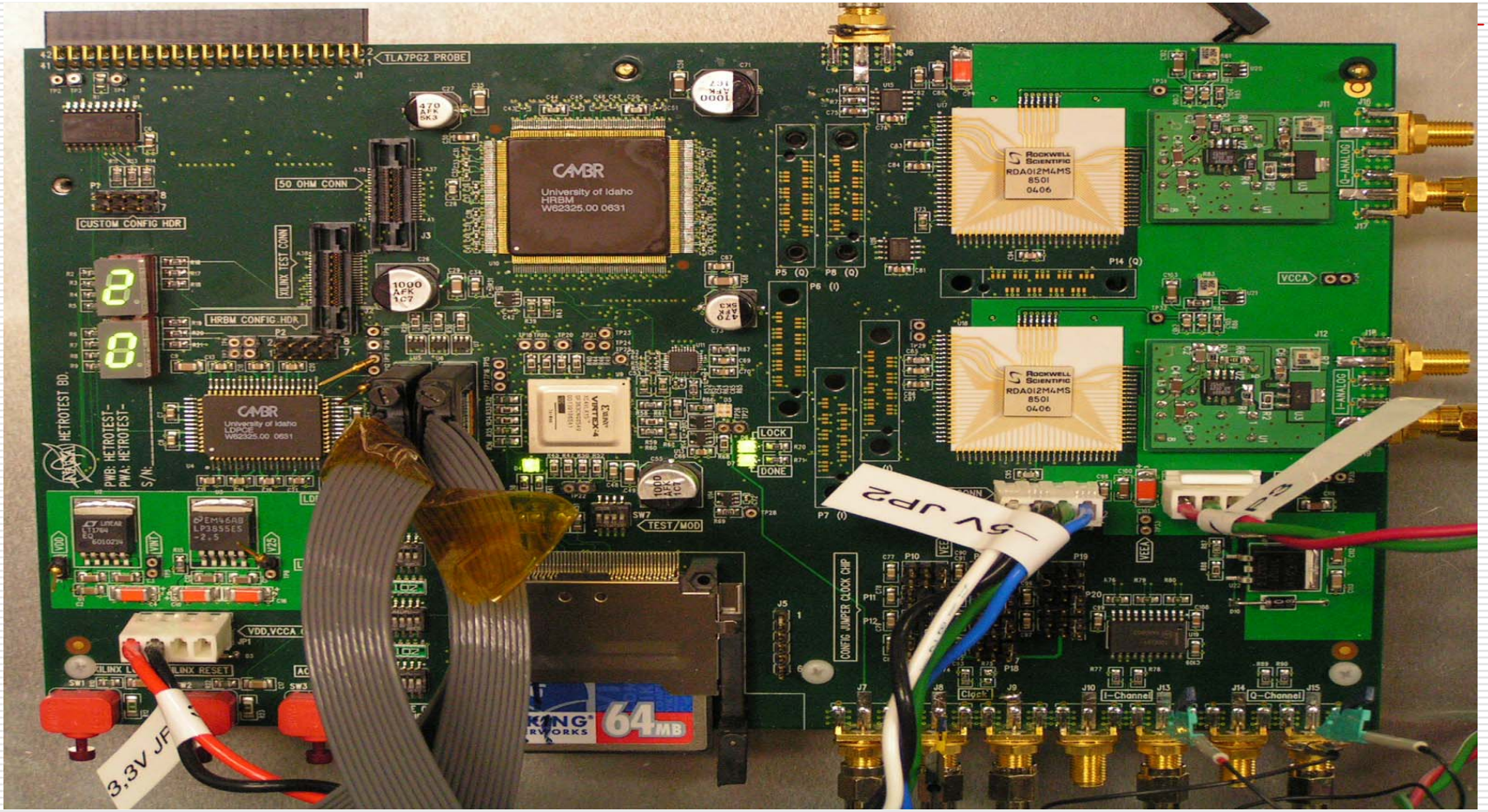
Data

Signal Transform

Data Compression

LDPC Encoder

Modulation



Demodulation

LDPC Decoder


ATTENTION
ELECTROSTATIC
SENSITIVE AREA
DO NOT

Summary

- Motivation for FPGA
  - FPGA > 200 Gig arithmetic ops/second
  - Parallel operation
  - CPU comparison
    - Assuming CPU does 8 G/ops then 25X
- Advantages & Disadvantages w/FPGA
  - Advantage: Easy to change functionality
  - Disadvantage: Limited routing & Logic
- Design
  - HDL: System Verilog to VHDL
  - About a year to decode core including random number generator
  - Longer for testing, front/backend interface

Summary Part II

- LDPC vs other ECC
  - Better performance than Reed Solomon for random errors
  - Better SNR than non soft error ECC's
- Implementation limitations
  - Interconnect routing
  - Number of FF's
  - Algorithm chosen to minimize both above
  - Initial synthesis step concluded insufficient number of FFs
  - Due to architecture, mapping phase resolved issues