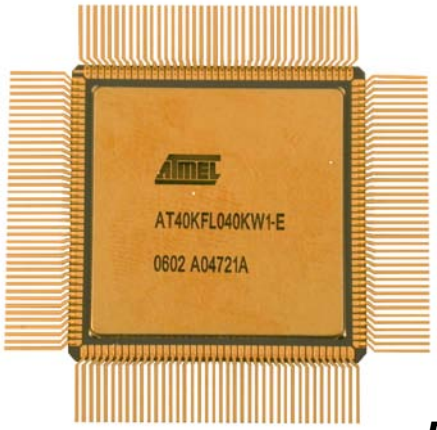
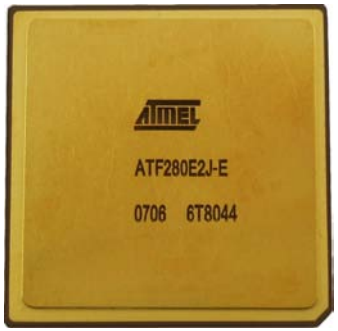
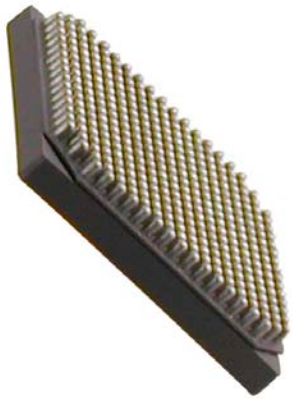
SRAM BASED REPROGRAMMABLE FPGAs FOR SPACE







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Overview

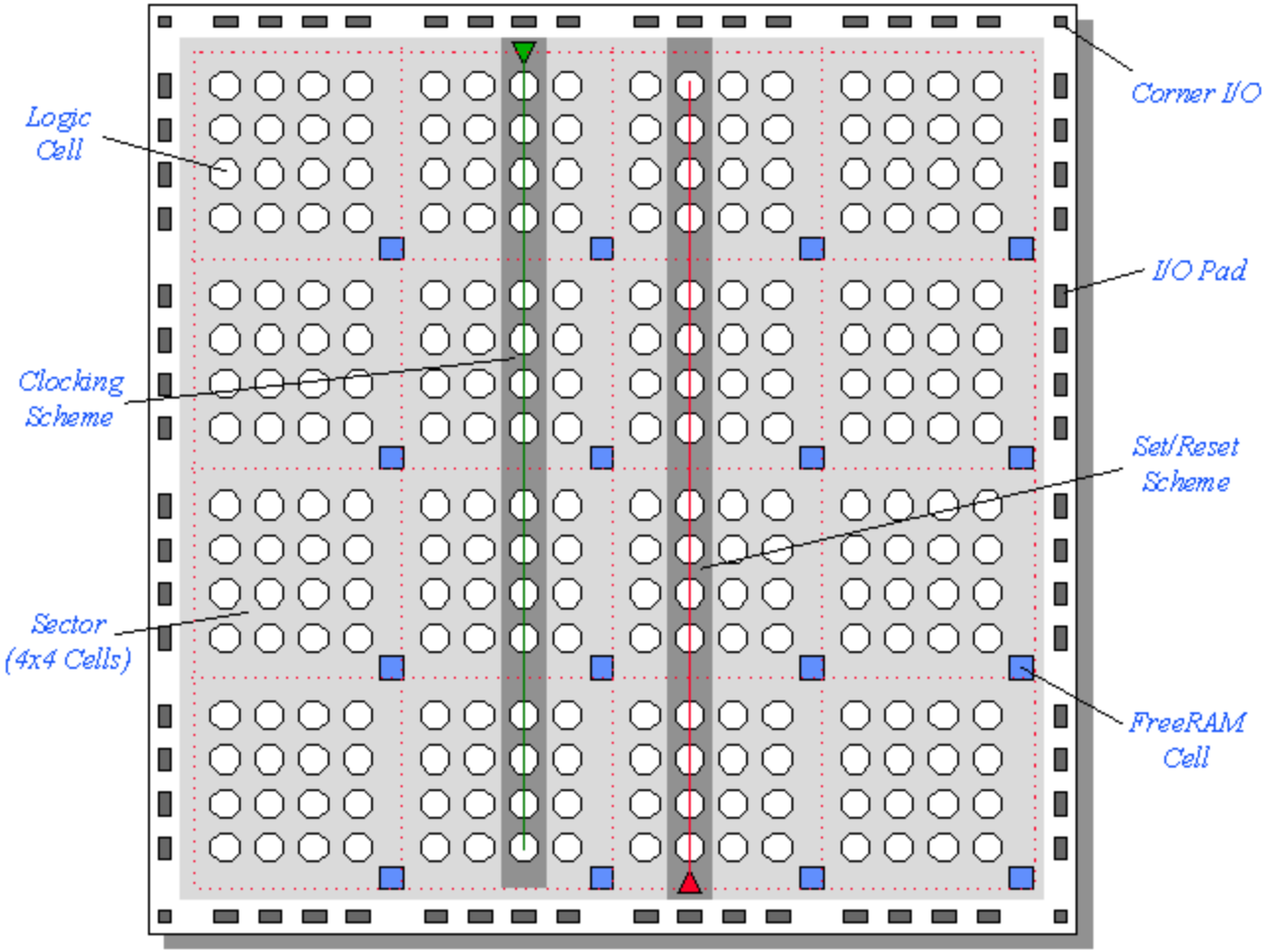
- **Atmel FPGA Key Points and Architecture**
- **ATF280E FPGA**
- **Configuration memory AT69170**
- **Tools (software and hardware)**
- **Roadmap**

ATF280E and AT69170 Developments are supported by ESA & CNES

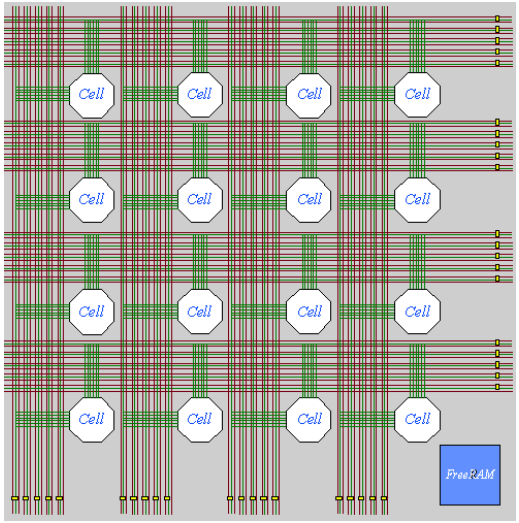
Atmel Radiation Hardened FPGAs

- **Re-programmable (SRAM based technology)**
  - **Reliability**
  - **Unlimited reprogramming**
  - **Easy to debug**
  - **Engineering models representative of flight models**
- **SEU hardened Memory points**
  - **Core cell Flip-Flops, embedded memory (FreeRAM), configuration memory and controller**
  - **No need for SEU mitigation**
- **Complemented with rad-hard EEPROMs for FPGA configuration**
  - **1 Mbit serial**
  - **4 Mbit serial**
- **In-Flight reconfiguration**

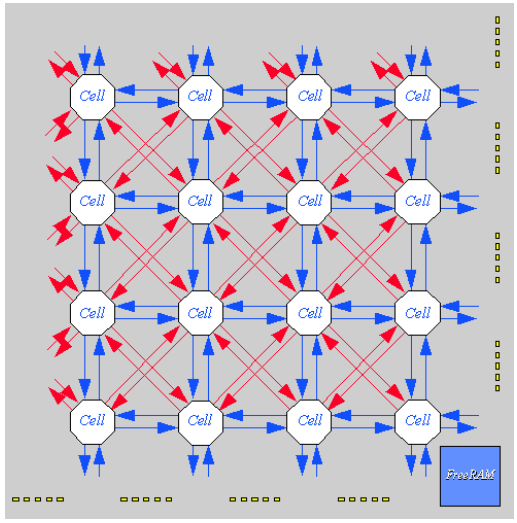
FPGA Architecture Overview



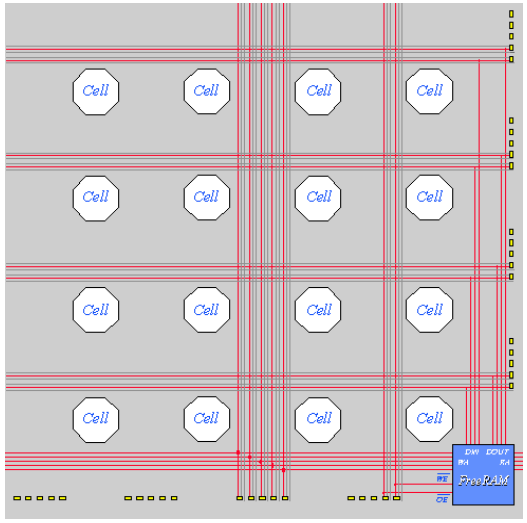
Efficient Routing Architecture



Cell to bus connection



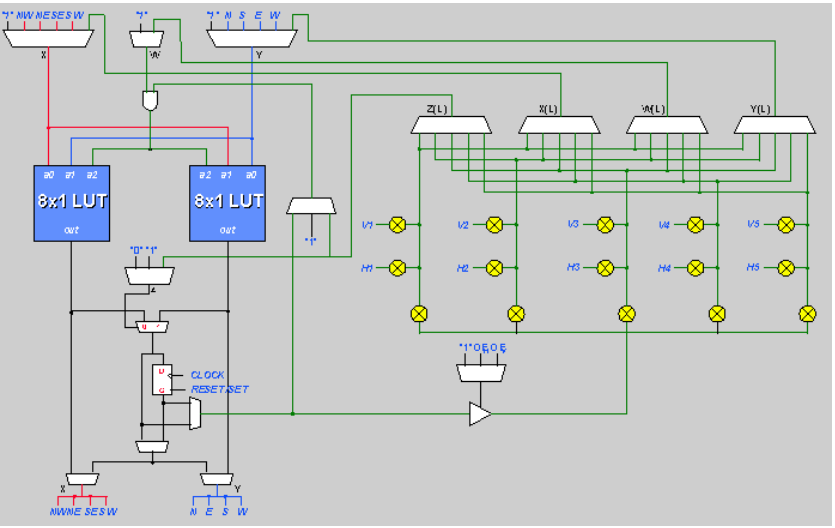
Cell to cell connection



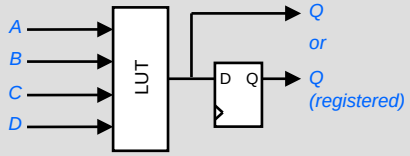
FreeRAM to bus connection

- **Efficient functions using almost only cell to cell connections**
- **FreeRAM uses very few global routing (address) and local (data) routing bus (free otherwise)**
- **Most of the routing structure is still available for global routing after blocks and RAM local routing**

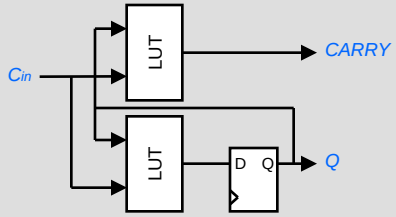
Core-Cell Modes



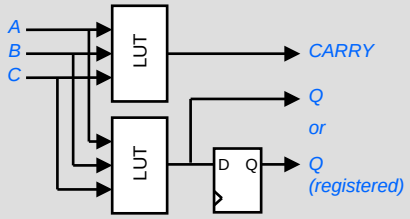
Synthesis mode



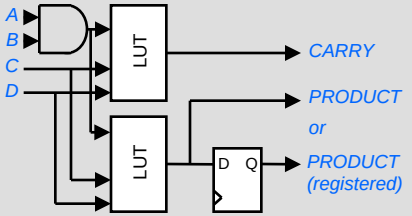
Counter mode



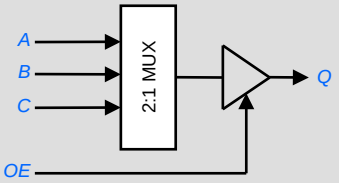
Arithmetic mode



DEP/Multiplier mode

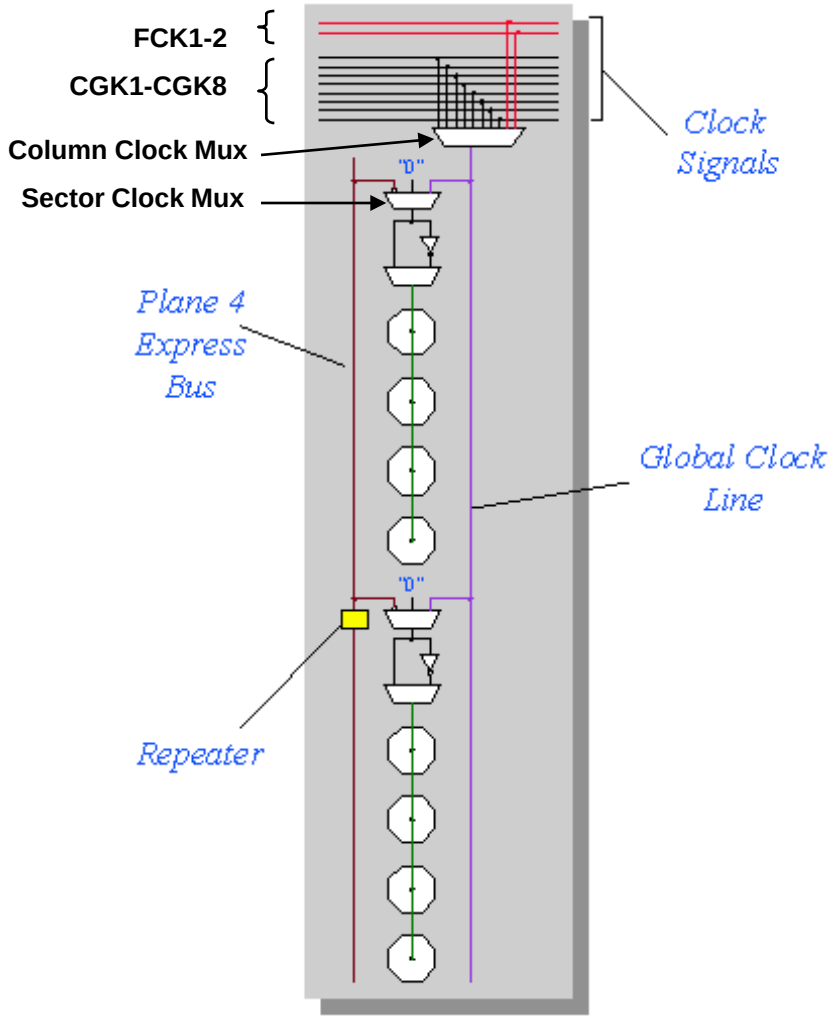


Tri-State/Mux mode



- **Efficient operators only use 1 core-cell / bit**
- **Fast multi-bit operators using cell to cell diagonal/orthogonal connections**
- **Pipelining (DFF) possible inside core-cell**

Global & Fast Clocking



8 Dedicated '<u>Global Clock buses</u>'

- Individual 'Global Clock' line feeds all the logic cells in one column
- GCK1 to GCK8
- Distributed across a special high-speed bus (top edge of the FPGA)
  - => FPGA distribution < 1 nS
- 'Global Clock Pad' connection
- Each column of the array has a Column Clock selected from one of the 8 'Global Clock' buses

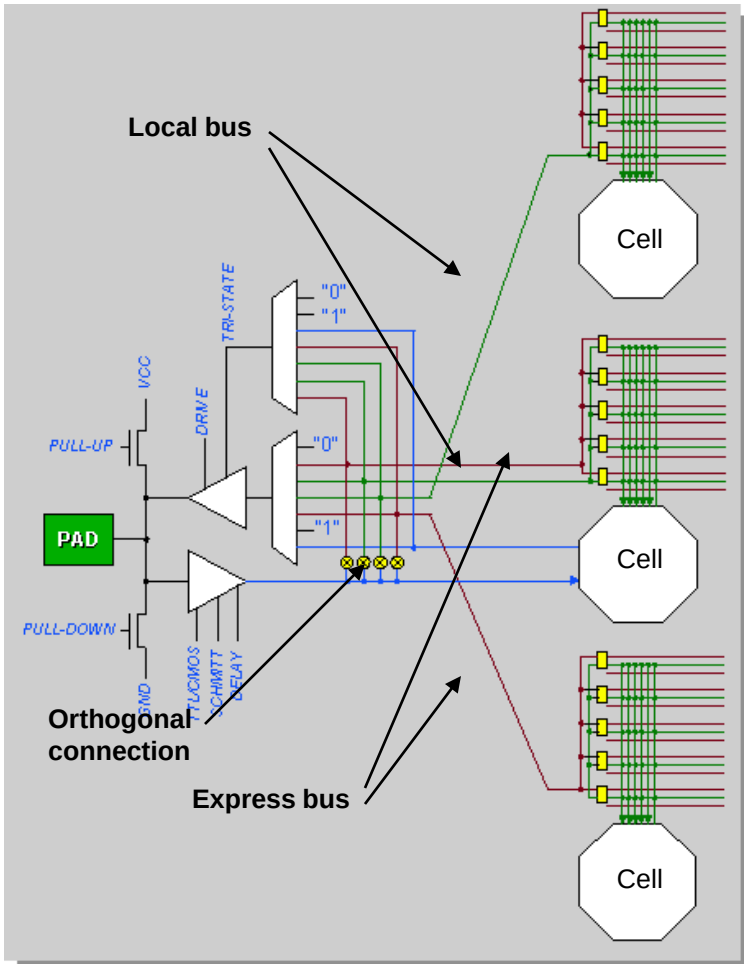
4 Additional '<u>Fast Clock buses</u>'

- Only for the right/left most columns of the array
- FCK1-2 to left-side I/O
- FCK3-4 to right-side I/O

Each sector column can be clocked by

- Plane 4 'Express bus'
- Global Clock column

Primary I/O



Located next to a core cell

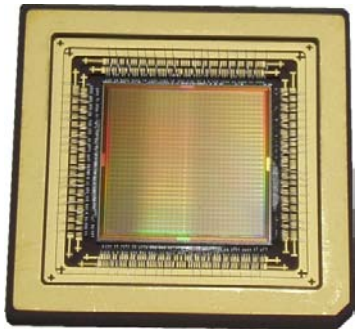
Interfaces directly to its adjacent core cell:

- **Adjacent orthogonal connections**

I/O connects the bussing network of the 3 nearest edge cells (repeaters):

- **Above local bus**
- **Adjacent local bus**
- **Below Express bus**

ATF280E Key Features



- 288K equivalent ASIC gates
- 50 MHz clock speed
- 14400 core-cells (each 2 LUT + 1 DFF)
- 115 Kbit FreeRAM (900 modules of 32x4 blocks)
- 1.8V Core / 1.8V and 3.3V Cold-sparing I/Os
- Dedicated 1.8V LVDS buffers: 8 pairs Rx + 8 pairs Tx
- 3.3V PCI-compliant I/Os

- ATC18KRHA 0.18um CMOS technology (same as ATC18RHA ASIC and AT697F LEON2 processor)
- MCGA472 (308 + 32 User I/O) / MQFP256 (148 + 32 User I/O)

- Configuration load integrity check
- Configuration self-integrity check
- Boundary scan interface

ATF280E Radiation Hardening

- **Process & library hardening**
  - **EPI substrate (low resistivity, low thickness)**
  - **Thin oxide**
  - **Density of body ties to delay parasitic transistor switch on**
  - **Spacing of body/well ties to active area**
  - **Increase N+/P+ spacing**
  - **Add charge collection diodes**
  - **Drain minimization (cross section minimization)**
  - **Isolation transistors with NP isolation resistors**
  - **Detection of most SEE sensitive nodes**

ATF280E Radiation Hardening

- **Memories, configuration bits**
  - **Bit separation (external EDAC)**
  - **Duplication**
  - **Dual Mode Redundancy**
    - **Bit Duplication**
    - **Self-regeneration logic**
    - **Differential write mechanism**

ATF280E Radiation Hardening

- **Design hardening**
  - **Redundant nodes separation by**
    - **Spacing**
    - **Guard ring**
  - **Isolation between N and P redundant paths**
  - **Delay**
  - **TMR with majority vote**
  - **TMR + delay**
  - **Differential signals**
  - **Single node simulation by current injection (LET evaluation)**
  - *Multiple node simulation needs 3-D simulator*

ATF280E Radiation Performances
(preliminary data)

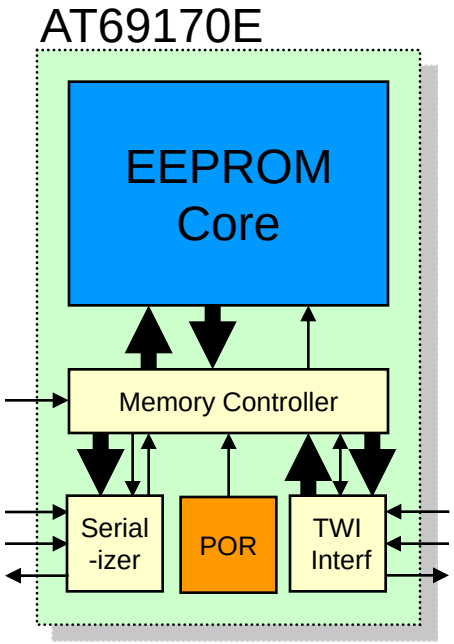
- **0.18um technology (same as ATC18RHA ASIC)**
- **Radiation test results on ATF280E**
  - **TID up to 300 Krad**
  - **No SEL up to 80MeV.cm²/mg @ 125°C**
- **SEU Performances**
  - **no SEU up to LET 30MeVxcm²/mg**
- **To be continued**
  - **FreeRAM**
  - **EDAC**
- **Final report end of the year**

AT69170E Key Features

- 4 Mbit Rad Hard EEPROM
- 512 bytes Pages

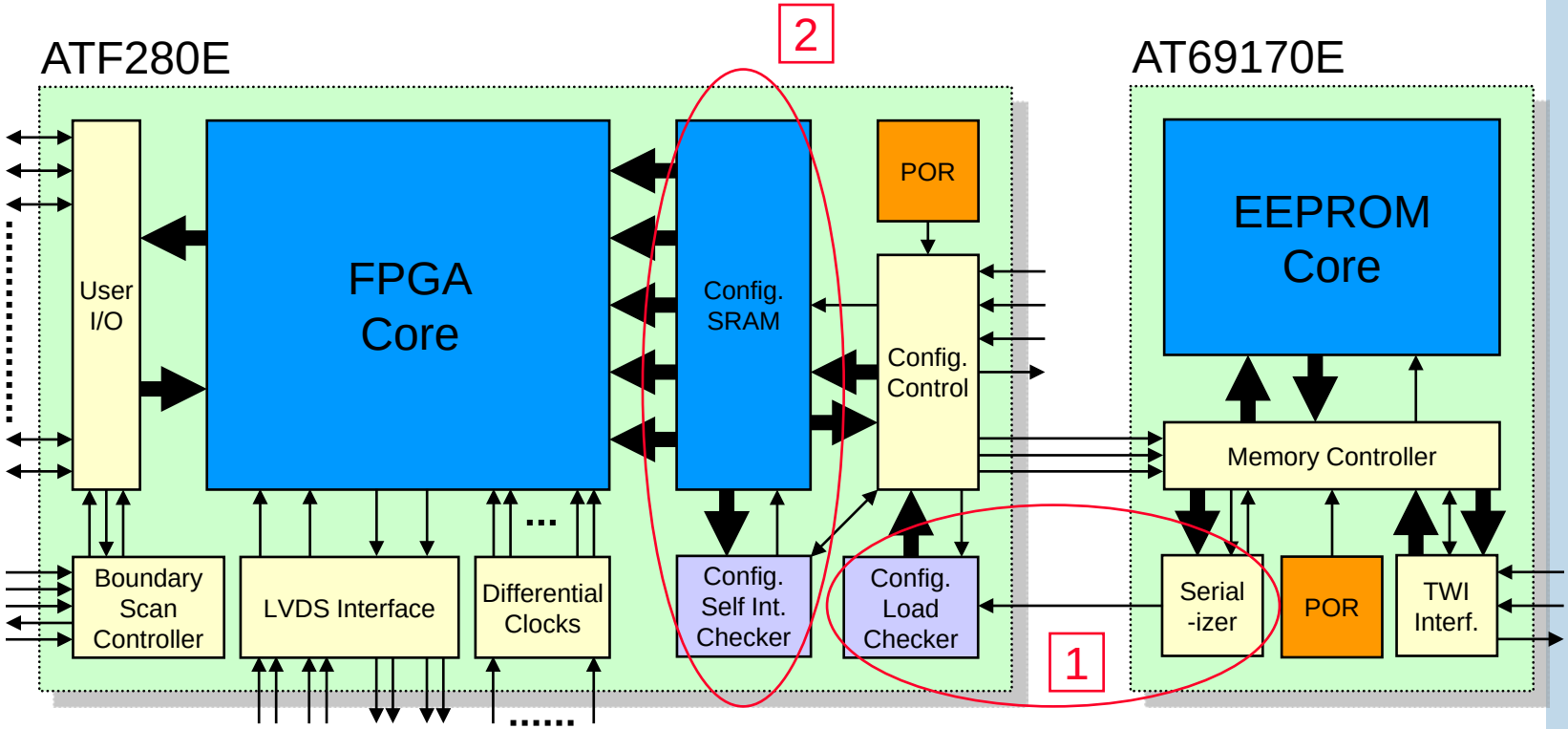
- Standard TWI programming interface
- FPGA serial configuration interface

- 3.3V Supply Voltage
- FP18 Package



- Endurance: 10K R/W cycles
- Data retention: 15 years (extension to 20 under analysis)
- ATC18RHA 0.18um technology + E2 cell: Hardening by design
  - TID expected better than 60 Krad
  - 5 E-7 error/device/day target in GEO (or 2 E-11 error/configuration)

Securing FPGA Configuration

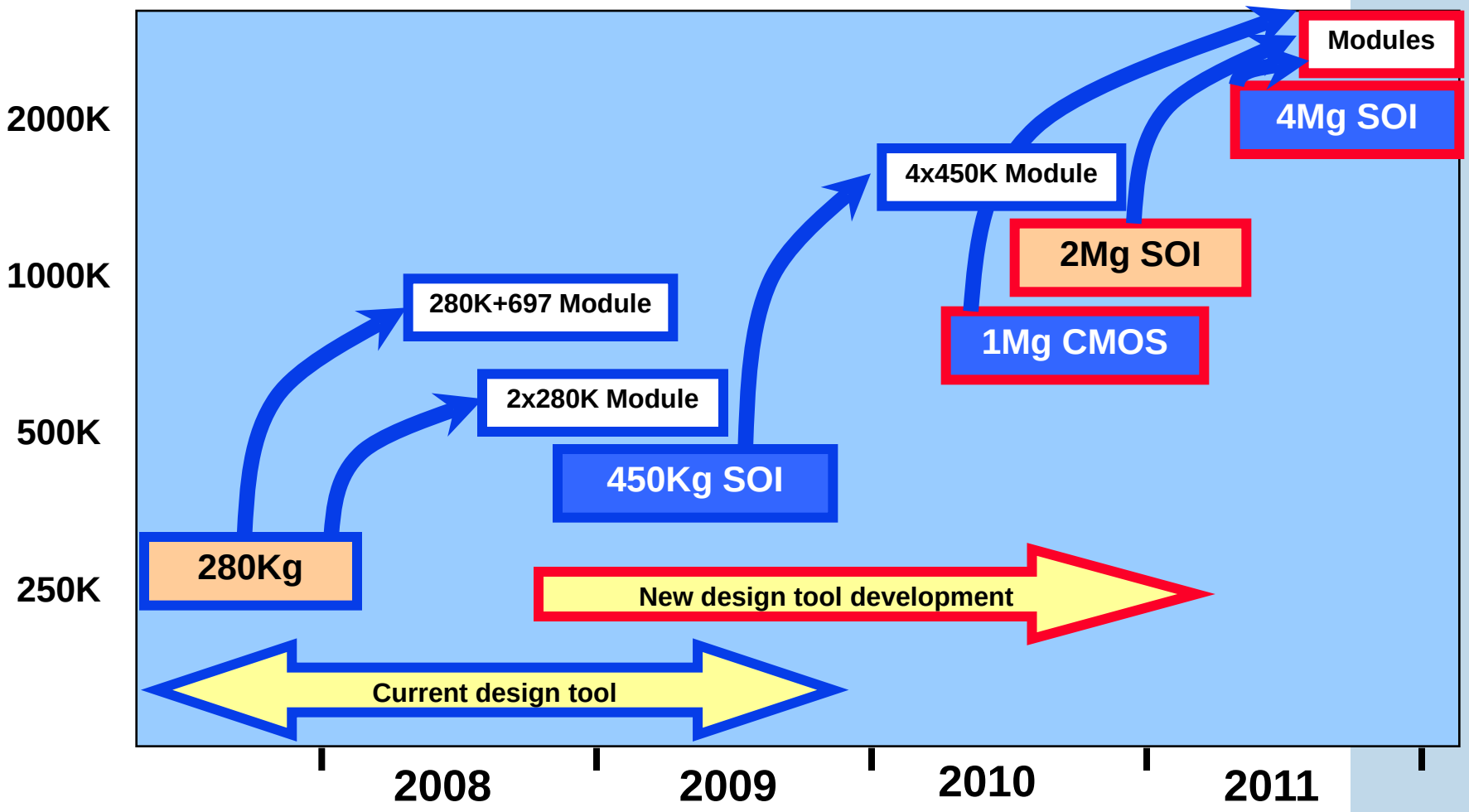


- **SRAM-based FPGAs reload their configuration on power-up**

  [1] Configuration Load checker (CRC) secures bit stream download

  [2] Configuration Self-Integrity checker secures internal configuration during operation

SPACE FPGA ROADMAP SUMMARY



Contact and Documentation

- **Atmel website**
  - http://www.atmel.com/dyn/products/devices.asp?family_id=641
- **Hotline**
  - Radhard-fpga@nto.atmel.com
- **Radiation reports upon request**
- **Qualification and Evaluation Qualpacks upon request**

Thank you!

Questions?

Add-On slides

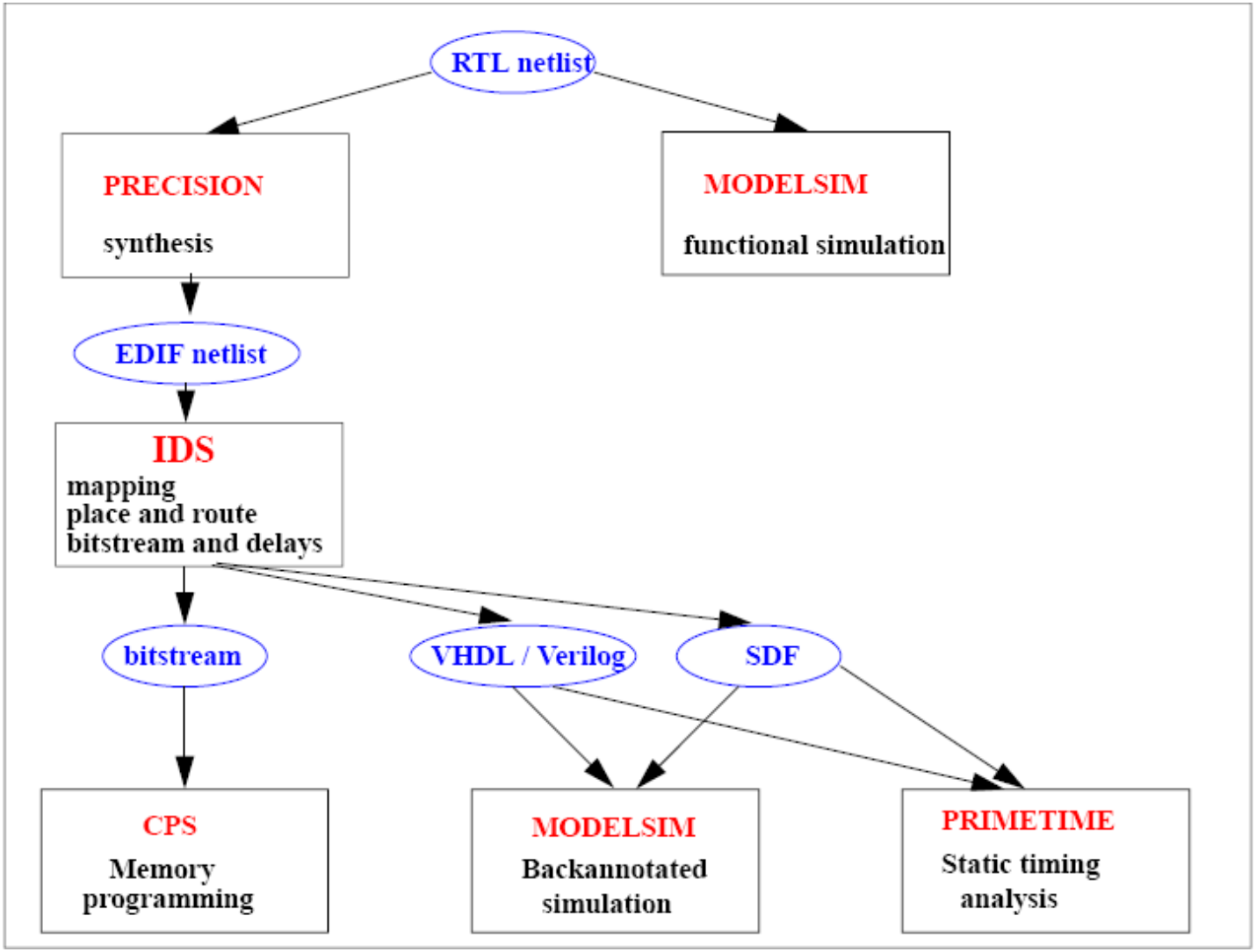
Key Features & Benefits (1/2)

Feature	Benefit
. Distributed Fast SRAM (FreeRAM™)	. Faster, lower cost for designs using SRAM
. Fast & efficient array multipliers & computing logic w/o using busses	. Faster, lower cost DSP designs
. Engineering Change Option (ECO)	. Fast Incremental design changes w/o recompiling entire design
. Schmitt Trigger on every input	. Better hysteresis (noise immunity) & performance
. Extremely low power consumption (~5mA standby)	. Improved reliability, longer battery life and autonomy
. Extremely small FreeRAM granularity	. Well suited for DSP applications

Key Features & Benefits (2/2)

Feature	Benefit
. On-board CRC data checker	. Reliable mission critical applications
. Full PCI compliance	. PCI logic can be implemented in ATF280E meeting PCI requirements
. Cache Logic capability	. Dynamic reconfiguration
. Automatic component generators (Logic & RAM compilers)	. Fully predictable, reusable designs
. Industry standard design tools with optimized synthesis compiler	. Minimizes investment in tools and don't have to learn new tools
. Easy Migration to Atmel ASIC	. Cost reduction for high volume designs

Design Flow


RTL netlist
PRECISION
synthesis
MODELSIM
functional simulation
EDIF netlist
IDS
mapping
place and route
bitstream and delays
bitstream
VHDL / Verilog
SDF
CPS
Memory
programming
MODELSIM
Backannotated
simulation
PRIMETIME
Static timing
analysis

AT40KEL040 Radiation Performances (1/2)

- **TiD Performances**
  - **Tested up to 300Krads**
    - **All parts passed all functional and electrical tests**
    - **Dynamic parameters unchanged**
    - **No leakage**

- **SEL Performances**
  - **Tested up to 70 MeV.cm²/mg**
    - **No single event latch-up up to 70 MeV.cm²/mg (maximum LET used for the test)**

AT40KEL Results
SEU results

Orbit	Error rate /bit/day	Error rate /device/day	MTTF (years)
GEO	4.1 E-9	7.0 E-5	39
LEO 53°/1000km	2.4 E-8	4.0 E-4	7
LEO 98°/852km. Spot	1.0 E-8	1.7 E-4	16
LEO 98°/600km	4.4 E-9	7.5 E-5	36
LEO 510/450km. ISS	1.3 E-9	2.2 E-5	125

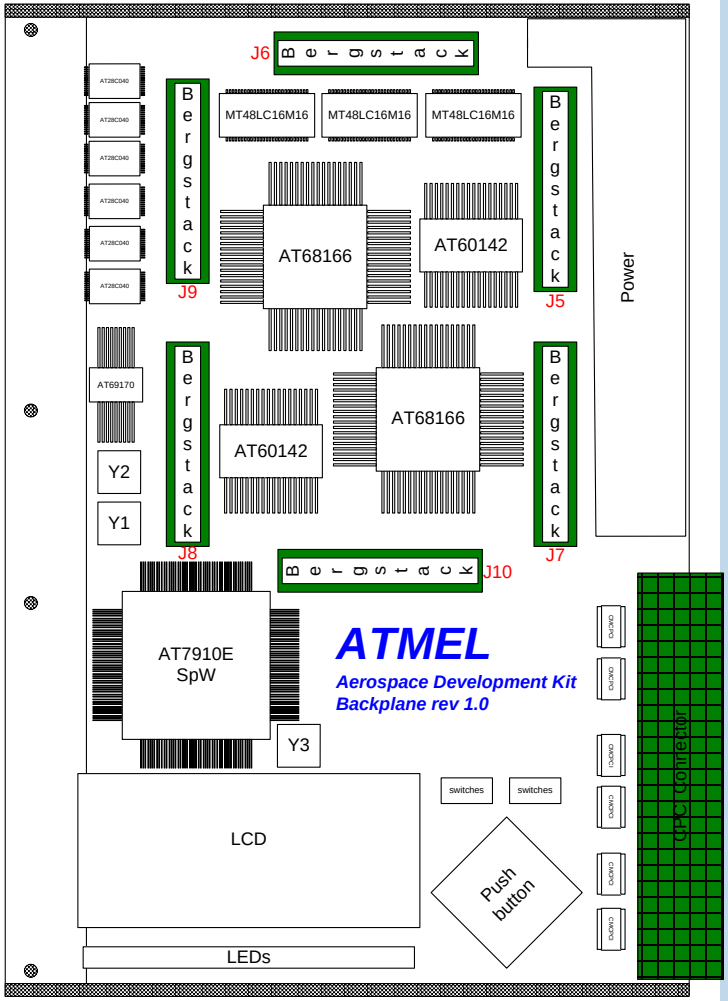
1Mbit EEPROMs

- **AT17LV010-10DP serial EEPROM**
  - **3.3V supply voltage**
  - **FP28 Package**
  - **Total dose better than 20 Krads when biased**
  - **Total dose better than 60 Krads when unbiased**

- **AT28C010-12DK 128k x 8 EEPROM**
  - **5V supply voltage**
  - **FP32 Package**
  - **Total dose better than 10 Krads when biased**
  - **Total dose better than 30 Krads when unbiased**

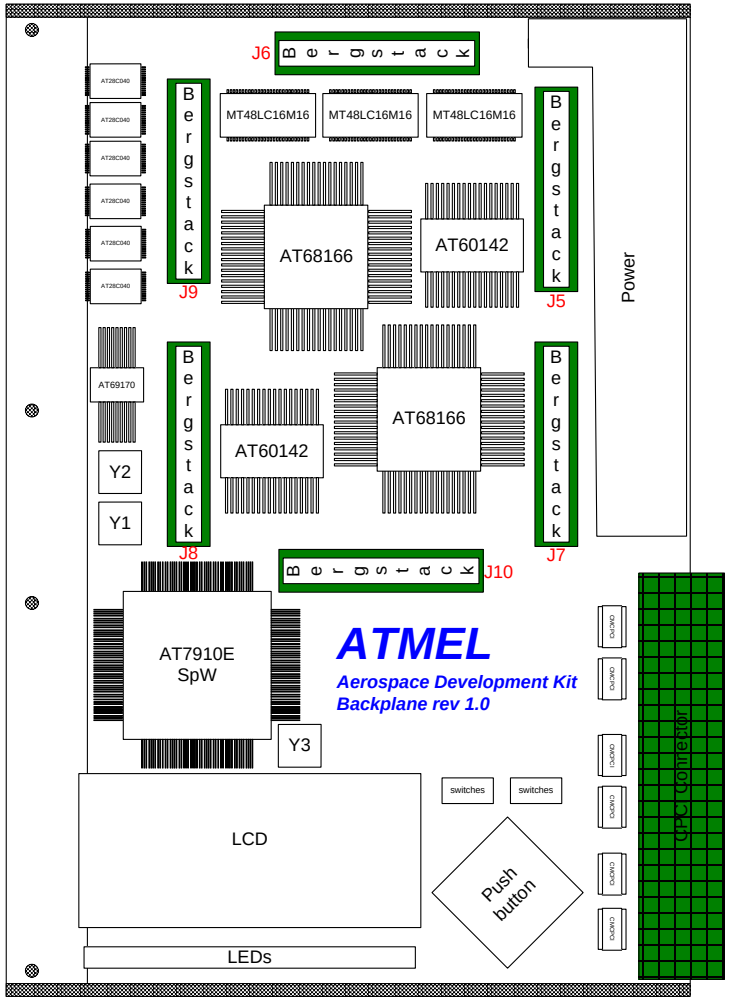
Hardware Platform – Backplane (1/3)

- **6U - Compact PCI form factor**
- **Front panel with communication interfaces connectors**
  - **Power Indicators**
  - **Main Reset Pushbutton**
  - **8x SpaceWire Interface**
  - **2x Uart Interface**
  - **1x SpaceProgrammer Interface**



Hardware Platform – Backplane (2/3)

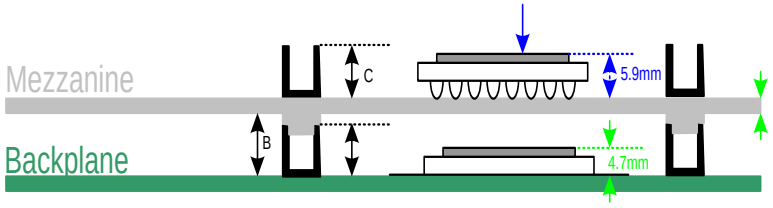
- **Main Features**
  - **AT69170E Configurator**
    - **4Mbit serial EEPROM**
  - **AT68166F SRAM MCM**
    - **16Mb SRAM (512K x 32)**
  - **AT60142F SRAM**
    - **4Mb SRAM (512K x 8)**
  - **AT7910 SpaceWire Router**
- **Allows evaluation of the FPGA with other ATMEL space qualified components**



ATF280 Hardware Development Platform

- **The hardware platform is the main platform for**
  - **Evaluating the ATF280E FPGA**
  - **Demonstrating the ATF280E FPGA**
  - **Developing ATF280E-based applications**

- **The hardware platform is made of two modules**
  - **A backplane with a set of peripherals**
  - **A mezzanine board with the ATF280 Soldered**



Hardware Platform – SpaceProgrammer (1/2)

- **SpaceProgrammer replaces CPS**
- **USB Host interface**
  - **Programmation Dongle seen as a standard RS232 COM port**
- **HE10 Target Interface**
  - **Galvanic isolation with Target(s)**