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RTProASIC3 Qualification Plans

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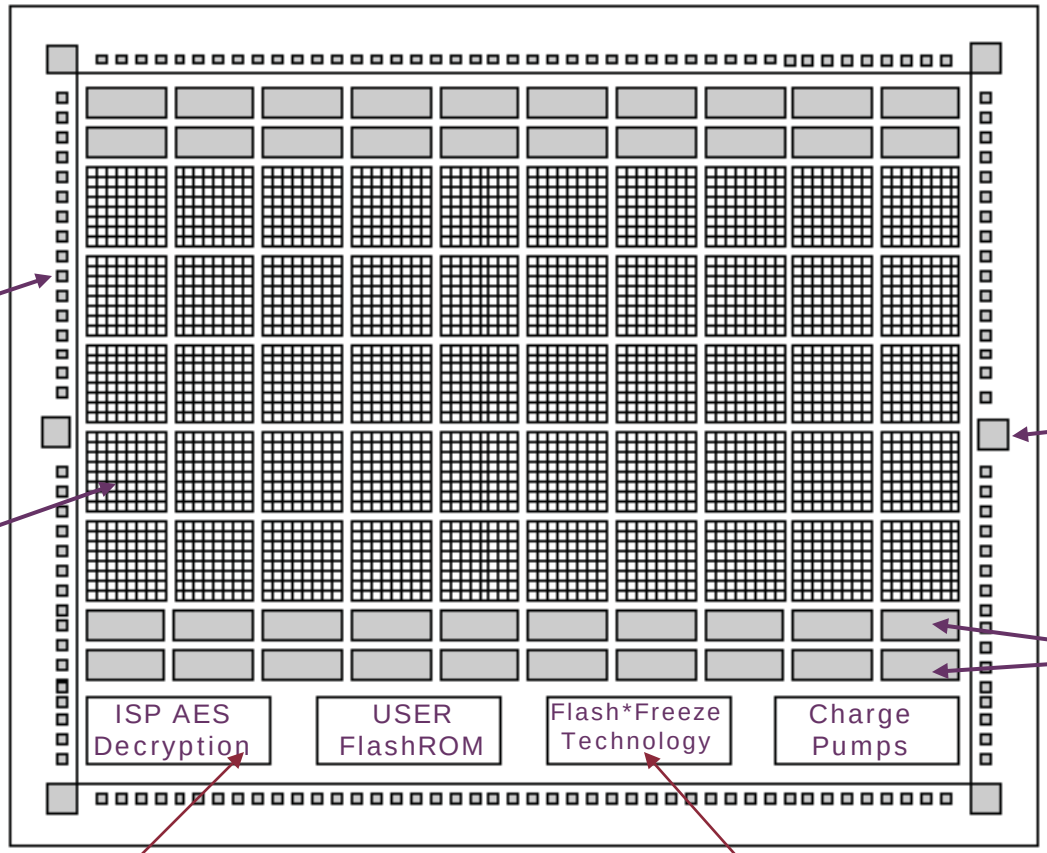
Presentation Outline

- RTProASIC3 Highlights
- Flash Switch Architecture and Operation
- Production Test Methodology
- Qualification Plans
- Conclusion

RTProASIC3 HIGHLIGHTS

- 130nm Flash based LVCMOS process
- Firm Error (FER) Immune



I/O's

(i.e. LVTTL, LVCMOS, PCI, PCI-X, LVPECL, LVDS, BLVDS, M-LVDS, GTL, GTL+, HSTL)

Versa Tiles
(Core operates at either 1.2V or 1.5V)

Clock Conditioning Circuit / PLL

Embedded SRAM Blocks

Secure Programming / Arm Cortex-M1 soft processor support

Allows instantaneous shut off of dynamic power consumption while retaining all SRAM and register information

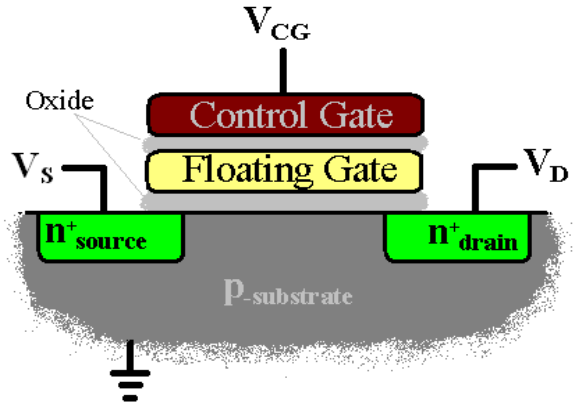
RTProASIC3 HIGHLIGHTS

Features Summary

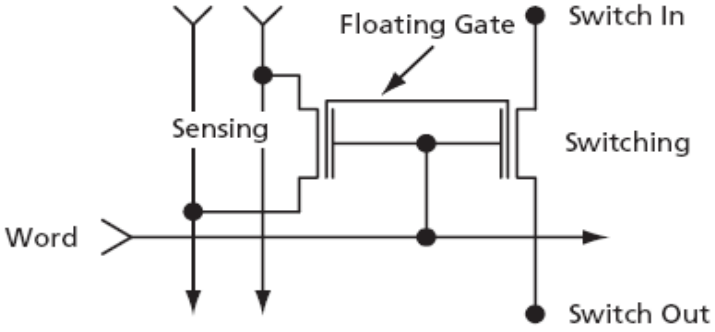
RT ProASIC3 Devices	RT3PE600L	RT3PE3000L
ARM Cortex-M1 Devices		M1RT3PE3000L
System Gates	600 k	3 M
VersaTiles (D-flip-flops)	13,824	75,264
RAM kbits (1,024 bits)	108	504
4,608-Bit Blocks	24	112
FlashROM Bits	1 k	1 k
Secure (AES) ISP	Yes	Yes
Integratred PLL in CCCs	6	6
VersaNet Globals	18	18
I/O Banks	8	8
Maximum User I/Os	270	620
Package Pins	CG/LG484	CG/LG484, CG/LG896

Flash Switch Architecture

- The Flash switch (Non-Volatile Memory cell) is a floating gate transistor

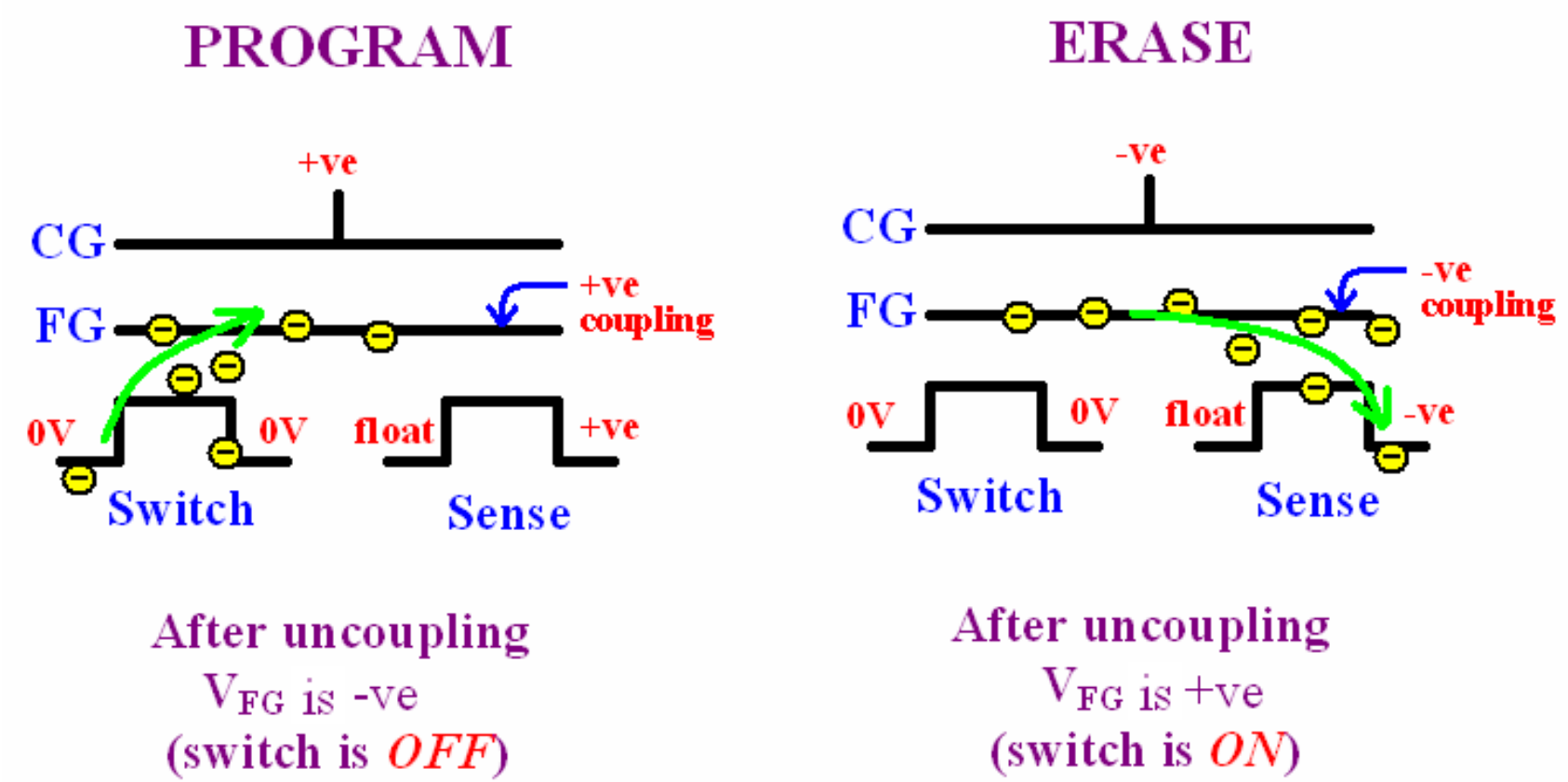


- The RTProASIC3 Flash cell is composed of 2 transistors sharing a common floating and control gate



- Used for logic head configuration and routing tracks connection/isolation

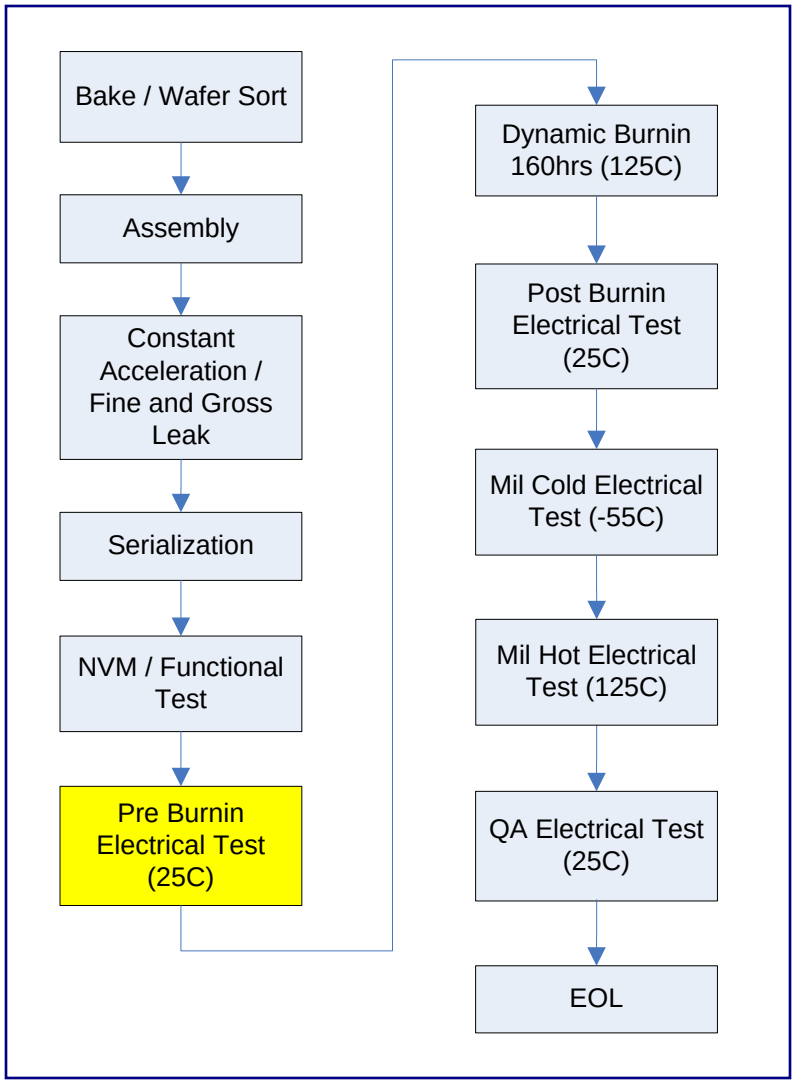
Program & Erase Operation



- Internal charge pumps provide the high positive/negative voltages required

Production Test Methodology

Per MIL-STD-883E Production Flow



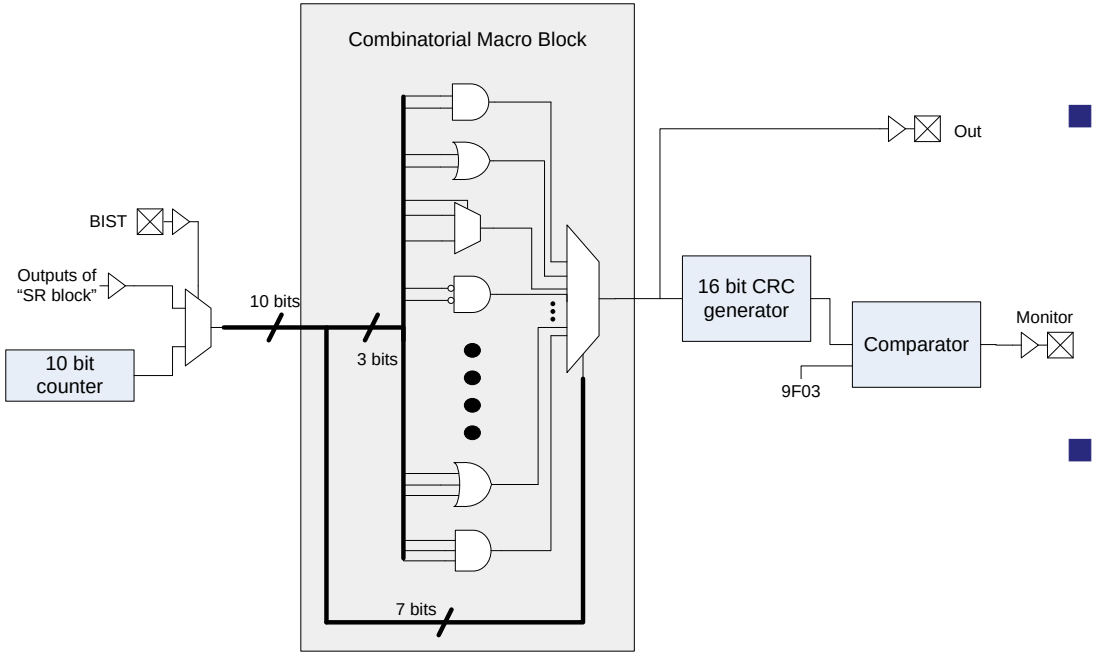
Burn-In Electrical Test

- High utilization Burn-In test design used in both production flow and qualification (Group C test)

- Coverage of test
  - **Electronic serialization based on Lot/Wafer/Die X,Y information**
  - **Standby I_{dd} on individual power domain**
  - **Full DC parametric testing for all configurations on all bonded I/Os**
  - **Functional test for Burn-in design**
  - **PLL functional test**
  - **Delay Line Test (speed performance)**

Burn-In Design Overview (1 of 3)

- Clock Source
  - External clock is fed into the PLLs of the device
  - PLLs deliver the clock signals through global (low skew) networks

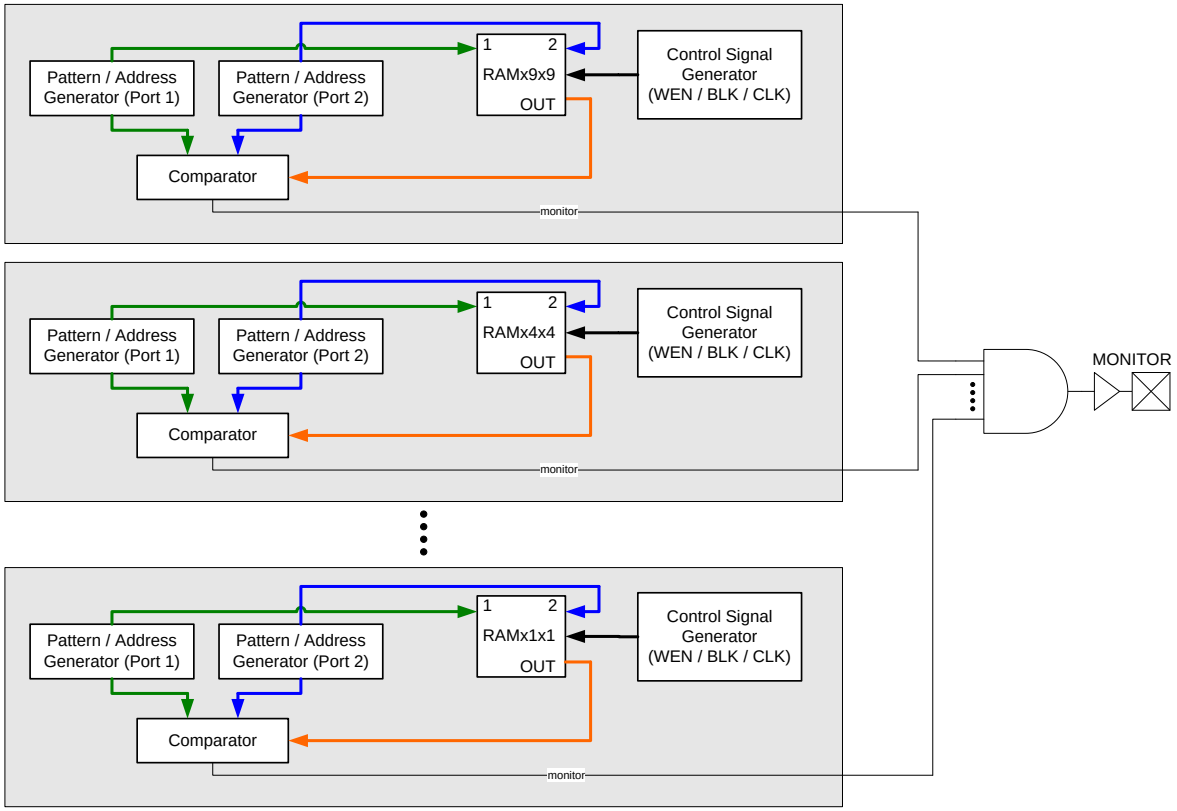


- Combo Block
  - Utilizes every combinatorial macro available in the A3P library.
- Register & Latch Block
  - Utilizes every sequential macro available in the A3P library.

- USER FlashROM (UFROM)
  - Pre-determined Combo Block output pattern is stored into the UFROM
  - Content is compared during burn-in

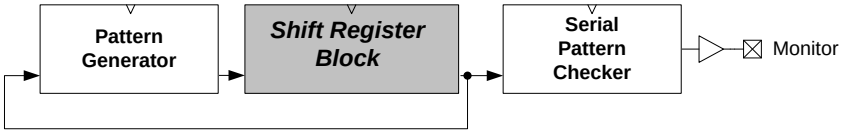
Burn-In Design Overview (2 of 3)

- Embedded SRAM Blocks
  - **Full test coverage on all SRAM cells**
  - **Dual Port / Two Port / FIFO configurations**
  - **Varying depth and width configurations**

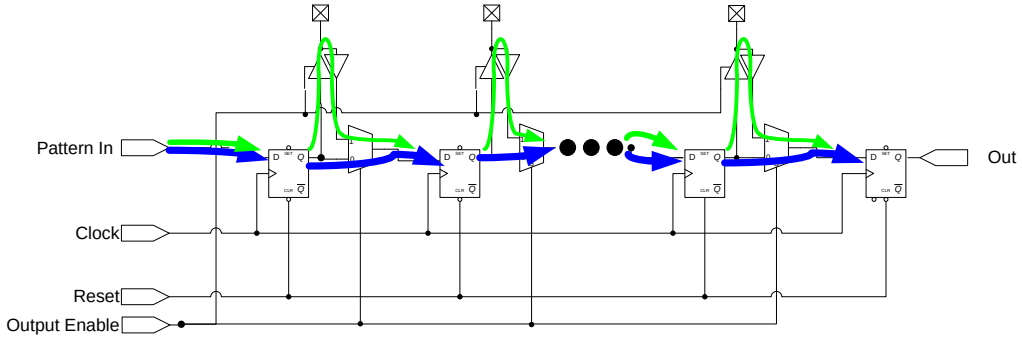


Burn-In Design Overview (3 of 3)

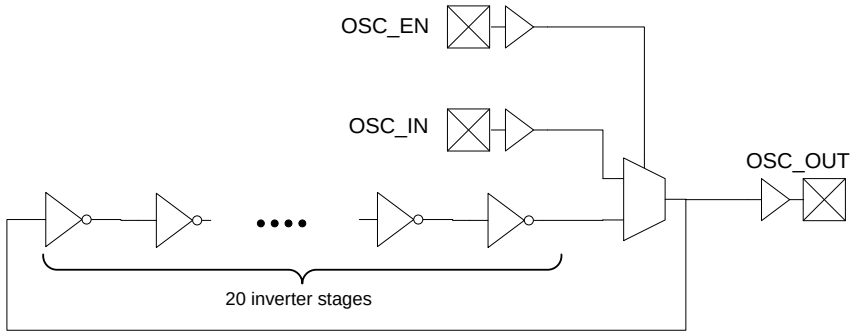
- Shift Register Block
  - Scalable block for maximizing core utilization
  - Controlled simultaneous switch rate (SSR)



- IO Block
  - Scalable block for maximizing I/O utilization
  - Utilizes all possible I/O configurations
  - Controlled simultaneous switching outputs (SSO)



- Oscillator Block
  - Free running oscillator to monitor silicon performance



Qualification Plans

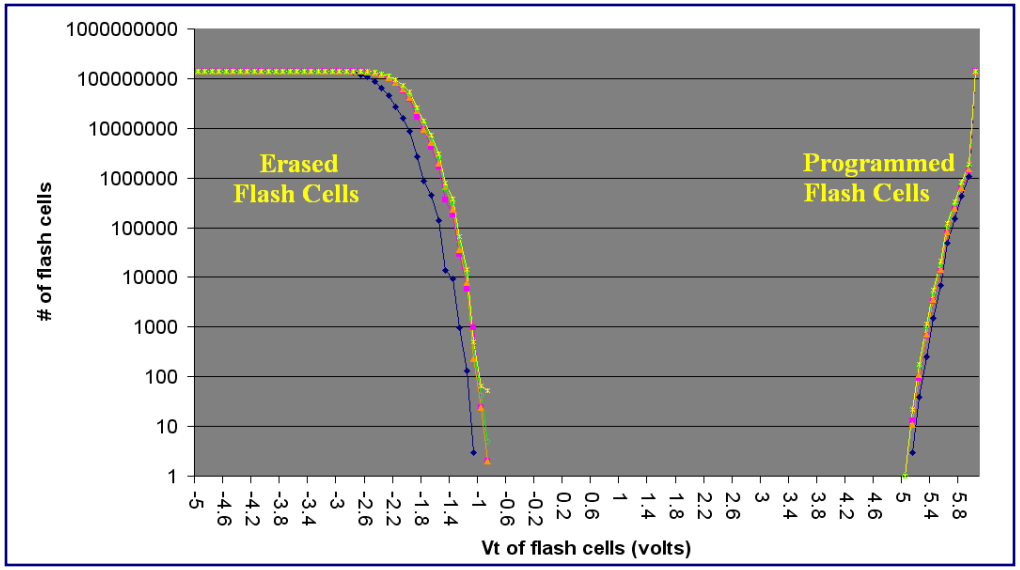
Qualification Device: RT3PE3000L–CG896

Stress Test	Reference	Test Condition	No. of Qual Lots	# Failures / Sample Size	Test Duration / Pull Point
Group A	MIL-STD-883	T_A = - 55°C / 25°C / 125°C	1	0/116	Electrical test points
Group C* (HTOL)	MIL-STD-883 (TM1005)	T_A = 125°C V_{CC} / V_{CC_PLL} = 1.6V V_{CCI} / V_{PP} / V_{JTAG} = 3.6V	1	1/77	168 hrs 500 hrs 1000 hrs
ESD	MIL-STD-883 (TM3015)	HBM	1	0/3	Target >= 2000V
Latchup	JEDEC 78	T_A = 125°C	1	0/3	> 200 mA
Capacitance Test	MIL-STD-883 (TM3012)	T_A = 25°C	1	0/3	< 8pF
Characterization		T_A = - 55°C to 125°C Bias = min to max operating condition	1	5	

**Note: As part of the ongoing reliability process, HTOL will continue up to 6000 hrs*

Group C Tests

- Pre Group C
  - **Endurance test – 550 program/erase cycles**
  - **Margining – complete characterization of flash cells**



- Group C
  - **1000 cumulative hours of HTOL (T_A = 125°C)**
- Post Group C
  - **Full electrical / functional test**
  - **Margining – monitor any Vt shift (charge leakage) in flash cells**

Conclusion

- First re-programmable RT Flash based FPGA
- Full compliance to MIL-STD-883B
- Qualification completion targeted in Q1’09

Acknowledgement

Thank you to the following people who helped made this presentation possible

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And everyone else who were involved in coming up with the Burn-in design methodology