Achieving High Performance Computing and Application Flexibility within the Spacecraft Payload

Ian Troxel, Matthew Fehringer, Michael Chenoweth, and Paul Murray
SEAKR Engineering, Inc.
Centennial, CO

Military and Aerospace Programmable Logic Devices (MAPLD) Conference
Annapolis, MD
September 16-18, 2008
Motivation

- Faster, better, cheaper – often no longer just picking two!

- Mission requirements increasing
  - Higher resolution data acquisition driving processing and storage requirements
  - Onboard processing and/or downlink often the system bottleneck
  - Increased need for autonomous functionality affecting system “overhead”

- Design challenges keeping pace
  - SWaP limitations on payloads not relaxing
  - Flexible, multiuse payloads sought to limit NRE
  - Use of Commercial-Off-The-Shelf (COTS) devices
    - “Radiation-hardened” components often not cost-effective for high-performance applications
    - COTS provide improved performance but typically require mitigation to achieve the same level of fault tolerance
  - Reconfigurable Computing (RCCs) devices
    - Typically improve performance/Watt for amenable application classes
    - Reconfigurability offers increased payload flexibility
HPC with Flexibility

- **Application Independent Processor (AIP) Features**
  - Mixture of scalar processors and RCCs
  - Reconfigurable on-orbit
  - Flexible, scalable architecture
  - Usage of open standards
  - SEE Tolerant system
  - Flexible I/O architecture

- **Designed for Responsive Space**
  - Low cost, high performance
  - Rapid deployment through adaptability
  - Designed for multiple missions

- **Missions To Date**
  - Advanced Responsive Tactically Effective Military Imaging Spectrometer (ARTEMIS)
  - Programmable Space Transceiver (PST)
  - Programmable Space IP Modem (PSIM)
  - Orion Vision Processing Unit (VPU)
  - JPEG2K image compression
AIP System Architecture

- Reconfigurable Computer Board(s)
  - Xilinx™ V4, high-speed memory and SERDES backplane
- COTS PowerPC™-based SBC(s)
  - 600 DMIPs, 1.2 GFLOP, Gigabit Ethernet and Spacewire
- Memory and I/O personality mezzanine cards
  - 16 GBytes flash memory, camera link, analog, digital developed to date
AIP Personality Mezz. Card

- Personality Mezzanine for application-specific functionality
  - Lower risk, quick development, lower costs
  - I/O and unique I/O connectors
  - Memory
  - Logic
  - TMR mitigation
  - Analog circuitry ADC/DAC
- High speed mezzanine connectors
  - 170 high speed I/O
    - LVDS
    - High speed serial
    - TMR’d signals
  - Symmetrical Design to all Xilinx™ FPGAs
- Fault tolerance options
  - “Radiation hardened” voter on the mezz.
  - Partial TMR
  - SEAKR replay capability provides temporal redundancy
  - Combinations
AIP SEE Mitigation

- One size does not fit all
- Mitigation methods are highly application dependant
  - SWAP constraints
  - Processing performance
  - Reliability requirements
  - Design schedule
  - Type of data and peripherals
  - Latency constraints
- Factors need to be weighed before an approach can be implemented
- Optimum designs may use a quiver of mitigation methods
  - Combination of HW and SW
- AIP personality mezzanine card provides fault tolerance options
TacSat-3 Mission Summary

- Tactical operations with real-time downlink for command and control
- Images processed by ARTEMIS
- First incarnation of the AIP
- AFRL system with Raytheon sensors
- Flight delivered, launch scheduled ‘09

**Tactical Ground Station:**
2. Uplink Tasking
6. Receive Data Cube Image
7. Disseminate Additional Data Products

**Spacecraft:**
3. Collect Image
4. Process Product
5. Downlink Narrow Band
6. Downlink Wide Band

**Warfighter:**
1. Send Tasking
6. Receive Product

**Target Area:**
2 km x 14 km

c/o AFRL-Kirtland
ARTEMIS Design Highlights

- Combination of sequential processor and RCC
  - Two Xilinx™ FPGAs required to meet data throughput from sensors
  - FPGAs perform data acquisition and preprocessing functions such as calibration
  - Microblaze™ core coordinates memory accesses and processor communication
  - PowerPC™ SBC dedicated to image generation and target cueing

- Prior generation did not use RCCs because the data processing and SWaP requirements were not as challenging (airborne system)
  - RCCs required to meet desired SWaP on spacecraft
    - Size: 7.82H x 11.41W x 10.0D inches
    - Mass: 18 lbs
    - Power: 40 Watts (requirement less than 50W)

- Configuration scrubbing used for RCC SEU mitigation
  - Need to correct control path corruptions
PST Mission Summary

- Programmable Satellite Transceiver (PST) provides frequency agile sat. comm.
  - Each band continuously tunable
  - Programmable on the ground and/or in flight
- AFRL Enhanced Phase-II SBIR with EM delivered Q2‘08

Receiver/Uplink
- L-Band 1760 to 1840 MHz
- S-Band 2025 to 2120 MHz

Transmitter/Downlink
- S-Band 2200 to 2300 MHz

Space Ground Link System (SGLS)
- FSK-AM Command Uplink (1 kbps, 2 kbps)
- Subcarrier BPSK Telemetry Downlink (256 kbps)

Universal S-Band (USB)
- Subcarrier BPSK Command Uplink (<= 4 kbps)
- Subcarrier BPSK Telemetry Downlink (256 kbps)

Future Waveforms in development
PST Design Highlights

- FPGA devices form the basis of the Digital Module
  - Agile waveform processing performed in Xilinx™ FPGAs
  - Given SWaP requirements, even high-end PowerPCs could not meet specs
    - 3.86H x 6.85 W x 7.0D inches, Mass: 10 lbs, Power: RX: 16W, TX: 45W
  - Waveform processing updated through reconfiguration

- RCC SEU mitigation
  - Xilinx™ configuration scrubbing used for SEU mitigation to correct control path
  - Memory interfaces replicated in triplicate
PSIM Mission Summary

- Programmable Satellite Internet Protocol Modem (PSIM) translates between standard sat. comm. waveforms and IP/Ethernet
- Commercial customer with flight units delivered Q3‘08
- Packet-based satellite communication
  - Virtual circuit philosophy
  - Beam and waveform independent routing
- Advantages over bent-pipe sat. comm.
  - Improves scalability and throughput
  - Decentralized multicast
  - Fine-grained QoS possible
PSIM Design Highlights

- Combination of two sequential processors, 12 FPGAs and analog switch card
  - FPGAs provide waveform processing
  - Processors provide Ethernet interfaces, packet switching
  - Leveraging the advantages of each type of component

- Mezzanine card includes majority voting and router physical interfaces

PSIM Configuration of AIP
Orion-VPU Mission Summary

- VPU provides a reconfigurable hardware platform for processing image algorithms
  - Pose Estimation
  - Optical Navigation
  - Compression/Decompression

- Receives image data from various Relative Navigation Sensors
  - Star Tracker
  - Vision Navigation Sensor
  - Docking Camera
  - Situational Awareness Camera

- Supports rendezvous, proximity operations, docking and undocking for ISS and Lunar missions

Images c/o Orion Program Office, NASA-Glenn

Troxel, Fehringer, Chenoweth, and Murray

Achieving High Performance Computing and Application Flexibility…
ORION-VPU Highlights

- Combination of sequential processor and RCC
  - Xilinx™ FPGAs deployed in TMR for high criticality sensor algorithms
    - Video processing algorithms (i.e. feature recognition, graphical overlay, tiling, etc.) and video compression
  - Microblaze™ core coordinates algorithm cores and processor communication
  - LEON™ SBC dedicated to system coordination, error handling, RCC configuration and oversight and interconnect control
    - Time-Triggered Gigabit Ethernet PMC and RS422

- Mezzanine card provides sensor interfaces
  - LVDS interfaces with access to all three FPGAs for flexibility in video stream selection and mitigation schemes

- Configuration scrubbing and TMR for RCC SEU mitigation
  - Corrects control path corruptions
Conclusions

- Application Independent Processor developed for space applications
  - Supports the responsive space mission (e.g. TacSat-3)
  - Reconfigurable on-orbit
  - Flexible, scalable architecture

- Mission performance requirements driving the use of commercial devices
  - Low cost, high performance
  - Designed for multiple missions

- Flexibility demonstrated on several missions
  - Advanced Responsive Tactically Effective Military Imaging Spectrometer (ARTEMIS)
  - Programmable Space Transceiver (PST)
  - Programmable Space IP Modem (PSIM)
  - Orion Vision Processing Unit (VPU)
### SEAKR Heritage

#### PRODUCT CODE
- Memory Systems
- On-Board Processors
- Manned Flight
- Spacecraft Avionics
- Satellite Communications
- Other-Than-Space

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<tr>
<td>Clementine</td>
<td>ACE SEASTAR</td>
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<tr>
<td>APEX MicroLabs RadarSat NEAR Spartan</td>
<td>MARS98 P91 QuickScat DMSP (F15) MightSat II</td>
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<td>ACTEX</td>
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#### 71 Launched Systems 100% Success Rate

- **Launched 2001 - 2002**
  - Mars Odyssey GeoLITE
  - Quickbird SAGE III
  - HESSI MMU (Shuttle) HCOR (ISS)

- **Launched 2003 - 2005**
  - Coriolis ICE Sat GALEX
  - Orimage (3 & 4) DMSP (F16)
  - Gravity Probe B MRO Swift

- **Launched 2005-2008**
  - Deep Impact CloudSat
  - DMSP (F17) Cibola P909 Phoenix Lander
  - JEM HRDR JEM-SSEDSU Worldview-1 Kepler Glast

- **Delivered**
  - ARTEMIS DMSP 5D3
  - Challenger HADAS/DAAS
  - LEO LTMPF
  - MAU - C&DH MMSM
  - NEMO NPP RCC-MAP
  - SRB SSP
  - DSX-ECS DSX-C&DH SBSS-SSR
  - SBSS-C&DH WBDG Worldview-2 PST SpaceCube WISE-FMC OCO

#### Development
- VPU NPOESS SBR-OBP IADMS - NGST
- SSP IRIS RSNIC C-17 MMC
- iAPS JWST SSR CEU

SEAKR’s product mix shift from nearly 100% SSRs to 25 – 40% SSRs
## Contact Information

<table>
<thead>
<tr>
<th>Name</th>
<th>Position</th>
<th>Contact Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dave Jungkind</td>
<td>Business Development</td>
<td><a href="mailto:dave.jungkind@SEAKR.com">dave.jungkind@SEAKR.com</a></td>
</tr>
<tr>
<td>Dr. Ian Troxel</td>
<td>Future Systems Architect</td>
<td><a href="mailto:ian.troxel@SEAKR.com">ian.troxel@SEAKR.com</a></td>
</tr>
</tbody>
</table>

SEAKR Engineering, Inc.
6221 South Racine Circle
Centennial, CO 80111-6427
main: 303 790 8499
fax: 303 790 8720
web: http://www.SEAKR.com