Implementing Image Registration Algorithms on Reconfigurable Computer

Miaoqing Huang\(^1\)
Olivier Serres\(^1\) Tarek El-Ghazawi\(^1\) Greg Newby\(^2\)

\(^1\)Department of Electrical and Computer Engineering
The George Washington University

\(^2\)Arctic Region Supercomputing Center
University of Alaska Fairbanks

MAPLD 2008
Outline

1. **Background**
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2. **Image Registration Using Hardware**
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3. **Implementation and Results**

4. **Conclusions**
Outline

1 Background
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2 Image Registration Using Hardware
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3 Implementation and Results

4 Conclusions
Outline

1 Background
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2 Image Registration Using Hardware
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3 Implementation and Results

4 Conclusions
Reconfigurable Hardware Accelerator (e.g. FPGA) is treated as co-processor to microprocessor ($\mu P$)
Reconfigurable Hardware Accelerator (e.g. FPGA) is treated as co-processor to microprocessor ($\mu P$)

FPGA is connected to $\mu P$ through high-speed interconnect

- SGI RC100: NUMAlink4, 3.2GB/s
- Cray XD1: HyperTransport, 1.6GB/s
Reconfigurable Hardware Accelerator (e.g. FPGA) is treated as co-processor to microprocessor ($\mu P$)

- FPGA is connected to $\mu P$ through high-speed interconnect
  - SGI RC100: NUMAlk4, 3.2GB/s
  - Cray XD1: HyperTransport, 1.6GB/s

FPGA is connected into multiple local memory banks
- User logic can access multiple banks in parallel
Outline

1. **Background**
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2. **Image Registration Using Hardware**
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3. **Implementation and Results**

4. **Conclusions**
What is Image Registration?

Image registration is a fundamental task in image processing used to match two or more pictures taken at different times, from different sensors, or from different viewpoints.

source  target  registered source
Image Registration as Transformation between Images

Mapping two images, the reference image and the test image, both spatially and with respect to intensity

\[ l_2(x, y) = g(l_1(f(x, y))) \]

Four components in image registration

1. **a feature space**: the set of characteristics used to match
2. **a search space**: the potential transformations between reference and test images
3. **a search strategy**: decide how to choose next transformation in the search space
4. **a similarity metric**: evaluate the match between reference image and transformed test image
Rigid-body Transformation

Rigid-body transformation [Brown 1992] is a combination of a rotation ($\theta$), a translation ($t_x, t_y$), and a scale change ($s$).

$$
\begin{align*}
(x_2, y_2) &= (t_x, t_y) + s \begin{pmatrix}
\cos \theta & -\sin \theta \\
\sin \theta & \cos \theta
\end{pmatrix} \begin{pmatrix}
x_1 \\
y_1
\end{pmatrix} \\
\overline{p}_2 &= \overline{t} + sR\overline{p}_1
\end{align*}
$$

Note: the scale change $s$ is assumed to be 1 in this work

Outline

1. Background
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2. Image Registration Using Hardware
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3. Implementation and Results

4. Conclusions
Selected Image Registration Mechanism

- Transformation: rigid-body transformation
- Search space: \((\Delta \Theta, \Delta X, \Delta Y)\)
- Similarity metric: correlation coefficient between reference image \(R\) and transformed image \(T'\)

\[
\frac{\sum_{x,y} (R(x, y) - \mu_R)(T'(x, y) - \mu_{T'})}{\sqrt{\sum_{x,y} (R(x, y) - \mu_R)^2 \sum_{x,y} (T'(x, y) - \mu_{T'})^2}}
\]

- Two search strategies
  1. Exhaustive search algorithm
  2. Discrete Wavelet Transform (DWT)-based search algorithm
Outline

1 Background
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2 Image Registration Using Hardware
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3 Implementation and Results

4 Conclusions
The Algorithm and Advantages of Hardware Implementation

- Initialize the maximum correlation coefficient $mcc$ to be zero
- Select the first test tuple $(\theta, t_x, t_y)$ in the search space
- Apply rigid-body transformation on test image to get $T'$
- Calculate the correlation coefficient $cc$ between $R$ and $T'$

**Decision Tree:**

1. $mcc > cc$?
   - Y: $mcc = cc$ and save the corresponding $(\theta, t_x, t_y)$
   - N: Select the next tuple $(\theta, t_x, t_y)$ in the search space

2. Are all tuples tested?
   - Y: Terminate
   - N: Select the next tuple $(\theta, t_x, t_y)$ in the search space

The advantages of hardware implementation:
- Multiple $(\theta, t_x, t_y)$ tuples can be tested in parallel
  - Limited by available *hardware resource* or *memory banks*
- Pipelined design can process multiple pixels every clock cycle
Calculate the Image Registration Time in Hardware – **Assumptions**

1. Both reference image and test image are in 8-bit gray-scale and consist of \( m \) pixels
2. \( n + 2 \) local memory banks with FPGA device
   - One bank \( \rightarrow R \), one bank \( \rightarrow T \), \( n \) banks \( \rightarrow n \ T' \)s
   - Each bank has independent read and write ports
3. The memory access port is \( d \)-byte wide
   - \( d \) pixels can be accessed every clock cycle
4. \( n (\theta, t_x, t_y) \) tuples are processed in parallel
   - Use forward transformation
5. All designs are fully pipelined
Calculate the Image Registration Time in Hardware

*Three steps to test one $(\theta, t_x, t_y)$ tuple:*

1. Initialize the memory region $T'$ to be zero
2. Apply rigid-body transformation on $T$ to get $T'$

\[
\begin{pmatrix} x_2 \\ y_2 \end{pmatrix} = \begin{pmatrix} t_x \\ t_y \end{pmatrix} + \begin{pmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{pmatrix} \begin{pmatrix} x_1 \\ y_1 \end{pmatrix}
\]

3. Calculate correlation coefficient between reference image $R$ and transformed image $T'$

\[
\frac{\sum_{x,y} (R(x, y) - \mu_R)(T'(x, y) - \mu_{T'})}{\sqrt{\sum_{x,y} (R(x, y) - \mu_R)^2 \sum_{x,y} (T'(x, y) - \mu_{T'})^2}}
\]
Step 1: Initialize the memory region $T'$ to be zero

Two reasons for initializing $T'$:

- Several regions (shown in red) may not be covered by $T'$. 
- Artifacts due to discretization in forward transformation (shown as dark spots in the transformed image). 
- $m$ pixels can be initialized to zero every clock cycle. 
- $d$ clock cycles are needed.
Step 1: Initialize the memory region $T'$ to be zero

Two reasons for initializing $T'$:

- Several regions (shown in red) may not covered by $T'$
Step 1: Initialize the memory region $T'$ to be zero

Two reasons for initializing $T'$:

- Several regions (shown in red) may not covered by $T'$
- **Artifacts due to discretization in forward transformation** (shown as dark spots in the transformed image)
Step 1: Initialize the memory region $T'$ to be zero

Two reasons for initializing $T'$:
- Several regions (shown in red) may not covered by $T'$
- Artifacts due to discretization in forward transformation (shown as dark spots in the transformed image)
- $d$ pixels can be initialized to zero every clock cycle
  - $\frac{m}{d}$ clock cycles are needed
Step 2: Apply rigid-body transformation on $T$ to get $T'$

\[ (x_2, y_2) = (tx, ty) + \begin{pmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{pmatrix} (x_1, y_1) \]

- Start calculating $(x_1, y_1) \rightarrow (x_2, y_2)$ every clock cycle
  - $m$ clock cycles required
- Calculate the mean of image $T'$, $\mu_{T'}$, in the Step 2
Step 3: Calculate correlation coefficient between $R$ and $T'$

\[
\frac{\sum_{x,y} (R(x, y) - \mu_R)(T'(x, y) - \mu_{T'})}{\sqrt{\sum_{x,y} (R(x, y) - \mu_R)^2 \sum_{x,y} (T'(x, y) - \mu_{T'})^2}}
\]

- Start the processing of $d$ pixels every clock cycle
  - $\frac{m}{d}$ clock cycles are required
- Compute $\sum_{x,y} (R(x, y) - \mu_R)(T'(x, y) - \mu_{T'})$, $\sum_{x,y} (R(x, y) - \mu_R)^2$, and $\sum_{x,y} (T'(x, y) - \mu_{T'})^2$ at the same time
  - $\mu_R$ is precomputed by $\mu_P$ and then forwarded to FPGA
  - $\mu_{T'}$ is computed in Step 2
Hardware Computation Time using Exhaustive Search Algorithm

**Given**
- Search space: \((\Delta \Theta, \Delta X, \Delta Y)\)
- Both reference image and test image are in 8-bit gray-scale and consist of \(m\) pixels
- \(n + 2\) local memory modules
  - The access ports are \(d\)-byte wide

**Computation Time**
- Each tuple \((\theta, t_x, t_y)\) takes approximately \(\frac{d+2}{d}m\) clock cycles
- The search of overall space takes approximately
  \[
  \frac{\Delta \Theta \cdot \Delta X \cdot \Delta Y \cdot (d + 2)}{n \cdot d} m
  \] clock cycles
Outline

1 Background
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2 Image Registration Using Hardware
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3 Implementation and Results

4 Conclusions
Reduce Computation Demand through DWT Decomposition

Original or previous low-pass results, \( I_k \)

- **Low pass:** Decimate columns by 2
- **High pass:** Decimate columns by 2

**Rows**

- **Low pass:** Decimate rows by 2
- **High pass:** Decimate rows by 2

**Columns**

- **Low pass:** Decimate rows by 2
- **High pass:** Decimate rows by 2

- **\( L_{k+1} \)**
- **\( H_{k+1} \)**
- **\( L_{H_{k+1}} \)**
- **\( H_{L_{k+1}} \)**
- **\( H_{H_{k+1}} \)**
- **\( L_{H_{k+1}} \)**
- **\( I_{k+1} \)**

**Search Resolution**

<table>
<thead>
<tr>
<th>( I_0 )</th>
<th>( I_1 )</th>
<th>( \cdots )</th>
<th>( I_n )</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size</strong></td>
<td>( H \times W )</td>
<td>( \frac{H}{2} \times \frac{W}{2} )</td>
<td>( \cdots )</td>
</tr>
<tr>
<td><strong>Search Resolution</strong></td>
<td>( \delta_\theta, \delta_x, \delta_y )</td>
<td>( 2\delta_\theta, 2\delta_x, 2\delta_y )</td>
<td>( \cdots )</td>
</tr>
</tbody>
</table>


## Search Strategy Summary

<table>
<thead>
<tr>
<th>Decomposition Level</th>
<th>Search Space</th>
<th>Search Resolution</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n$</td>
<td>$\Delta \Theta$</td>
<td>$2^n \delta_\theta$</td>
<td>$\theta_n$</td>
</tr>
<tr>
<td>$n-1$</td>
<td>$[\theta_n - 2^n \delta_\theta; \theta_n + 2^n \delta_\theta]$</td>
<td>$2^{n-1} \delta_\theta$</td>
<td>$\theta_{n-1}$</td>
</tr>
<tr>
<td>$n-2$</td>
<td>$[\theta_{n-1} - 2^{n-1} \delta_\theta; \theta_{n-1} + 2^{n-1} \delta_\theta]$</td>
<td>$2^{n-2} \delta_\theta$</td>
<td>$\theta_{n-2}$</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>2</td>
<td>$[\theta_3 - 2^3 \delta_\theta; \theta_3 + 2^3 \delta_\theta]$</td>
<td>$2^2 \delta_\theta$</td>
<td>$\theta_2$</td>
</tr>
<tr>
<td>1</td>
<td>$[\theta_2 - 2^2 \delta_\theta; \theta_2 + 2^2 \delta_\theta]$</td>
<td>$2 \delta_\theta$</td>
<td>$\theta_1$</td>
</tr>
<tr>
<td>0</td>
<td>$[\theta_1 - 2 \delta_\theta; \theta_1 + 2 \delta_\theta]$</td>
<td>$\delta_\theta$</td>
<td>$\theta_0$</td>
</tr>
</tbody>
</table>

- **Decomposition**
  - $I_0$
  - $I_1$
  - $I_{n-1}$
  - $I_n$

- **Image Size**
  - $I_0$
  - $I_1$
  - $I_{n-1}$
  - $I_n$

- **Search Space**
  - $I_0$
  - $I_1$
  - $I_{n-1}$
  - $I_n$

- **Decrease the search space and increase the search resolution in the search process**
Outline

1 Background
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2 Image Registration Using Hardware
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3 Implementation and Results

4 Conclusions
Testbed: Cray XD1 Reconfigurable Computer

Specifications:

- FPGA device: Xilinx Virtex-II P50
- 4 local SRAM banks, 4 MBytes each
- Maximum user logic clock rate: 200 MHz

Memory usage of two different approaches:

**Exhaustive Search**

- mem#0
- mem#1
- mem#2
- mem#3

- \( R \)
- \( T \)
- \( T'_0 \)
- \( T'_1 \)

**DWT-based Search**

- mem#0
- mem#1
- mem#2
- mem#3

- \( R^{(0)} \)
- \( T^{(0)} \)
- \( T^{(1)} \)
- \( T' \)

Not Used
Experimental Results

<table>
<thead>
<tr>
<th>Algorithm Name</th>
<th>Computing Time (s)</th>
<th>Resource Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( \mu P )</td>
<td>Cray XD1</td>
</tr>
<tr>
<td>Exhaustive Search</td>
<td>157.347</td>
<td>16.193</td>
</tr>
<tr>
<td>DWT-based Search</td>
<td>1.298</td>
<td>0.829</td>
</tr>
</tbody>
</table>

- The reference and test image are both 1024\( \times \)1024 pixels and in 8-bit gray-scale
- The search spaces of \( \Delta \Theta, \Delta X \) and \( \Delta Y \) are all from -8 to +8
- Three levels of DWT decomposition, which is based on LL coefficients, are performed in the DWT-based search
- The referenced \( \mu P \) is AMD Opteron 2.4 GHz
- The hardware computation time is end-to-end time
  - Data transportation time + data processing time
- The hardware implementation was developed using Verilog HDL and VHDL; Xilinx ISE 8.1 was used for synthesis and p&r
Outline

1 Background
   - High Performance Reconfigurable Computer (HPRC)
   - Image Registration

2 Image Registration Using Hardware
   - Exhaustive Search Algorithm
   - Discrete Wavelet Transform (DWT)-based Search Algorithm

3 Implementation and Results

4 Conclusions
Two related image registration algorithms based on rigid-body transformation are presented

- For exhaustive search algorithm, the performance is linearly proportional to the available number of local memory banks.
- For DWT-based search algorithm, the efficiency is improved by applying DWT decomposition on both reference and test images to reduce the search scope.

Compared to software implementation on AMD Opteron 2.4 GHz, experimental results on Cray XD1 show:

- Exhaustive search algorithm: 10× speedup
- DWT-based search algorithm: 2× speedup

Can be improved further by increasing the parallelism in hardware implementation.