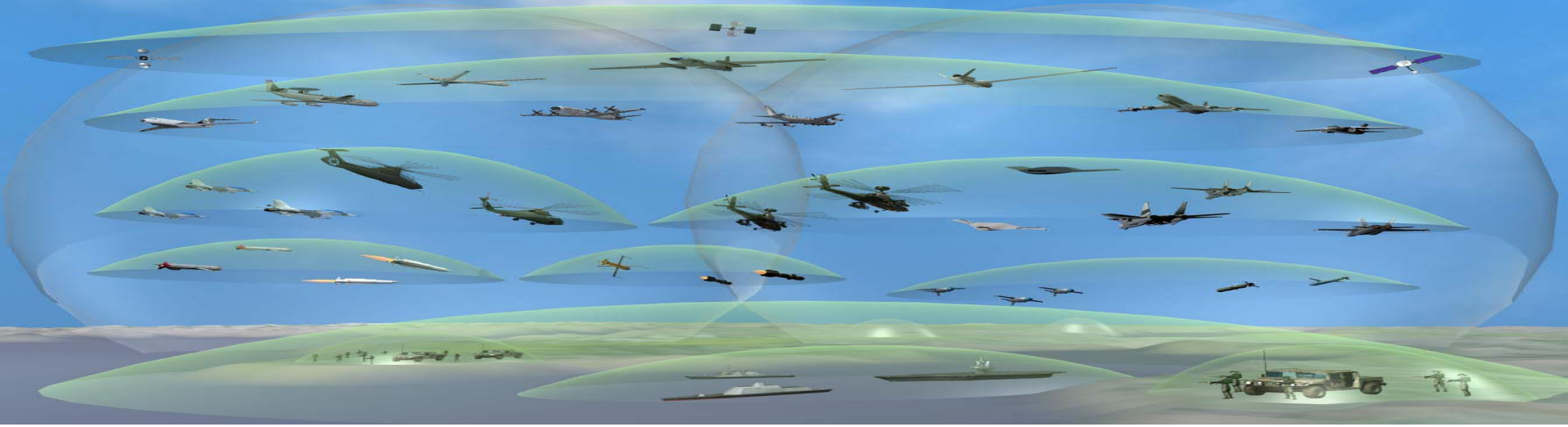

Secure SDR in Space

Architectural Considerations

MAPLD, September 16, 2008

Session A

Ian Land – Xilinx, Inc
John Corbett – Xilinx, Inc.
David Buechner – ImpulseC
Paul Murray – SEAKR Engineering

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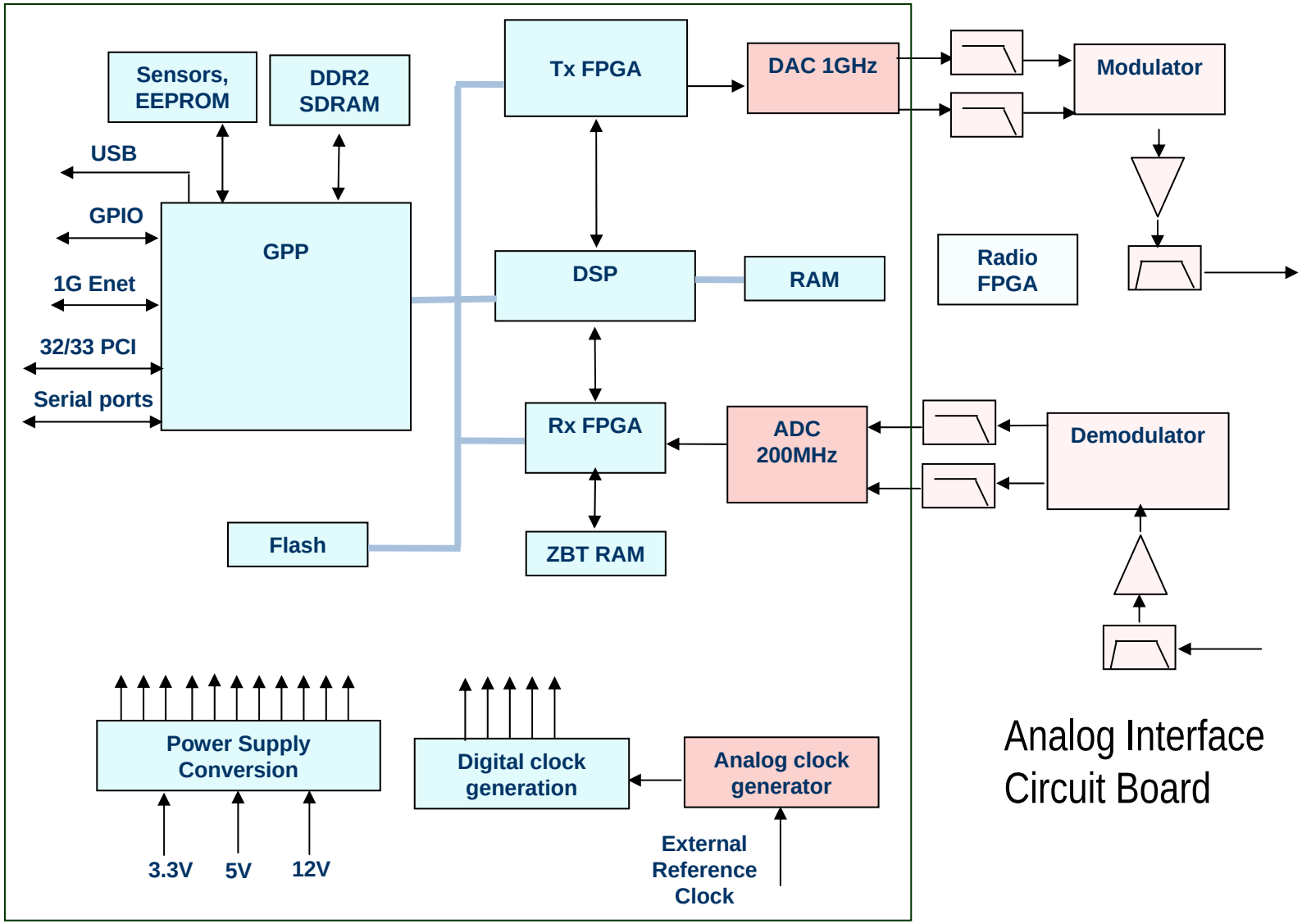
Rationale

- Why Space and why secure?
  - Every satellite needs to communicate
  - Radio-based communication can be intercepted
- Why use an FPGA?
  - Reconfigurable design
  - Parallel processing: increase performance/lower power
  - Accelerate via logic gates next to processor
  - Self-contained, high-integration, partitioned HW & SW

Radio Modem (component)



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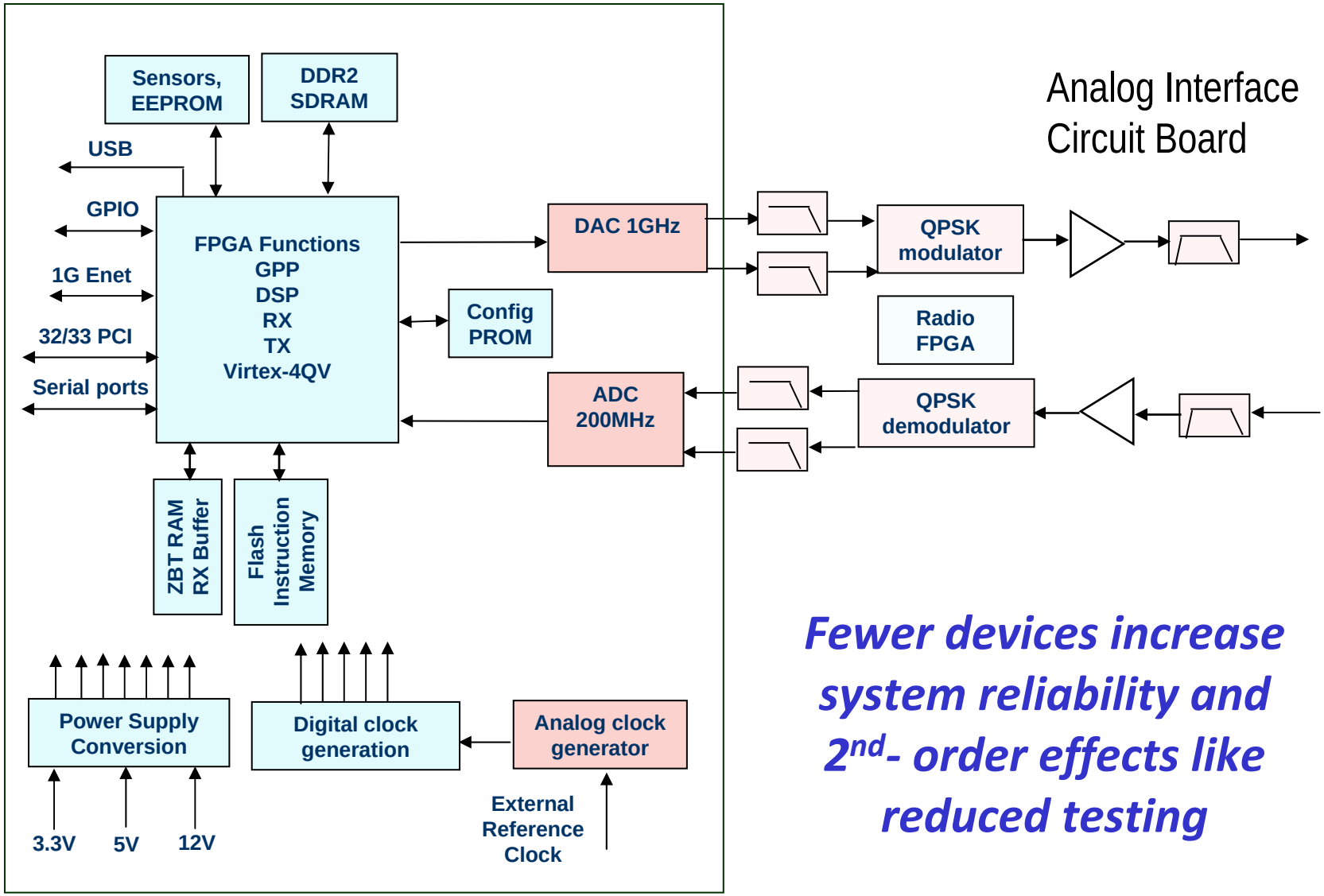
SDR Modem (integrated)



Fewer devices increase system reliability and 2nd- order effects like reduced testing

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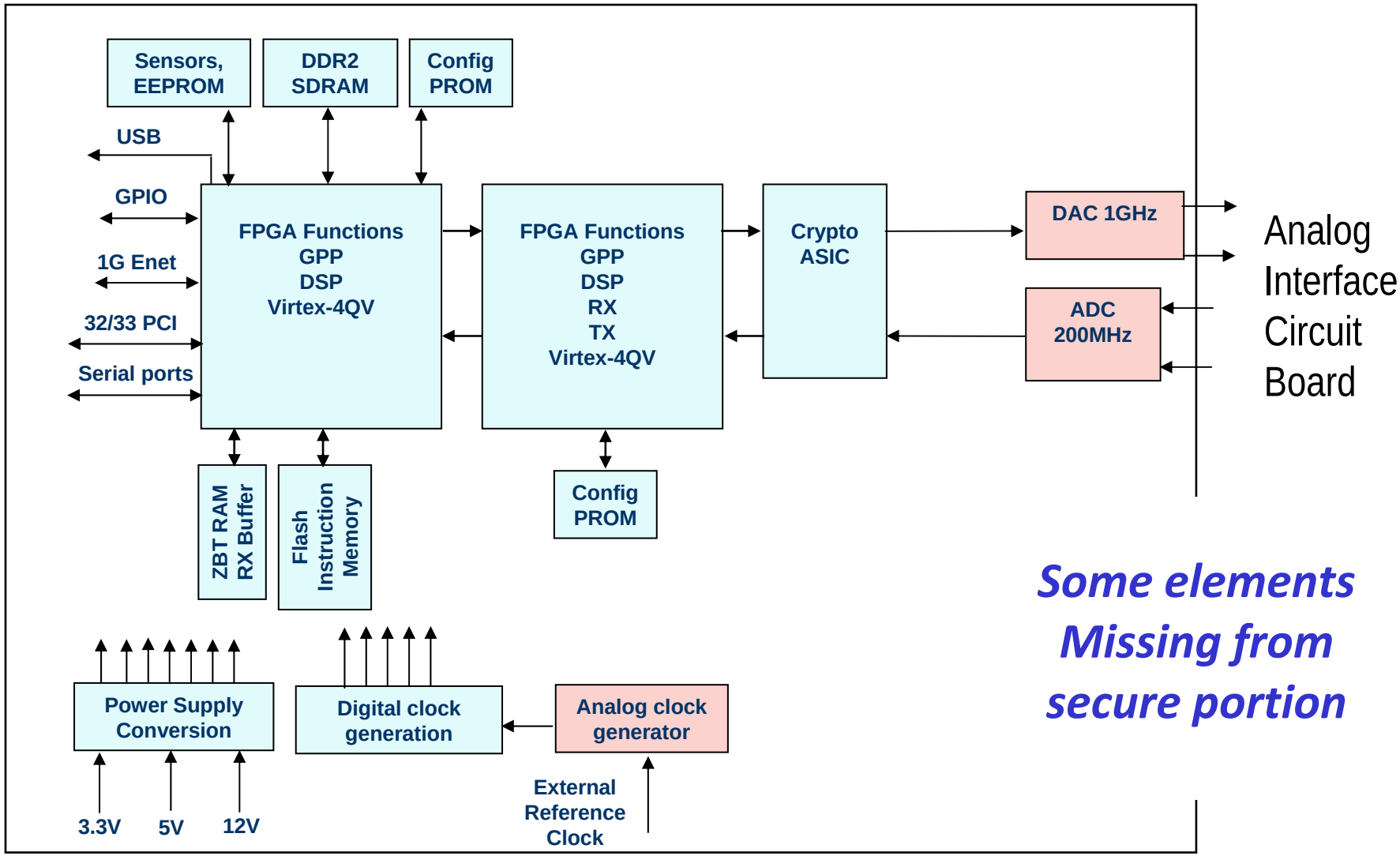
Secure SDR Modem



Some elements Missing from secure portion

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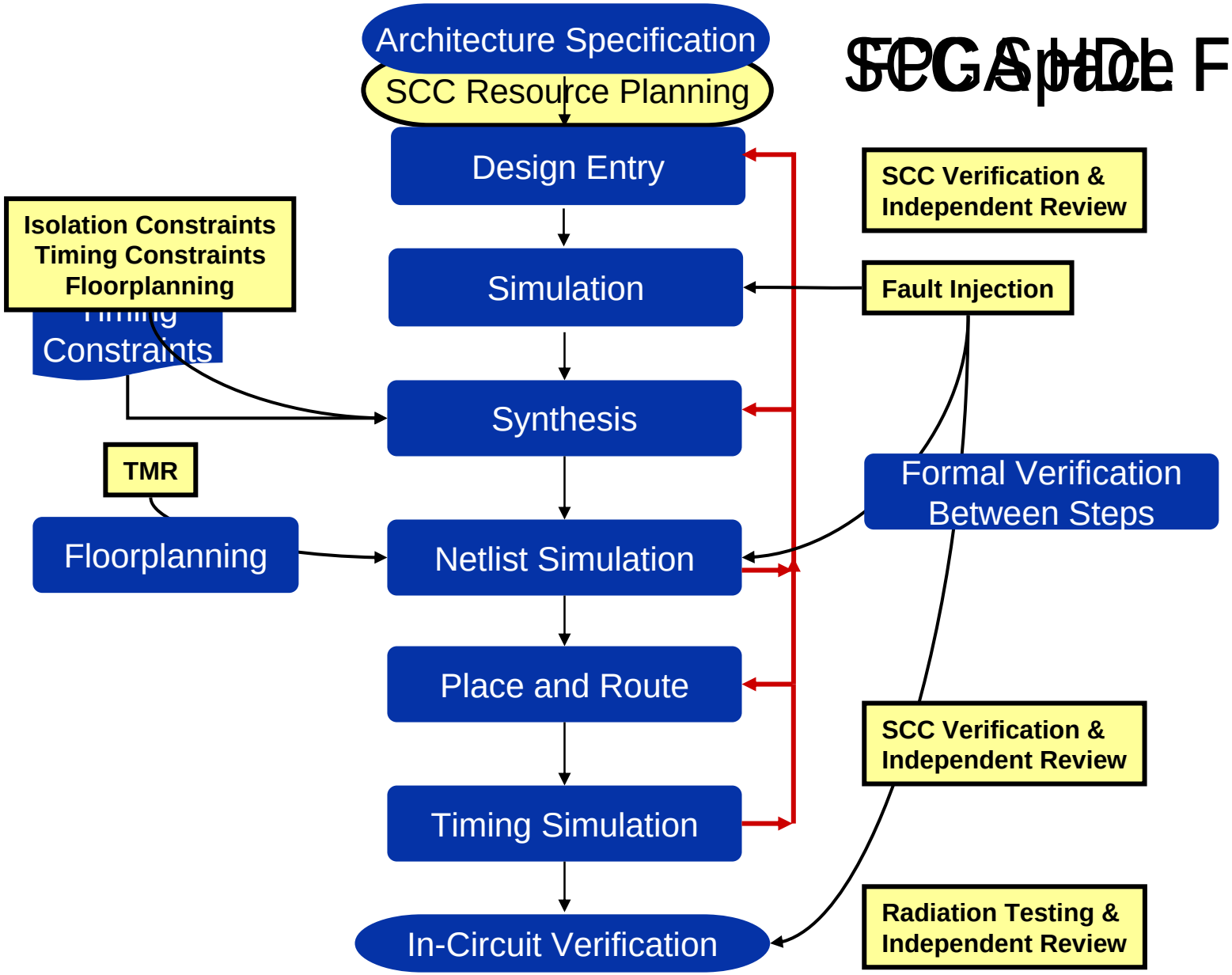
SCC Space Flow



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Secure Considerations

- Secure tool flow leverages partial reconfiguration (PR)
  - Provides low-level routing control with ease
  - PR enables algorithm agility (replacing modules)
    - Swap out algorithms or update portions of the device while in service
    - Static portion controls reconfiguration of other regions
  - PR provides a base level of isolation naturally
  - Isolation Verification Tool confirms section isolation
- Secure designs should have
  - Meet US Government Fail Safe Design (FSDA) Criteria
  - Plaintext (Red) and ciphertext (Black) separation
  - Support Multiple Independent Levels of Security
  - Capable of Type-I Algorithms
  - Avoid attacks on ground and hacks in flight

Space Considerations

- All semiconductors are susceptible to radiation effects
  - Destructive or non-destructive
- Virtex-4QV response to radiation is non-destructive
  - >300 KRad TID, SEL Immune
  - SEU resistant with adequate mitigation, orbit dependent
- Mitigation: TMR & Error correction
  - Implementing TMR gives correct operation in spite of an upset or transient in either configuration memory or user resources
  - Constant monitoring & configuration scrubbing fixes upsets
  - Adding SEFI detection allows quick reconfiguration => availability
  - Together they lower the system error rate (appendix)

Secure in Space Challenge

Space & Secure need partial reconfiguration and are complex

- Space uses PR for scrubbing of configuration memory
- Secure uses PR for routing and containment

Secure SDR in Space

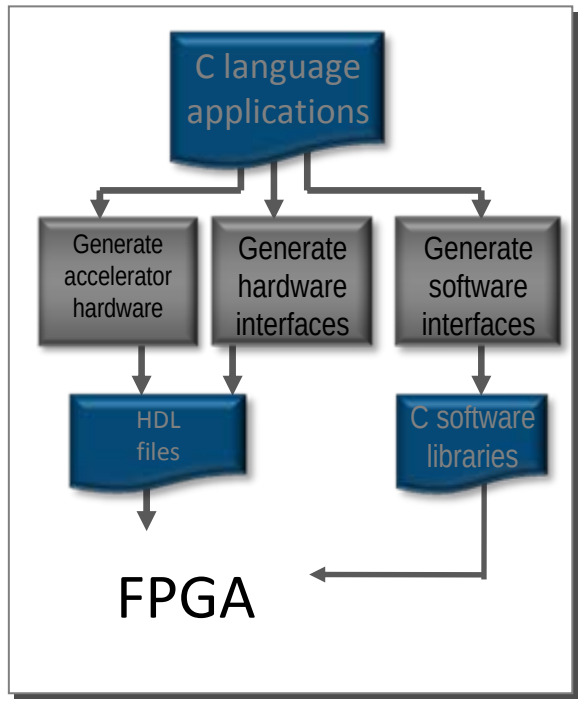
- Both need PR and would require tool flow changes
- The Secure/Space combination is not yet Xilinx sponsored
  - Possible solution: component-level triplication of secure design

We do have customers already undertaking this task

- SEAKR is highlighted here demonstrating SDR in Space
- At least a few are doing Secure SDR in Space

Partitioning from C to HW & SW

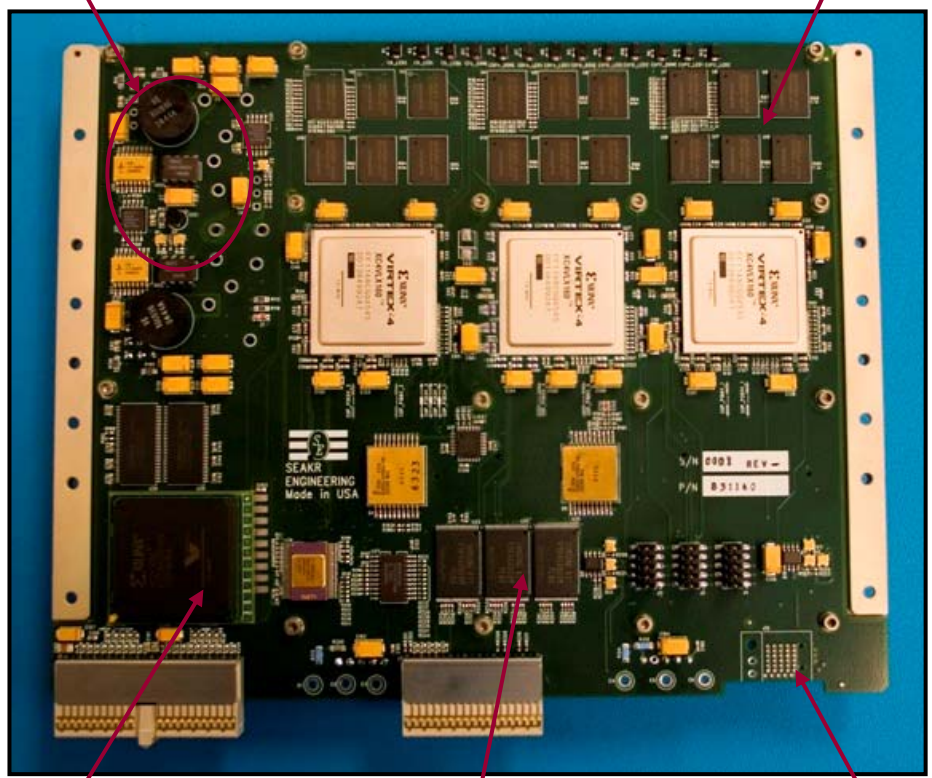
- Most signal processing code in C
- New way to partition from C to FPGA
  - Engineers start with standard C
  - Impulse builds HW interfaces & HDL
  - Engineers partition some C to HW
  - Engineers partition C as SW on MPU
  - Impulse generates SW interfaces
- Results
  - C-based SW libraries, & HDL (VHDL / Verilog)
  - Portable, reusable libraries and files



Courtesy of ImpulseC

Flight-ready Integrated SDR

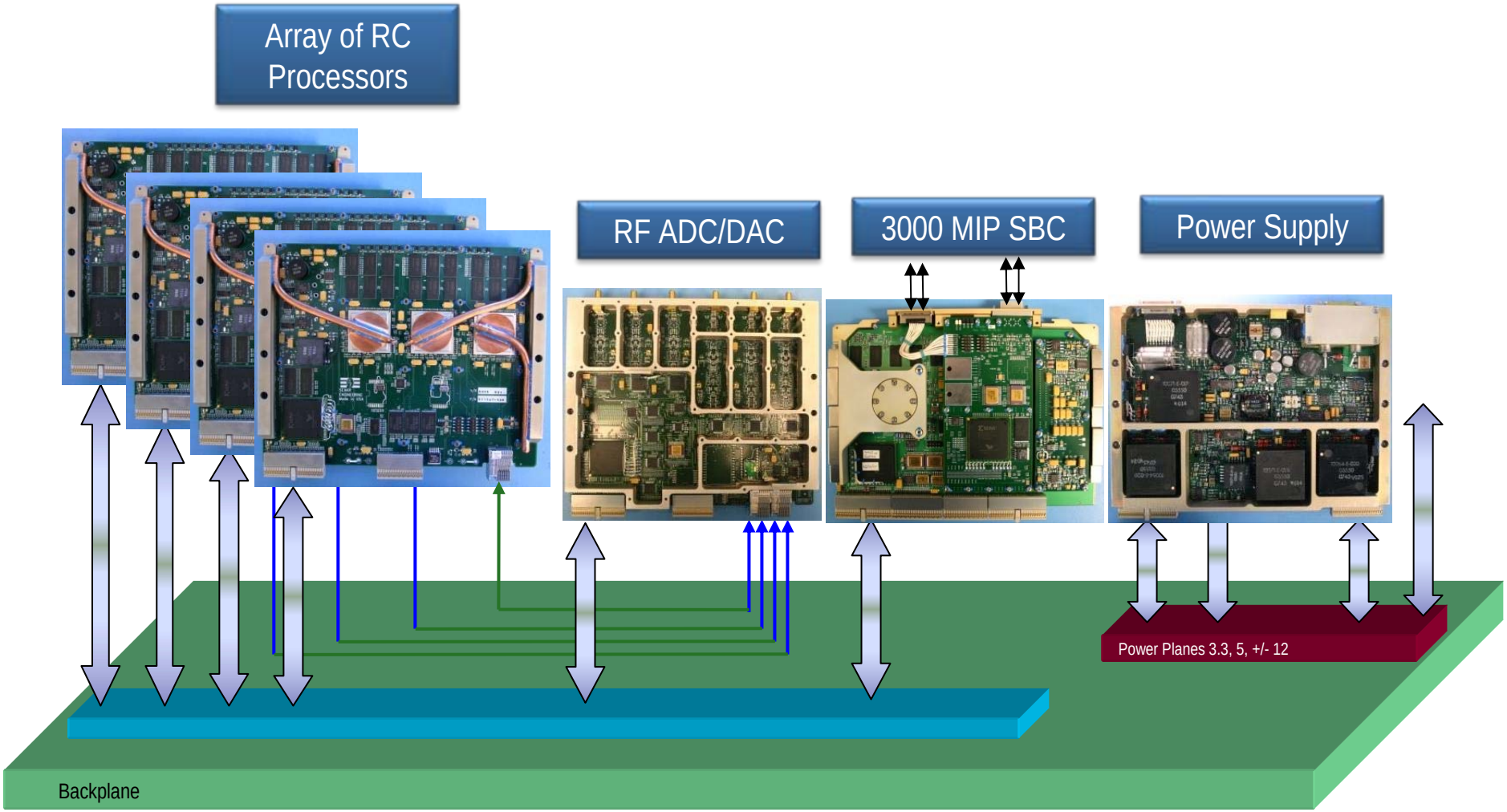
- 3 Virtex-4 FPGAs
- TID >40krad; higher options
- 256 MBytes DDRII SDRAM x 3
- 170 user defined I/O per FPGA
- Extended 6U cPCI
- Symmetrical Design
- 62 stored configuration files
- Device-level TMR with external majority voting
- Autonomous FPGA scrubbing
  - With SEFI protection & recovery
- High Speed Serial Backplane I/F
- 2.6 lbs; 9.2 x 7.3 x 1.43”



Courtesy of SEAKR Engineering

SDR with Packet Processing

A System Level View



Courtesy of SEAKR Engineering

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Conclusion

- Nearly all space applications need radio communication
  - And, many programs require secure communications
- SDR enabled by large-density, high-performance FPGAs
  - Look for government-evaluated devices with multiple, independent levels of security and regional isolation
  - Reconfigurable devices have benefits for C to FPGA users
- Secure SDR in Space
  - It requires strong user effort and knowledge
  - It can be board-level or FPGA-level (very cutting edge)
  - It can increase reliability due to fewer devices
- The future is secure, single-chip, radio processing