Reconfigurable, High Density, High Speed, Low Power, Radiation Hardened FPGA Technology

MAPLD2008

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Agenda

- RH FPGA Roadmap
- RH FPGA Product Features
- Achronix Technology Overview
- BAE Radiation Hardened Process Technology Overview
- Program Status / Summary
Radiation Hardened FPGA Roadmap

Past
- Heritage: Actel ONO RH1280 and RH1020
  - Anti-fuse technology, non-volatile
  - 0.8µm RH CMOS, 5V Supply
  - In production since 1996, over 25,000 shipped

Present
- M2M Anti-fuse Technology:
  - 250K-gate (RHAX250-S)
  - RH15 CMOS, 1.5V Core / 3.3V I/O
  - Flight Orders in 2009

Future
- ≥3M-gate, re-configurable, non-volatile
- Radiation Hardened, high speed
- RH15 CMOS, 1.5V Core / 3.3V I/O
- Projected qualification starts in 2009
RHFPGA Product Features

- TID tolerance of > 1Mrad Si
- SEU immunity < $10^{-11}$ errors/bit-day
- System speeds > 300MHz
- Support of RADHARD IOs and RAMs for integration into Systems
- Reconfigurable/Reprogrammable
- Low Power
- Extreme Temperature Operation
- Non Volatile
- EMP Protected
- Full Compatibility with Existing EDA Tools
- Product Name -> Radrunner
Achronix Company Overview

- Privately held fabless semiconductor company founded in New York in 2004
- Achronix has received $34.4M Series A funding
- Founders developed technology in 1998 at Cornell University
- Headquartered in San Jose, CA
- Working 90 and 180 nm prototype silicon
- Partnerships with the world leading foundry TSMC, BAE Systems and numerous IP & EDA vendors
- 65 nm commercial FPGA silicon has been received from TSMC; currently shipping
- All Key IP’s protected by patents
Reconfigurable RH FPGA Proof of Concept

Key Roles to support Reconfigurable RH FPGA Proof of Concept:

**Achronix:**
- Product Design
- Architecture Definition
- Reprogrammable Fabric, S-Frame
- Incorporate BAE RHSRAM
- Final Design & Simulation
- Product Testing Support
- Sales and Marketing

**BAE:**
- Design Custom Blocks
- Physical Design/Integration
- Wafer Processing/Characterization
- Wafer Sort and Packaging Tests
  - Packaging
  - Radiation Testing

POC Ready
Option for QML Qualification
Commence Enhancement of the FPGA

ACX RH FPGA Product Development…. A collaborative effort
Achronix RH FPGA Technology
Achronix Core Technology

- Core contains ‘picoPIPE’ technology used for both logic and routing
  - You do not need to know the details in order to benefit from this
- Fully synchronous I/O ‘frame’ surrounds the core
- picoPIPE technology is used to implement synchronous hardware
  - A design is input using a HDL such as RTL
  - The RTL does not need to be targeted to picoPIPE technology

Looks like a regular FPGA, but has approx 4x throughput
Data Tokens

Traditional FPGA

- In globally-clocked logic, a data value at a clock edge can be considered as a “Data Token”
  - Only valid data (data at a clock edge) is propagated
  - Hence each register output’s a new Data Token (value) at every clock edge

Achronix FPGA

- picoPIPE logic also contains Data Tokens
  - Each data token uses 2 signals instead of 1
  - Data validation (clock-like functionality) is performed using acknowledge instead of a global clock
More on Throughput

**Traditional FPGA**
- Globally Clocked Logic is not balanced
- The clock rate must allow for the slowest path in the entire clock domain
- Any combinatorial logic faster than the slowest path (by definition, all remaining logic) waits for the slowest one to finish

**Achronix FPGA**
- Achronix technology allows fine-grained pipelining
- Allows data rate to be much faster
- Pipelining also allows more data values in flight
- Equates to faster throughput

**Globally-clocked Logic**

<table>
<thead>
<tr>
<th>0ps</th>
<th>.67ns</th>
<th>1.3ns</th>
<th>2.0ns</th>
<th>2.7ns</th>
<th>3.3ns</th>
<th>4ns</th>
<th>4.7ns</th>
<th>5.3ns</th>
<th>6ns</th>
<th>6.7ns</th>
<th>7.3ns</th>
<th>8ns</th>
<th>8.7ns</th>
<th>9.3ns</th>
<th>10ns</th>
<th>10.7ns</th>
</tr>
</thead>
</table>

**picoPIPE Logic**

**BAE SYSTEMS**

**Achronix SEMICONDUCTOR CORPORATION**
Familiar Silicon & Familiar Tools

- Traditional 4-input LUT architecture
  - With GHz performance
- SRAM-based reprogrammable FPGA
  - Uses BAE’s Radiation Hardened SRAM cell

- Synplify-Pro and Mentor Precision Synthesis Flows
- Full compatibility with existing third party simulation, debug, and verification tools
Trading off Speed for Power Dissipation: V^2f

- **Supply Voltage**: 97% less @ 0.6V → 250 MHz
- **Operating Power**: 78% less @ 0.8V → 1 GHz
- **Nominal**: 1.2V → 2 GHz

The robustness properties of the Achronix picoPIPE technology allow it to operate reliably over both a wide Voltage and Temperature range!
Achronix Patented SEE Mitigation Methodology: Redundancy Voting Circuits (RVC)

• **Redundancy Voting Circuits (RVC)**
  – Two copies of all circuits are implemented
  – Copies are non-adjacent to avoid the risk of a single upset affecting both
  – Every stage (combinatorial and state) has local voting mechanism

• **Local voting waits until both copies agree**
  – no SEE, values will agree at the voter, tokens propagate
  – When SEE occurs values won’t agree at voter, local voter **blocks** token propagation
  – After event energy dissipates the upset circuit value is resolved to the correct value and tokens propagate
**RVC Proof of Concept Test Chip**

- Radiation Hardened By Design (RHBD) circuit techniques portable to any foundry to enable **extremely** low SEU and SET rates (< $10^{-11}$ upsets/bit day)
  - Circuit technique proven thru SEE testing at 150 nm applicable to any process node

<table>
<thead>
<tr>
<th>Proof of Concept Vehicle</th>
<th>150 nm BAE Systems test chips</th>
</tr>
</thead>
<tbody>
<tr>
<td>Where</td>
<td>Cyclotron Institute</td>
</tr>
<tr>
<td>Who</td>
<td>NASA Electronic Parts and Packaging Program</td>
</tr>
<tr>
<td>Result</td>
<td>No observed SET or SEU events in SEE testing up to a LET threshold of 55 MeV-cm²/mg</td>
</tr>
</tbody>
</table>
Defined goal of initial radiation test was to prove that tokens continue to propagate in the event of heavy ion impact.

Test Chip contained a 4x4 array of FPGA Tiles implemented with RVC picoPIPE elements.

One dedicated tile had an 8 bit counter (implemented in RVC) on output acknowledge to observe the functioning of the various FPGA configurations at a reasonable frequency with standard I/O.

Five different FPGA patterns utilized during testing.
Summary: Heavy Ion SEE Test of BAE-Achronix Rad-Hard FPGA Test Chip

- Testing completed by NASA at Texas A&M University Cyclotron Single Event Effects Test Facility (SEETF)
  - **Test Date:** August 14th, 2007
  - **Sample size:** Three devices tested including one control not exposed to the radiation source
  - **Flux:** $1 \times 10^3$ to $1 \times 10^4$ particles/cm$^2$/s
  - **Fluence:** $5 \times 10^6$ particles/cm$^2$
  - **Test Angles:** Normal, 45 degree

- **SEL Analysis**
  - No SEL observed through tests with temperatures up to 74 °C and LET of 55 MeV*cm$^2$/mg

- **SEE Data and Analysis**
  - No SEFI observed for all tests run
  - Tokens continued to propagate throughout testing
BAE RH FPGA Process Technology
# RH FPGA Technology (RH15F) Features

## Key Features

<table>
<thead>
<tr>
<th>Features</th>
<th>RH15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation</td>
<td>STI</td>
</tr>
<tr>
<td>Thin Oxide / DGO Devices</td>
<td>26 Å / 70 Å</td>
</tr>
<tr>
<td>Vdd Options</td>
<td>1.5 V / 1.8 V / 3.3 V</td>
</tr>
<tr>
<td>Metal Levels</td>
<td>7</td>
</tr>
<tr>
<td>Capacitors</td>
<td>Yes</td>
</tr>
<tr>
<td>Resistors</td>
<td>Yes</td>
</tr>
<tr>
<td>C4 / Wirebond</td>
<td>Y/Y</td>
</tr>
</tbody>
</table>

## Radiation Hardness Assurance Levels

<table>
<thead>
<tr>
<th>Environment</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dose (rad(Si))</td>
<td>1M</td>
</tr>
<tr>
<td>SEU (errors/bit-day)</td>
<td>1E-11</td>
</tr>
<tr>
<td>SEL (MeV-cm²/mg)</td>
<td>120</td>
</tr>
<tr>
<td>Neutron Fluence (n/cm²)</td>
<td>1E13</td>
</tr>
<tr>
<td>Prompt Dose Upset (rad(Si)/s)</td>
<td>1E9</td>
</tr>
<tr>
<td>Prompt Dose Survival (rad(Si)/s)</td>
<td>1E12</td>
</tr>
</tbody>
</table>
### 16M SRAM – Next-Generation Strategic RH SRAM

<table>
<thead>
<tr>
<th>Access Time</th>
<th>15-20 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process Technology</strong></td>
<td>0.15 µm CMOS</td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>16 mm by 16 mm</td>
</tr>
</tbody>
</table>
| **Power Supply**    | 1.5 V + / - 10% core  
                      | 2.5 or 3.3 V + / - 10% I/O |
| **Power Dissipation** | 10 mW/MHz at 1.5V (per die)  
                         | 100 mW standby |
| **Temperature Range** | -55°C to +125°C |
| **Packaging**       | 23.2 mm by 26.2 mm by 6.0 mm  
                      | 100 pin Flat Pack (5-high stack) |
| **Radiation Hardness** | Total Ionizing Dose > 1Mrad(Si)  
                          | Prompt Dose > 1E9 rad(Si)/sec  
                          | SEU < 1E-12 errors / bit-day (W.C. 90% GEO)  
                          | Latchup: Immune |
| **ESD**             | TBD |
| **Screening level** | Prototype and Flight flows |
| **Organization**    | 2Mx8 die – single chip package  
                      | 2Mx32 4-high package  
                      | 2Mx40 5-high package  
                      | 512Kx32 die – single chip package |

#### Configuration Memory Cell for RH FPGA uses the 16M SRAM Cell
Standby mode – periodic reads

No Proton Upsets
No Latchup

Background 6e-16 u/b-d; Solar Flare 4e-13 u/b-d

SEU for Memory Cell Exceeds RH FPGA SEU Targets
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
<th>Goal</th>
<th>Achieved</th>
<th>Outlook</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Speed - worst case 125C and post radiation</td>
<td>≤ 20 ns</td>
<td>≤ 15 ns</td>
<td>≤ 15 ns</td>
<td>G</td>
</tr>
<tr>
<td>Operating Temperature Range Full Performance Functionality</td>
<td>0 to 80C -55C to 125C</td>
<td>-55C to 125C Same</td>
<td>-55C to 125C</td>
<td>G</td>
</tr>
<tr>
<td>Standby Current - worst case 125C and post radiation</td>
<td>≤ 60 mA</td>
<td>≤ 40 mA</td>
<td>≤ 40 mA</td>
<td>G</td>
</tr>
<tr>
<td>SEU (upsets/bit-day)</td>
<td>&lt; 1E-10</td>
<td>&lt; 1E-11</td>
<td>&lt; 1E-12</td>
<td>G</td>
</tr>
<tr>
<td>Total Ionizing Dose - Gamma</td>
<td>≥ 0.5 Mrad</td>
<td>≥ 1 Mrad</td>
<td>≥ 1 Mrad</td>
<td>G</td>
</tr>
<tr>
<td>Prompt Dose Upset (rad/sec)</td>
<td>≥ 1E9</td>
<td>≥ 1E9</td>
<td>Planned on 5-high stacks</td>
<td>G</td>
</tr>
<tr>
<td>Survivability (rad/sec)</td>
<td>1E12</td>
<td>1E12</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Characterization complete  
Qualification in progress, Prototypes Samples Available
RHFPGA Package Definition

- Substrate—ceramic 32 mm x 32 mm
- 32 mm x 32 mm Column Grid Array
  - 1.27 mm pitch
  - 624 Total I/O
- Capacitors
  - Sizing suggests 16 Low Inductance Flip Chip Capacitor Sites
  - Can be used to support several different voltages
- Hermetic Seam Weld Sealing
### RHFPGA Preliminary Engineering Estimate of Part Resources

#### Radrunner Family (150 nm)

<table>
<thead>
<tr>
<th>Device Resources</th>
<th>RDR500</th>
<th>RDR1000</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device Name</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LUT</td>
<td>4,320</td>
<td>8,640</td>
</tr>
<tr>
<td>Number of 18 Kbit Block RAM</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Block RAM (Kbit)</td>
<td>90</td>
<td>180</td>
</tr>
<tr>
<td>Number of PLL</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>SpaceWire Interfaces</td>
<td>4</td>
<td>7</td>
</tr>
<tr>
<td>User Programmable I/O</td>
<td>336</td>
<td>384</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCGA624 (32 mm x 32 mm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CQ340</td>
<td>286</td>
<td></td>
</tr>
</tbody>
</table>

Design under optimization to maximize RHFPGA Resources
SUMMARY

- Program Fulfills Critical Need for Reconfigurable RH FPGAs for Strategic Applications
- Excellent Partnership between BAE Systems and Achronix Ongoing
- Initial Achronix Commercial Chip First Pass Success
- Test Chip Functionality Demonstrated, Radiation Testing Successful
- Design Activities Continuing with No Technical Concerns
- Plans In Place for Further Device Enhancements

Program Outlook Overall Positive for Initial POC Device 2Q09