SpaceCube: A Reconfigurable Processing Platform for Space

by Gordon Seagrave

SpaceCube Chief Architect / Inventor

Gordon@gordonicus.com

Gordonicus LLC
Design Goals

Maximum Computing Power
Reconfigurable
Radiation Safe

Flexible Architecture – Stackable
Minimum Power – Under 10 Watts
Minimum Size – 4in x 4in x 4in Cube System
Minimum Cost – $40K + $35K Flight Boards
Minimum Weight – System is less than 4 Lbs.

TRL Level 8 - TRL Level 9 (Hubble Mission STS125)
Processing Architecture: SEU Immune and SEU Susceptible Areas

**SEU Susceptible**
- 4 x 450 MHz PowerPC™ 405
- TID 250 krad (Si)
- SEL 100 LET (MeV-cm²/mg)
- SEFI 1.5 E-6 Upsets / device / day

**SEU Immune**
- Fuse array
- TID 300 krad (Si)
- SEL Immune >120 (MeV-cm²/mg)
The SpaceCube architecture is based around four PowerPC 405 microprocessors which are embedded into a reconfigurable FPGA fabric.
PPC405 Supported Operating Systems

• VxWORKS
• BlueCat Linux
• RTEMS

Mixed operating system scheme supported
SEU Immune Architecture

- Comprised of dual Aeroflex FPGAs.
- Operated by the Instantiated SpaceRISC 8 bit Microcontroller having an instruction set compatible with the PIC16F86
- Loads/re-configures the PowerPC code or Xilinx node fabric from redundant FLASH
- I2C inter-module communication controller via stacking connector
Processor Board Dataflow

Node 1 = QUAD 1
- IBM PowerPC405
- 450MHz
- 128M x 16 SDRAM
- 256MB

Node 2 = QUAD 2
- IBM PowerPC405
- 450MHz
- 128M x 16 SDRAM
- 256MB

Node 3 = QUAD 3
- IBM PowerPC405
- 450MHz
- 128M x 16 SDRAM
- 256MB

Node 4 = QUAD 4
- IBM PowerPC405
- 450MHz
- 128M x 16 SDRAM
- 256MB

External Connectors
- 8 SpaceWire Ports or 16 LVDS / RS422

Internal Stacking Connector
- 8 SpaceWire Ports or 16 LVDS / RS422

Xilinx V4 FX60
- Radiation Immune RISC Microcontroller
- 512MB FLASH
- 32kB RAM
- 32kB PROM
- 3DPlus

Data Validation
- ISC Microcontroller
- Housekeeping

512MB FLASH
- SDPlus

32kB RAM
- SDPlus

32kB PROM
- SDPlus
Data Flow In

SpaceCube architecture uses a “shared via” approach which provides the same inputs to each of the SpaceCubes four processing nodes. These nodes are physically separated to provide maximum protection from multi-bit single event upsets (SEUs).
Intra Node Communication

The Quads have high speed cross-channel links via reconfigurable fabric.
Data Validation: Quad redundancy mode

The PPCs may be configured for Quad redundancy processing where the outputs are voted.

A small, radiation hardened, microcontroller provides the synchronization to allow for voting in this multiprocessor system when operating in the quadruple mode redundancy approach.
The **PPCs** may act as 4 unique engines performing 4 unique tasks where the outputs are not voted.
SEU Immune Functions

- Initialization and reconfiguration of the Xilinx processing nodes
- Data voting and validation
- Monitors, controls and communicates with PowerPCs, node logic and Xilinx self-scrubbing.
- Module communication via the stacking connector
- Monitoring of Xilinx Self-Scrubbing
- Routing Processed data
- Access to FLASH memory
- System Debug Ports
- Intra Module Communication
RISC Microcontroller Housekeeping

Each Xilinx Virtex 4 houses (2) PPCs.

Xilinx FPGAs are monitored, programmed and synchronized by a RISC microcontroller in the Aeroflex FPGA.

The Xilinx FPGAs implement self-scrubbing, monitored by the RISC Microcontroller.
SpaceCube Node Partial or Full Reconfiguration

A Single Node can be reconfigured with:
- PPC Operating system
- PPC application code or
- Xilinx fabric reconfiguration

WITHOUT disruption to the other nodes

New sources are stored in FLASH and loaded via the RISC microcontroller.
RISC Microcontroller Software Modification

- After reset, ROM is loaded into RAM
- Processor boots from top half of RAM
- Software looks to FLASH for updates
- Loads updates into bottom half of RAM
- Processor jumps to bottom half of RAM
- New code patches can be received via uplink

New RISC Microcontroller software is loaded into a specific section of RAM
Stacking Connector Interface
4 x 4 inch Processor Board
STACKING CONNECTOR SIGNALS

- Slice to Slice communications are handled via a combination of configurable high and low speed serial links.
  - Redundant I2C Busses (400 Kb/S) provide for low speed command and telemetry functions
  - High Speed LVDM busses such as Ethernet or SpaceWire provide for high speed communications (125Mb/s – 250 Mb/s per bus)
- 8 high speed busses and two low speed busses on the stack.
- I2C Communication is from hard microcontroller to hard microcontroller for critical functions
Stacked Architecture Allows Endless Flexibility

• SpaceCube uses a stacked architecture composed of cards or “slices” connected via a connector running the length of the stack.

• Slices can be made redundant and the stacking architecture allows any slice to communicate with any other slice – thus allowing card level redundancy.

• Custom Slices Stack onto the SpaceCube Processor and LVPS Slices.

• Small card size (4x4 inches) means mass is minimal. (<2Kg for minimum configuration)
Stackable Architecture

- SpaceCube uses a stacked architecture composed of cards or “slices” connected via a connector running the length of the stack.
- Slices can be made redundant and the stacking architecture allows any slice to communicate with any other slice – thus allowing card level redundancy.
- Each slice has an individual enclosure which encloses it on 5 sides.
- Slices are stacked in whatever order desired and covered by a top plate.
- Up to two Power slices can be combined in a stack (one on the top, one on the bottom) to allow for a complete “warm back-up” system.

Minimum Configuration = 4 x 4 x 3 inches

- Scup
- LVPC

Gordonicus LLC
SpaceCube Packaging
Processor Slice and CCA

- Designed per IPC-2222 and Fabricated per IPC-6012
- Multi-layer (18 layers) board material construction per IPC-4101
- PWB, 2098673, size 4.00W x 4.00L x .093T (inch)
  (Polyimide-glass laminate)
- Up to 2 oz top & bottom, and internal signal & ground planes utilized for thermal management of components.
- Maximum component heights: 0.79 inch (primary side), and 0.21 inch (secondary side)
- External interface thru two MIL-DTL-83518 (Micro-D) connectors
- The Processor board is supported by 2 stiffeners and 2 integral stand-offs.

Gordonicus LLC
SpaceCube Packaging
Power Slice Assembly
(contains DCC and LVPC Boards)
Power Slice Functions

- Redundant 1553
- 8 analog inputs
- 10 Mb Ethernet
- Redundant I2C for intra-module communication
- Power Supply Monitoring
- Power on/off functions
- Provides power to other modules
- 28 V power input
Power Slice

DCC Level Block Diagram

- Reference Voltage
  - 2.0V
- 28V to 12V Power Converter
  - +28V
- Oscillator
- Stacking Connector
- Stack I/O Mil-1553 Ethernet DCC
  - Power Reset Power Warning All Power
- Aeroflex UT6325 484 CGA
- Analog Multiplexer HS9-508BRH 8 to 1
- Analog Multiplexer HS9-508BRH 8 to 1
- Voltage Scaling
- Thermistor +9V +3.3V +2.5V +1.5V +12V +12V +2.5V REF
- 3 analog inputs (spare) N/C
- 5 analog inputs (0V - 5V)
- RS-422 Transmitter 8 wires
- RS-422 Receiver 8 wires
- RS-422 Transmitter 8 wires
- RS-422 Receiver 8 wires
- LVDM Transceiver
- Ethernet Transformer
- MIL-STD-1553B Transceiver
- MIL-STD-1553B Transformer

J1 51 Pin MDM Connector

SpaceCube LVPC Digital

J2 20 Signal Pin + 4 Power Pin Hybrid Connector

Gordonicus LLC
STS125 Mission SpaceCube

Total Weight: 7.3 lbs
Dimensions: 5.58W x 7.03L x 4.60H (inch)

SLICE STACK UP
POWER 1
PROCESSOR 1
VIM
PROCESSOR 2
POWER 2
RNS SpaceCube Stacks
SpaceCube Software Loads for RNS

SCuP#1
- C&DH#1
- NFIR
- ULTOR

SCuP#2
- C&DH#2
- AGC
- GPS
- Ku-Band Downlink

Tim Module
- MSM 1
- MSM 2
- GPS
- Ku

250 Kbps UART (cmd)
- RS-644 data strobe
- 1 Mbps bi-Φ

250 Kbps UART (data)
NFIR Algorithm Description

- Model – effectively a wire frame delineating the coordinates of vehicle (HST) features expected to be ‘readily recognizable’ in the video images.

- ‘Readily recognizable’ implies detectable through use of an edge detection algorithm under the expected lighting conditions.

- NFIR uses the Pose, model points (3D), matched image points (2D) to estimate the motion between frames. This motion is applied to the Pose to obtain the estimated Pose.
MSM Commands are received from the TLM interface. Each PowerPC receives the command and processes it. The MSM command is then queued up in a FIFO. When each PowerPC has placed the command in the FIFO, the PIC starts the voting process.
SpaceCube on Shuttle Mule
Implementation of Space Cube within a Rover

- Low Voltage Power Converter & Discretes
- Reconfigurable Logic
- C&DH & Nav Processor
- Comm. Interface
- Power Electronics
- Battery
- Power Services
- Un-switched Power Services
- Heaters
- Two high speed 100 Mbps links / Two low speed 400 Kbps links
- Redundant Serial busses
- Firewire (1394a)
- Ethernet/Spacewire
- MIL-STD-1553
- Simulated RF Com Interfaces (Ethernet)
- CMD and TLM Lines
- Sensors
- Actuators
- Additional Hardware (per Rover Specification)
- ITOS / ASIST
- Navigation Cameras
- Slice #1
- Slice #2
- Slice #3

Gordonicus LLC
NASA Rover in Antarctica
Next Generation SpaceCube / Flight Processor

- 2 Xilinx Virtex 4 FX60 w/ 4 PPC405
- Aeroflex RAD-HARD LEON_3 FT
- 12 GBytes FLASH
- 2 GBytes EDAC SDRAM (for LEON)
- 1553 A&B
- 256 Mbytes SDRAM / PPC
- cPCI – 32bit 33MHz
- 3U – 4 in x 6 in
3U cPCI SpaceCube
SpaceCube High Speed Processors

4 x 450 MHz PowerPC™ 405, 32-bit RISC processors:
   2 x Xilinx XC4VFX60
   Redundant to handle SEFI
   32K bytes of secondary (L2) on-die cache

Common Processor Features:
   700+ DMIPS RISC core
   32-bit Harvard architecture
   16 KB 2-way set-associative instruction and data caches

Auxiliary Processor Unit (APU) controller

1.2V core voltage

RECONFIGURABLE RESOURCES
   2 x 56,880 logic cells
   2 x 25,280 slices
   2 x 4,176 Kb block RAM
   232 18K block RAMs
   Example: Helion AES core
      447 slices, 10 block RAM, 2548Mbps performance

DRAM
   3Dplus stacked SDRAM
   8 Gbit 75 MHz
   Each PPC processor has 2 Gbit dedicated.
ETHERNET CAPACITY
2 x 10-Base-T Ethernet Interfaces
   Physical Interface is
   Hardened/Transformer coupled
   IEEE 802.3 compatible
   Ethernet MACS are built in to
   Virtex

DIGITAL SIGNAL PROCESSING
128 XtremeDSP Slices
18-bit by 18-bit, two's complement
   multiplier with full precision 36-
   bit result, sign extended to 48
   bits.

FLASH EPROM
256 Mbyte of Flash EPROM
   application storage
   Flash has separate power switching.
   Allows Flash to be powered off when
   not in use.

BOOT PROM
32 Kbyte of Rad-Hard Boot PROM for
   SpaceRISC Microcontroller
   Utilized at startup/reconfiguration as a
   “Hard” source of code

SOFTWARE SUPPORT
Support for Linux, VxWorks
   WindRiver
   MontaVista, BlueCat
   GNU GCC Compiler
SpaceCube Technical Information

SERIAL INTERFACES
32 x LVDS serial pairs:
- Support DS Ethernet, SpaceWire, or custom interface.
- 16550 compatible UARTs
- Aeroflex LVDS drivers and Receivers
- RS422 can be substituted for LVDS if desired

STACKING CONNECTOR INTERFACE
122 pins ICI Solder-mount Stacking Connector
Design uses no backplane or motherboard.
Low speed internal bus – 400Kbps Redundant I2C
High speed LVDM bus – 8 Bidirectional Pairs
Power Pins 3.3V, 5V

RAD-HARD SCRUBBER
2 UT6325 RadHard Eclipse FPGAs
320,000 usable system gates
Incorporates a SpaceRISC Microcontroller to monitor Xilinx Devices
RadHard to 300K rad(Si)/sec

OTHER PERIPHERAL INTERFACES
(Available through stacking connector by additional card slices)
Low Voltage Power Converter card slice
Provides low voltages from spacecraft bus voltage
1553 interface, transformers and signal drivers

Gordonicus LLC
Electrical and Environmental

**ELECTRICAL SPECIFICATION**
21V to 35V voltage input through optional low voltage power converter card slice
Power Slice can provide:
+5V@ 2 Amps
+3.3V@ 6 Amps
+2.5V@ 4 Amps
all voltages are tolerant to +10% / -10%

**SAFETY**
SDRAM power is switched separately to handle any potential latchup conditions.

**ENVIRONMENTAL SPECIFICATION**
-20°C to +55°C (operating Baseplate temperature)
-40°C to +85°C (storage baseplate temperature)
10% to 90% Relative Humidity, non-condensing (storage)

**MECHANICAL SPECIFICATION**
4 inches x 4 inches (PCB)
Box slice 4.25 inches x 4.25 inches x 1.25 inches/slice
double sided single board, double sided
I/O connectors:

Xilinx V4 FX60 (X 4)
TID 250 krad (Si)
SEL 100 LET(MeV-cm2/mg)
SEFI 1.5 E-6 Upsets / device / day