Military/Aerospace Programmable Logic Devices Conference, September 15, 2008

Retention Projections for SONOS Nonvolatile Semiconductor Memories (NVSMs) Based on Activation Energy Studies

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***Abstract* – At the backbone of every programmable logic/computing system is a nonvolatile semiconductor memory (NVSM) used to store the configuration code. If this memory, for example a NVSM-based FPGA, loses data, or becomes corrupted, the entire system operation is at risk. In the past few years this has become a major issue for space systems as there have been documented cases of commercial nonvolatile memory, while being packaged and screened for space applications, losing bits, or even pages of mission critical data. In response to these concerns, an extensive memory retention activation energy study has been carried out on an Northrop Grumman W28C0108 radiation hardened SONOS (Silicon – Oxide –Nitride - Oxide – Silicon) 1Mb (128K x 8) EEPROM, which is currently in production. Memory retention activation energies are 1.68 eV at the 1Mb EEPROM part level and 1.86 eV at the NSONOS NVSM transistor level. A 100% product screen has been implemented to guarantee all product exceeds 100 year memory retention at +125 C, thereby, making this part an ideal solution for mission critical applications. Detailed results of this study are presented in the paper.**

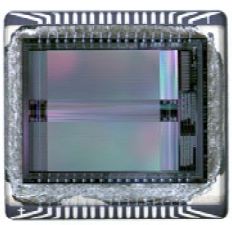
1. Approach

A two pronged approach has been employed to measure memory retention activation energy on a Northrop Grumman (NGC) W28C0108 1MB (128K x 8) EEPROM part level (See Figure 1) as well as at the NSONOS NVSM transistor level. For the 1Mb study, 58 1Mb EEPROM parts were characterized for memory retention over three temperatures (wafer level probing at +225 C, +250 C, +300 C) to obtain a consistent data set which could be fitted with a the traditional Arrhenius equation relationship:

$$MTF = A \exp(Ea/kT)$$

Rad Hard 1Mb EEPROM Characteristics

Parameter	Specification
Organization	128Kb x 8
Power Supplies	+3.3 V (Vdd), -4.2 V (Vwr)
Program Time (page)	100 ms
Endurance	
Write	1E4 cycles (min)
Read	Infinite cycles
Read Access Time	250 ns
Retention	>10 yrs @ +125° C
Temperature	-55 to +125C
Power Dissipation	
Standby	1 mW
Read	60 mW
Write	40 mW
Radiation	
Total Dose	300 krad(Si)
Prompt Dose Upset (logic)	>1E8 rad(Si)/s
Prompt Dose Upset (memory)	>1E12 rad(Si)/s
Prompt Dose Survivability	>1E12 rad(Si)/s
SEU (logic)	40 MeV-cm2/mg
SEU (memory)	>94 MeV-cm2/mg
Latch-up	None



▪ NGC 1Mb EEPROM has been successfully characterized in all radiation environments and has successfully passed life testing (1000 hour @ +150° C).

Fig. 1 - NGC W28C0108 1Mb (128K x 8) EEPROM

where A is a temperature independent constant, Ea is the activation energy, k is Boltzmann's constant and T is the absolute temperature.

The 1Mb EEPROM devices were programmed once for each temperature and subsequently read for memory retention at multiple time intervals. Testing was continued until the failure rates for the population were above 60% for each temperature. (Failures are defined to be ANY bit errors in the entire 1Mb memory.) For the NSONOS transistor array study, a sample of 7 packaged 1000 transistors arrays were evaluated for memory retention out to 2 days at +250 C and 1000 seconds at +125 C. (The purpose of this work was to model NSONOS NVSM transistor reliability on the 1Mb EEPROM product subjected to a 2 day / +250 C memory retention screen.)

2. Test Results

The data for the 1Mb EEPROM memory retention activation energy study is summarized in Fig. 1. The data set was analyzed using a commercially available failure analysis software tool. The calculated activation energy was 1.68 eV with a sigma of 0.68. (This is a low value for sigma, which indicates the data set is well-behaved and follows an Arrhenius relationship.) Mean times to failure for this study were 60 days, 5.5 days and 0.5 days at +225 C, +250 C and +300 C, respectively. Confidence interval calculations were performed to analyze the data. In Figure 2, for a 95% confidence level, initial 1Mb EEPROM retention failures are estimated to occur at 250 years at +125 C for this part.

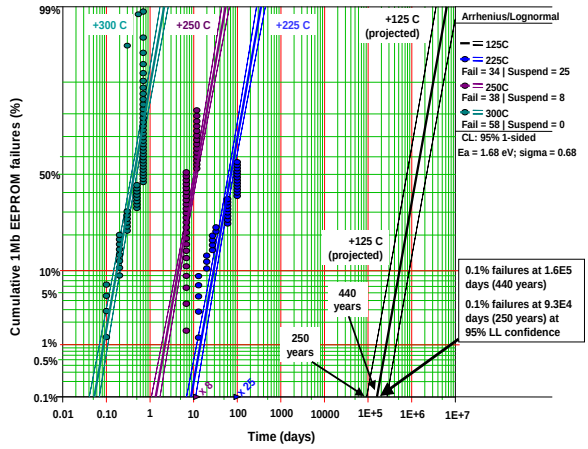


Fig. 2 -1Mb EEPROM NVSM retention data at +225 C, +250 C and +300 C. Memory retention activation energy is 1.68 eV

The NSONOS NVSM transistor array test results are summarized in Figure 3. This plot shows the two SONOS program states vs log of time for the +250 C and +125 C test conditions. The difference between the two memory states is referred to as the Memory Window and the 1Mb EEPROM sense amplifiers have been designed to operate with differences as low as 100 mV. The plot shows a 400-500 mV memory window after the 2 day / +250 C bake, so parts still exhibited a robust separation after this bake. The data taken at +125 C was then extrapolated out in time to match the memory window observed on NSONOS transistor arrays after a 2 day / +250 C retention bake. Note that this graphical representation shows that the 2 day / +250 C retention bake is equivalent to over 2600 years at +125 C. Using Arrhenius equation calculations, this thermal acceleration translates to an activation energy for memory retention at the NSONOS transistor level of 1.86 eV.

4. Summary

A radiation hardened SONOS 1Mb (128K x 8) EEPROM has been successfully characterized for memory retention over temperature at both the 1Mb part level and individual NSONOS NVSM transistor level. Memory retention activation energy has been determined to be 1.68 eV on 1Mb EEPROMs and 1.86 eV for NSONOS NVSM transistor arrays, which equates to a conservative estimate of 100 year retention at +125 C for the 1Mb W28C0108 EEPROM. As a result of our studies, memory retention projections can be carried out at different temperatures for different user applications.

5. Acknowledgements

The authors would like to thank the U. S. Army Space and Missile Defense Command (USASMDC), U. S. Air Force Space and Missile Systems Center (SMC), Navy Strategic Systems Program Office (SSP), National Science Foundation, NASA GSFC and the Missile Defense Agency (MDA) for past and continued support of our program.

6. References

[1] M. H. White, D. A. Adams, J. Bu, "On the Go with SONOS", *IEEE Circuits and Devices*, pp22-31, July 2000

[2] S. J. Wrazien, M. H. White, D. A. Adams, J. R. Murray, Y. Zhao, Y. Wang, B. M. Khan, W. S. Miller, R. Mehrotra, "Characterization of Scaled SONOS EEPROM Memory Devices for Space and Military Systems", *Non Volatile Memory Technology Symposium (NVMTS)*, Orlando, FL, November 2004

[3] J. Bu and M. H. White, "Design Considerations in Scaled SONOS Nonvolatile Memory Devices", *Solid-State Electronics*, 45, 113 (2001)

[4] M. H. White, Y. Zhao, Y. Wang, S. Wrazien, J. D. Krayer, D. A. Adams, J. R. Murray, "Scaled SONOS NVSM Devices for Space and Military Systems", *Non-Volatile Memory Technology Symposium (NVMTS)* 2003, San Diego, CA, November 2003

[5] D. A. Adams et al, "A Radiation Hardened SONOS 1Mb EEPROM for Space Applications", *2007 HEART Conference*, San Diego, CA

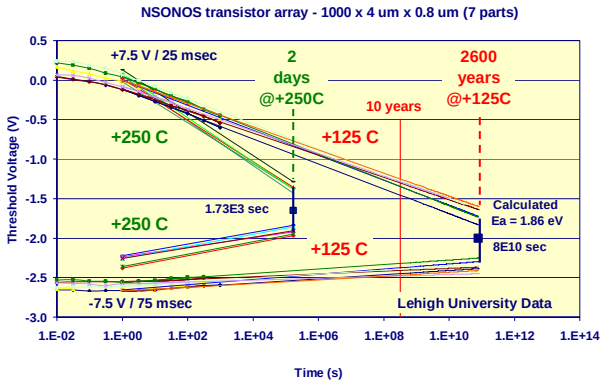


Fig. 3 - 2 day / +250 C retention screen performed on all 1Mb EEPROM product is equivalent to 2600 years at +125 C.