FPGA-Enhanced Ball Stack Rad-Hard Memory

Don Hayashigawa
NxGEN Electronics Inc.
San Diego, CA
donh@nxgenelect.com

***Abstract*- This paper examines the concept of packaging a ball stack memory with an on-board FPGA for military and aerospace applications. The benefits for such a design can include smaller size and reduced weight, higher performance and higher functionality. Higher performance can be achieved, for example, by using the FPGA to create higher data throughput than a single memory device. Some performance improvement can also be achieved through the reduction of package parasitics inherent to the ball stack design. Higher functionality can be achieved, for example, by using the FPGA as a memory controller for the entire memory stack. These potential benefits are weighed against potential drawbacks, which may include higher design and assembly complexity and higher material and assembly costs. These tradeoffs will be illustrated with a preliminary design using Rad-Hard Non-Volatile RAM consisting of 32 2Mbit FeRAM. In addition, an overview of the memory architecture, the design features of the FPGA and the FPGA selection process will be provided. A discussion of the electrical, mechanical and thermal considerations of the package design, which includes a ball stack package for the FeRAM memories and an interposer for the FPGA, will also be presented.**

Keywords-FPGA; CSP (chip scale package); FeRAM (ferroelectric memor); hardened-by-design; memory stack;SEU(single event upset); TID (total ionizing dose); EDAC (error detection and correction), TMR (triple mode redundancy), SET (single event transient), SEL (single event latchup); CCGA (sceramic column grid arrays);CQFP (ceramic quad flat packs)

I. INTRODUCTION

The requirements for non-volatile memory for military and aerospace applications continue to increase both for memory density and performance. On the one hand, there are some applications, boot EEPROMS for examples, which require only a few hundred kilobytes of non-volatile memory. On the other hand there are applications which require up to several terabytes of non-volatile memory, specifically solid state recorders and solid state drives used for storing flight, scientific instrumentation or terrain mapping data, as examples.[1]

For terabit/terabyte solid state drives and data recorders, the only apparent non-volatile memory technology which is practical is flash memory, simply because the density of flash technology is three orders of magnitude higher than any other competing non-volatile technology. The largest available ferro-electric memory is typically around 4 Mbits to the best of our knowledge, while Micron has just recently announced a 32 Gbit MLC devices.[2,3]

To achieve higher memory densities, some form of memory stacking is almost always utilized. Memory in the form of BGA'S or TSOP's may have as many as eight die stacked internally. Multi-chip packages are formed by stacking multiple TSOP's again as much as eight high.

II. FLASH MEMORY STACK AND FPGA DESIGN

At NxGen Electronics Inc, a 64 Gbyte memory stack (see figure 1 and figure 2) consisting of 32 16 Gbit flash die is being developed for a military application.[4] Prototypes for this design are to be completed in early 2009. The memory itself consists of eight CSP's, each containing four thinned flash memory die microns. The die are wirebonded to substrate wirebond pads which then interconnect through traces to solderball pads. The solderball pad pitch is currently set at .8mm, although pitches down to .65 mm are possible. Adding solderballs to each of the solderball pads and encapsulating completes the CSP package**.**

It should be noted that since each 4-high stack can be individually tested, a reasonable final yield should be obtainable. In addition each CSP substrate accommodates two chip capacitors for improved power supply bypassing.

A stack of eight of these memory CSP's stacks are reflowed together onto an interposer substrate. Mounted underneath the interposer is a FPGA, which acts as a memory controller. Large peripheral BGA balls on the underside of the interposer form the interconnect to the motherboard. Another viable option would be to use formed flat leads for this interconnect.

The final dimensions for this package are 21mm x 13.5 mm and less than 6 mm high. The space savings of this approach are significant. If one were to lay the equivalent memory using single die TSOP's, the area consumed would be roughly 30 times larger and this number does not take into account the area saved on the PCB.

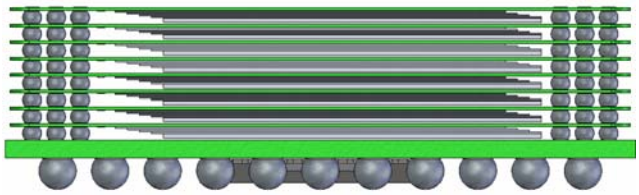

Figure 1.

lash Stack (Side View)

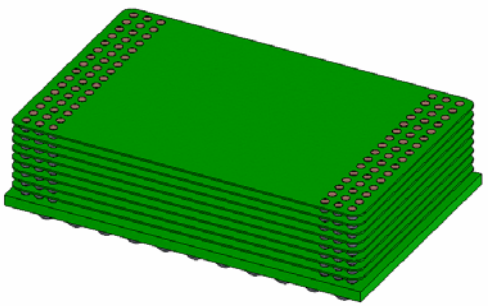

Figure 2.

lash Stack Design (Top Views)

A simplified, preliminary block diagram is shown for the FPGA memory controller in figure 3 below. Note that the memory stack is organized as an interleaved memory consisting of two 32G x 8 memory blocks. The reasons for interleaving the memory is to improve output loading of the memory and to provide for a more efficient interconnect between the memory stack and the FPGA.

For the package thermal analysis it was assumed that that the controller would dissipate roughly 250 mW. To improve thermal heat transfer, a solderable metal plate is attached to the encapsulation side of the FPGA, providing a thermal path to the motherboard. This plate will be soldered to a pad during SMT reflow of the package to the motherboard along with package leads or balls. The other thermal path will be provided by a coldplate to which the top die of the stack will contact through either thermal grease or a thermal pad. For consistency with the proposed organization of the memory stack, the analysis assumes that two die are on at the same time, each dissipating a ¼ watt. With these assumptions a thermal analysis was conducted with the results as below in figure 4.

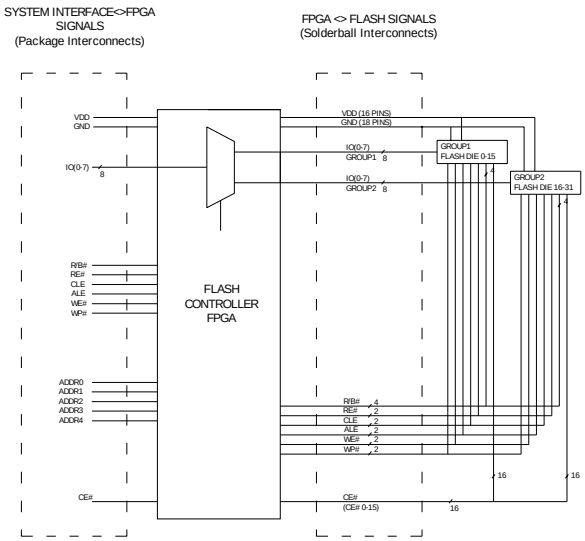

Figure 3.

Flash Stack Block Diagram

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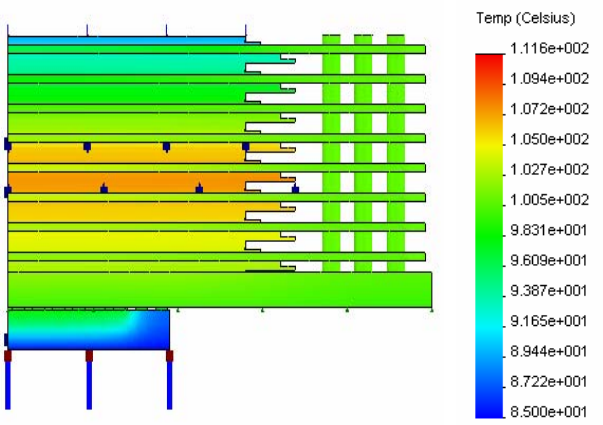

- ¼ of Package Utilized (symmetry assumed)
- ½ Watt on FPGA die. 2 die on at middle at ¼ watt apiece
- Upper Cold plate at 85 °C.
- Lower Heat sink at 85 °C.
- Max Heat Rise- 26°C

Figure 4.

lash Stack Thermal Analysis

III. RADIATION-HARDENED MEMORY STACKS

Although the above package is non-volatile and combines a memory stack with an FPGA, neither the FPGA nor memory is

radiation hardened. One method for achieving radiation hardening is to select a Rad-hard FPGA, typically made by Xilinx or Actel, find an appropriate flash memory with the reasonable radiation characteristics (i.e reasonably high SEL) and then apply appropriate design techniques within the FPGA to mitigate the effects of radiation on both the FPGA and memory. Current techniques include EDAC, TMR, SET filtering for combinational and memory scrubbing.[5, 6] It should be noted that between SRAM-based and flash-based FPGA's, the flash-based FPGA's

Another method would be to replace the flash memory with a non-volatile memory which is radiation-hardened by design. One example is a 2 Mbit FeRAM, which has been developed by NxGen and Celis Semiconductor for space and military programs requiring radiation hardening.[7,8] The FeRAM has been designed for fast read/write times, good data retention characteristics, high endurance and low power. The block diagram and the target design characteristics are shown below in Fig. 5 and Table I. It should be noted that work remains to improve the standby leakage results after TID testing.

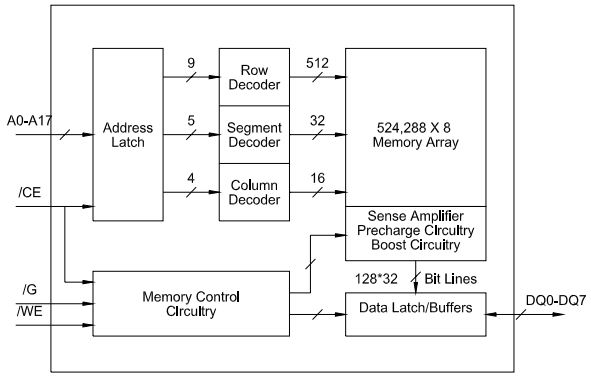

Figure 5.

eRAM block diagram

TABLE I. 2MB FERAM TARGET DESIGN CHARACTERISTICS

Radiation Tolerance	>10^6 rads (Si)
Single Event Upset	<10^–10 errors/bit-day (–55°C to 125°C)
Data Retention	>10 year at 85°C
Read/Write Endurance	>10^12 cycles
Read and Write Cycle Time	<100ns
Active Current	40mA
Standby Current	10µA (Pre-radiation)
Power Supply Level	3 ± 0.3V
Operating Temperature Range	–55°C to 85°C
Temperature Range	–55°C to 125°C Storage

As mentioned before the, the density of flash memory is so much greater than FeRAM or virtually any other non-volatile memory that the density of the FeRAM stack will be correspondingly less. In fact, even with 32 die, the total stack memory is 64 Mbits. However, the rad-hard FeRAM is rad-hard, lower power and is much more reliable than flash with regard to data retention and wearout. Where this reliability is critical and a modest amount of memory is required, as for a buffer or cache application, the FeRAM stack may provide the best solution.

A block diagram for a FeRAM stack with FPGA is shown below in figure 6. As a way to improve performance, the memory is interleaved into 4 memory banks. The FPGA is used to implement this control. In theory, this would allow the memory to run a four times its normal speed.

It is possible to reduce the number of FPGA-to-memory connections, if the FPGA has sufficient drive capability. As designed, each FPGA output driving the memory inputs has a maximum fanout of 16.

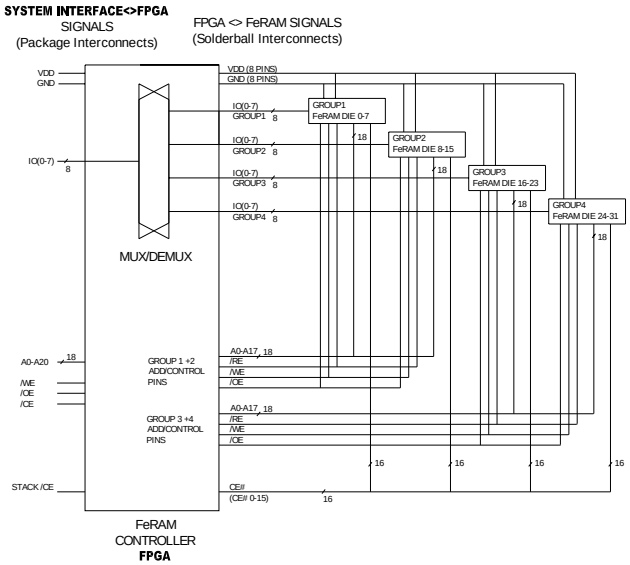

Figure 6. F

onceptual Block Diagram of FeRAM stack with FPGA

Most rad-hard products are packaged in either CCGA's (ceramic column grid arrays) or CQFP (ceramic quad flat packs). It does not seem practical to mount a CCGA's underneath the interposer as this would radically increase the height of the package. The simplest approach to take is to mount a CQFP package underneath instead, as shown in the conceptual drawing in the figure below. The other possibility is to obtain Known Good Die for the FPGA, but this does have a significant NRE/NRT cost associated with it. As a result, if the FPGA requires a few hundred I/O and a CCGA, the memory stack may not be a viable packaging option. Having FPGA outputs with good fanout capability will help to reduce the number of required CQFP leads.

In assembly, the CQFP will need to be mounted face-down along with the leads of the interposer. The attachment could either be with solder if there is a metal pad to solder to. If not, then the attachment would have to be with a thermal adhesive or gel. In either case, there should be a good thermal conductive cooling path through the board.

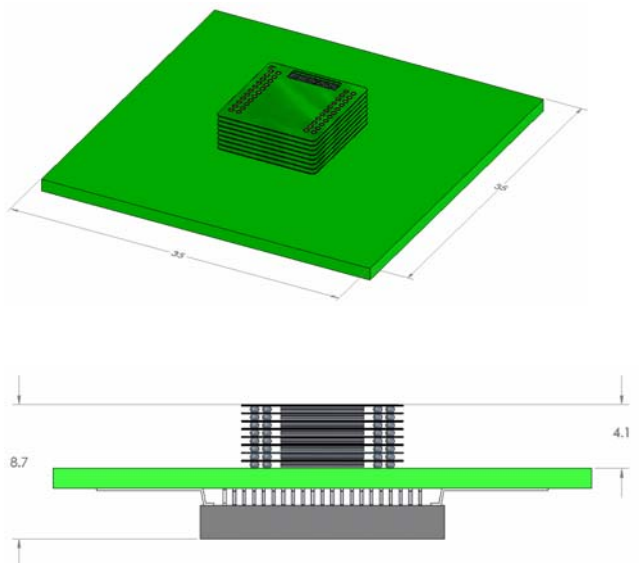

Figure 7. onceptual Drawing FeRAM Stack with CQFP FPGA C

IV. CONCLUSIONS

The design concept of a non-volatile memory stack consisting of up to 32 memory die combined with a rad-hard FPGA has been examined. From this it appears that this approach is viable for use with low-density memory (e.g. FeRAM) and high density memory (e.g. flash memory). Moreover, the memory stack may be radiation hardened either because the constituent memory die are rad-hard (e.g NxGen/Celis FeRAM) or because the FPGA uses radiation mitigation circuitry to . In the case of the FeRAM, the likely use of the memory is as a memory cache or buffer. For a rad-hard package design, the most apparent choice for the FPGA is a CQFP package.

The next steps would, hopefully, be to determine an appropriate application for this memory stack design, generate the product requirements and proceed onto prototype development and qualification.

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