High Speed Radiation Tolerant PLD/FPGA I/Os for the Next Generation of High Performance On-Board Computing

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Presentation Outline

1. Design goal identification and overview;

2. I/O schematic and layout designs;

3. Simulation results;

4. Utilized radiation tolerance techniques;

5. Test results;

6. Conclusions.

Programmable Logic Devices (PLD)

PAL
Programmable Array Logic

Architecture:

"Sum-of-products" combinational cells

Programming:

One-time (fuses or anti-fuses).

Complexity:

100x logic gates,

10x I/Os.

CPLD
Complex Programmable Logic Device

Architecture:

Macro cells with complex functions

Programming:

On-chip Non-volatile memory.

Complexity:

1000x logic gates,

100x I/Os.

FPGA
Field Programmable Gate Array

Architecture:

"Lookup table" logic blocks;

Programming:

Hardware-based reprogrammable.

Complexity:

10^6x logic gates,

1000x I/Os.

SCMP
Software Configurable Micro Processors

Architecture:

Multi-core micro processors;

Programming:

Software-based reconfigurable.

Complexity:

10^6x logic gates,

100x I/Os.

Input/Output Buffers

Input/Output buffers (I/Os) are among the most critical parts of PLD ICs:

• I/Os can consume up to 50% of the total IC's power; for example: **1 *CML_OD* = 40 *HS_GATES* = 1000$^+$*LS_GATES***,

• I/Os have to deal with large parasitic components associated with packages and/or external connections (several *nH* and *pF*);

• I/Os must function at high speeds in order to meet current and future PLD data through-put demands.

• I/Os must exhibit a certain level of radiation tolerance to be considered for space bound PLDs.

Common Interface Standards

• <u>LVDS is a low power & high speed standard [1-2] that meets the demands of high performance PLD I/Os.</u>

Logic type	Supply voltage, V		Interface type	Voltage swing, mV	Common-mode, V	Termination type
	Vcc	Vee				
ECL	0	-5.2	Diff.	800	-1.3	2X50 Ohm to –2V
PECL	5.0	0	Diff.	800	3.7	2X50 Ohm to 3V
LVPECL	3.3	0	Diff.	800	2.0	2X50 Ohm to 1.3V
CML	3.3	0	Diff.	800	3.1	2X50 Ohm to Vcc
LVDS	2.5-3.3	0	Diff.	400	1.2	100 Ohm diff
TTL	3.3-5.0	0	SE	2000	1.4	
CMOS	1.8-5.0	0	SE	Rail-to-rail	Vcc/2	

Targeted in this design

Abbreviated Target Specs. For I/Os

IO Type	Parameter name	Parameter value		Units	Comments
		min	max		
OB	Operational frequency	1.0	1.5	GHz	
	Output swing	260	400	mV	Single ended
	DC common mode voltage	1125	1275	mV	
	Output impedance	40	140	Ohm	Each pin
	Power supply	+2.375	+2.625	V	±5%
	Anti-TID and Latch-up protection	Yes			By layout
	Anti-SET protection		No		
IB	Operational frequency	1.0	1.5	GHz	
	Input sensitivity	100		mV	Single ended
	Common voltage range	0	2.4	V	DC to 1GHz
	Input impedance	90	110	Ohm	Differential
	Power supply	+2.375	+2.625	V	±5%
	Anti-TID and Latch-up protection	Yes			By layout
	Anti-SET protection		No		

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Output Stage

1.6V Power Supply (VS)

High Speed FETs

0.8V Power Supply (VS)
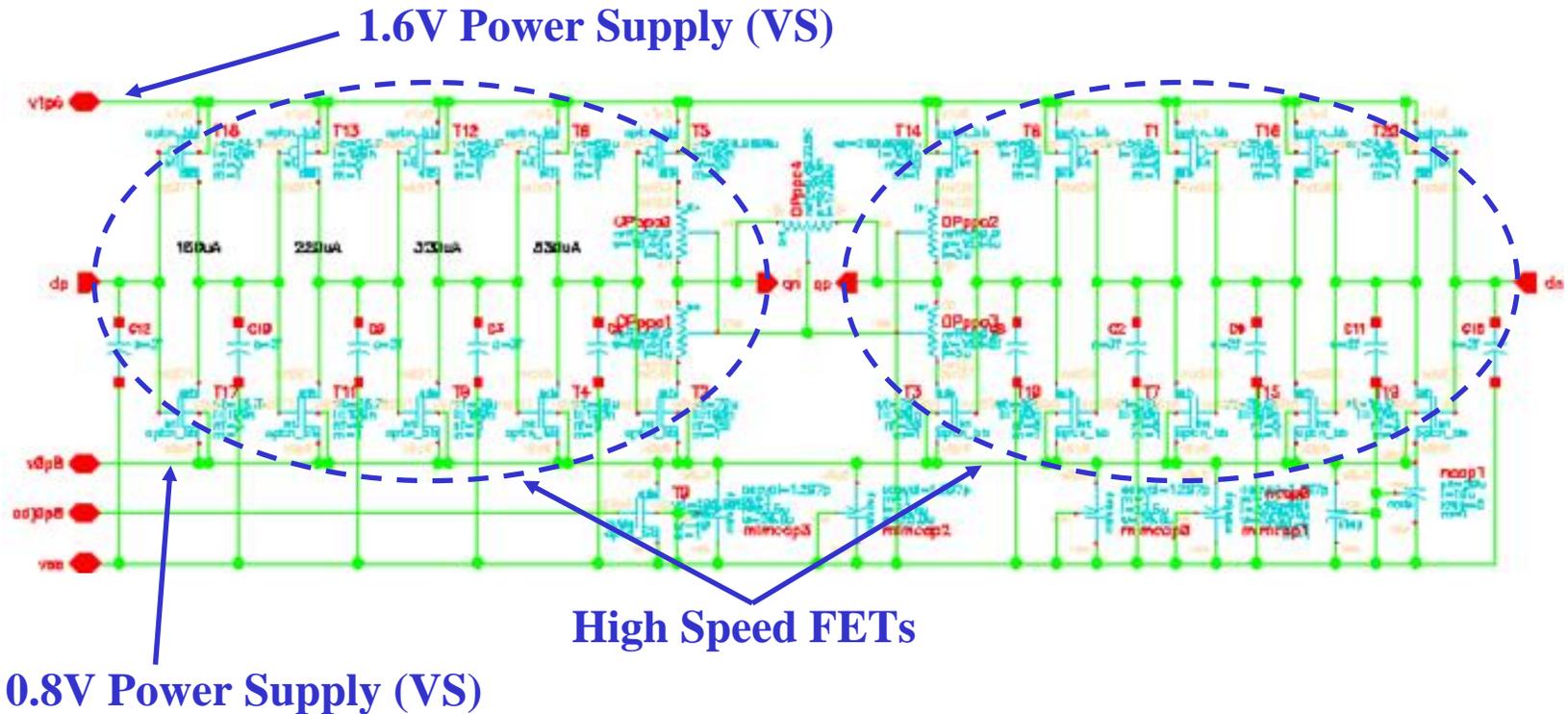
- Voltage source (VS) – VS architecture for low power performance (<10mW at 1GHz);

- Internally generated 0.8V power rail allows for utilization of high speed FETs;

Output Stage Description

- Employs high-performance and low-power architecture detailed in [3].
- Main section of the output buffer consists of four FETs (T5, T2, T14, & T3) and 33Ω resistors (OPppc0,1,2,&3) where the 8 additional CMOS inverters are for buffering reasons.
- NFET (T0) works in concert with a voltage regulator/comparator (not shown) to generate the stable $0.8V$ supply (v0p8) while another regulator (also not shown) produces the $1.6V$ supply (v1p6). These two supplies allow for the utilization of high speed devices in the output stage.
- Depending on the logic of the input signal (dp&dn), either the pair T2&T14 (logic=1) or T5&T3 (logic=0) is open creating high quality output signaling and buffer characteristics that satisfy the LVDS standards.
- A large resistor (OPppc4) is included between the differential output pins (qp&qn) to avoid any device breakdown conditions during power up due to the "slow" time constants of the regulator cells.
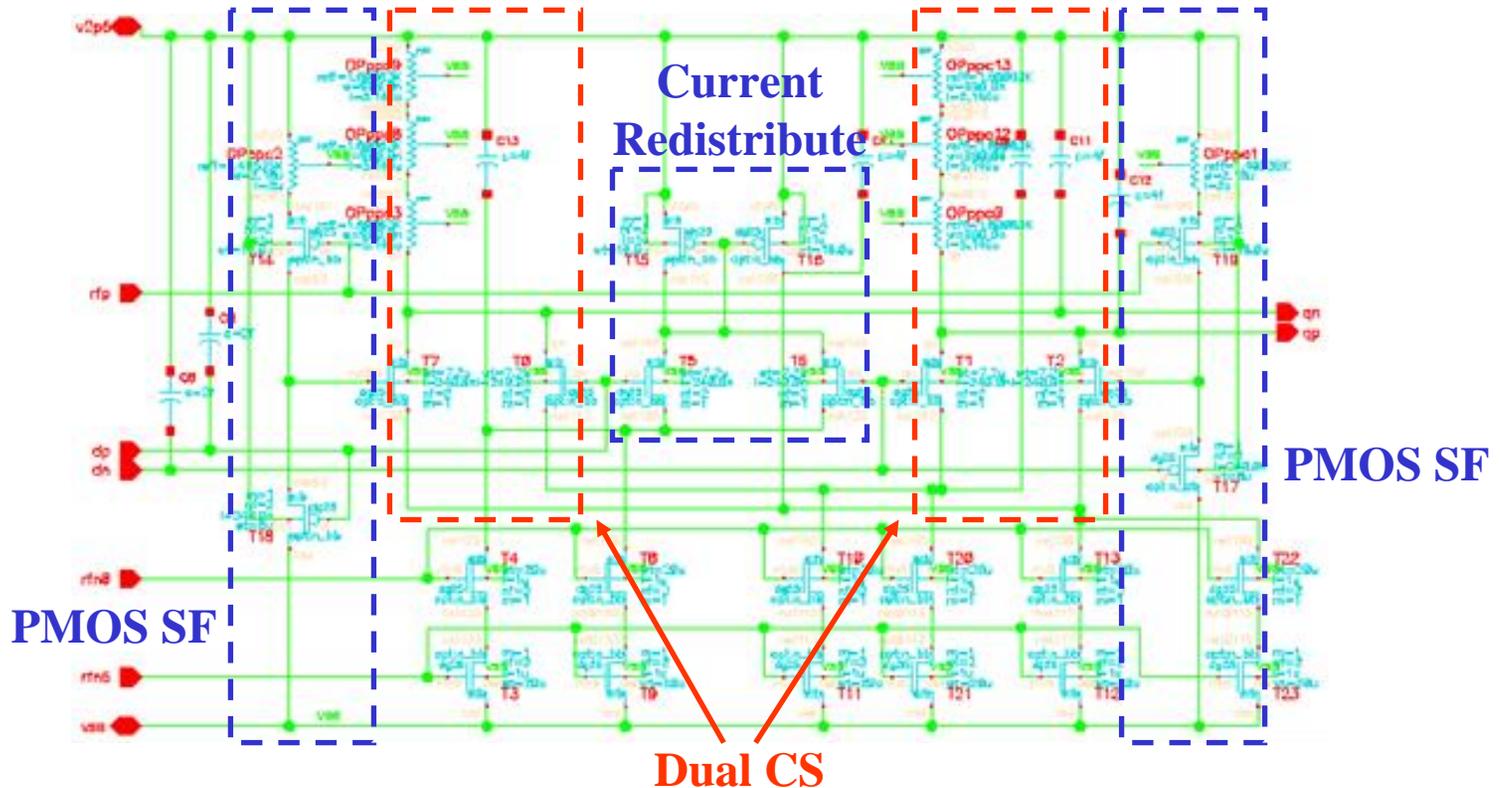- Accurate optimization results in total current consumption below $5mA$.

Output Stage Simulations

Vcm=1.2V

Vdiff=±330mV

(a)

(b)
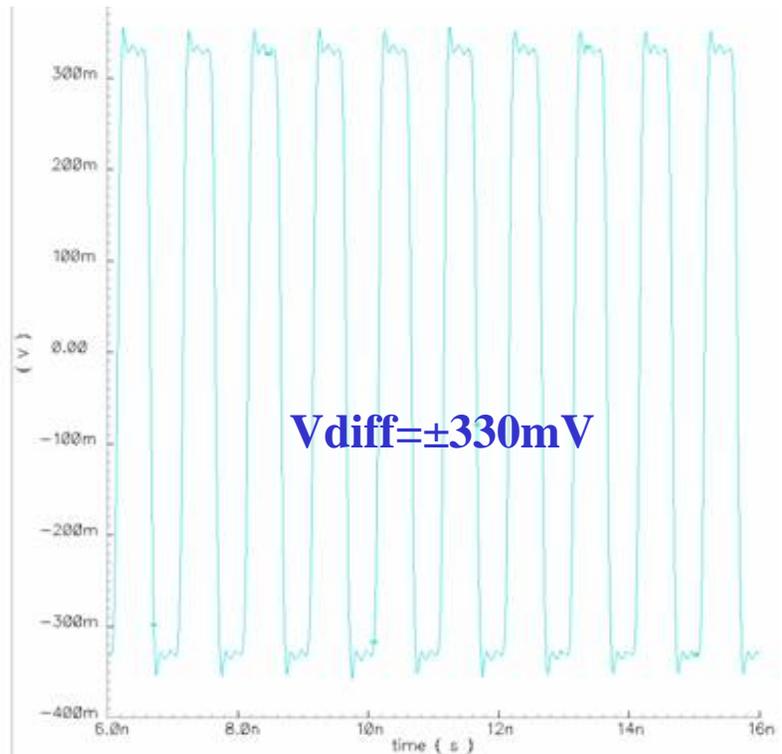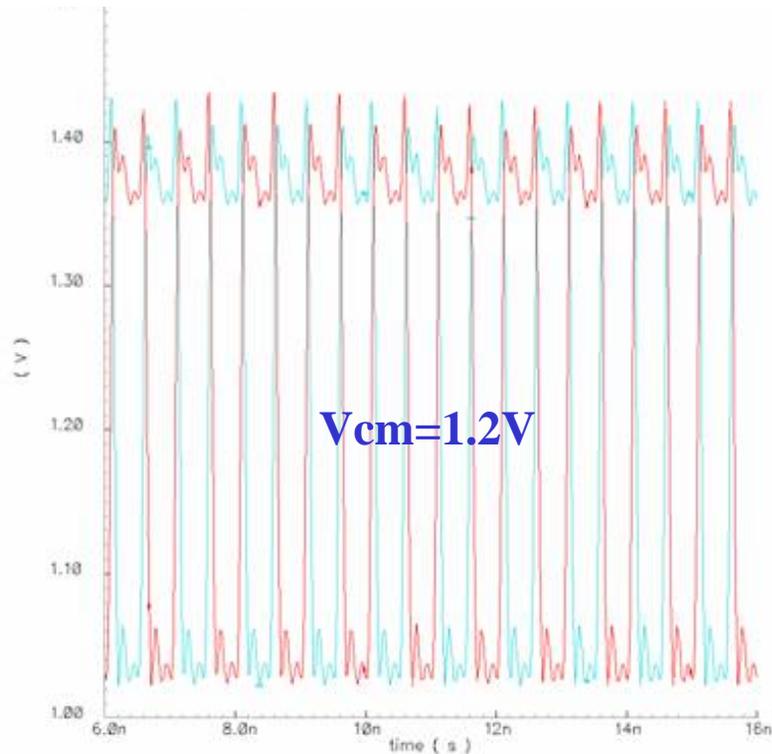
Output Signal at 1GHz: (a) Single Ended and (b) Differential Signals.

Input Stage

- Produces identical output signals for input signal CM values between < 0V to > 2.5V:

    - Level shifting PMOS source followers (SFs) for low CM values;

    - Dual current switch (CS) configuration for high CM values.

Input Stage Description I

- Accepts LVDS input signaling with CM voltage levels between Vee (GND) and Vcc (2.5V).
- Includes the following primitive cells:
  - Two CML buffers with common loading resistors and equal tail currents (NFETs: T0& T1 and T7&T2, resistors: OPppc3,8,9 and OPppc0,12,13);
  - Two P-MOS source followers (PFETs: T18 and T17);
  - Tail current redistributing cell (FETs: T5, T6, T15, and T16).
- Input signals with high enough common mode voltages are processed by the first differential current switch (T0&T1), which is directly connected to the input pins (dp&dn).
- Current switch (T7&T2) receives the same two input signals through voltage level-shifting source followers (T18 and T17), and thus can deal with low common voltage levels.
- The total current through the common load resistors is kept at a constant level by the tail current redistributing cell (T5, T6, T15, and T16), which mirrors the current of the first buffer and subtracts it from the second buffer's tail current source.

Input Stage Description II

- The input buffer automatically adapts to the input common mode voltage and provides standard CML (current-mode logic) output voltage levels.
- The maximum operational speed of the buffer is limited at low DC input signal CM levels by the PMOS source followers.
- The buffer's adaptability to AC CM levels is determined by the speed of the tail current redistribution cell. Simulation results reveal that the buffer's output signal remains stable over AC CM signals $>1 GHz$.
- A CML latch connected to the buffer's outputs (not shown) provides the switching hysteresis required by the IEEE LVDS standard. For additional signal shaping the output signals are processed by an additional RS latch (also not shown in the drawing).
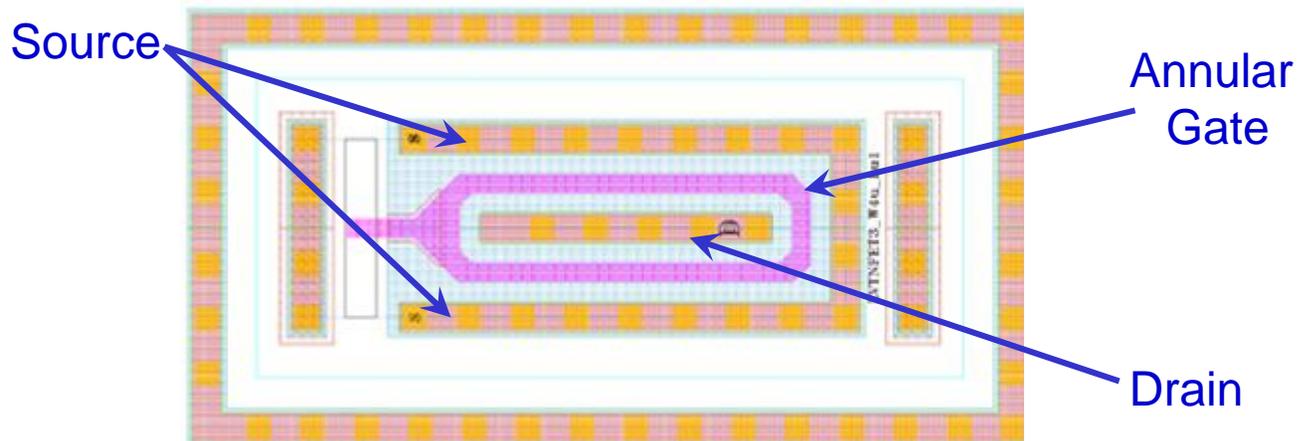
Input Stage Simulations

(a)

(b)

Vcm=2.5V

Vcm=1.2V

Vcm=0V

Similar Output Signals
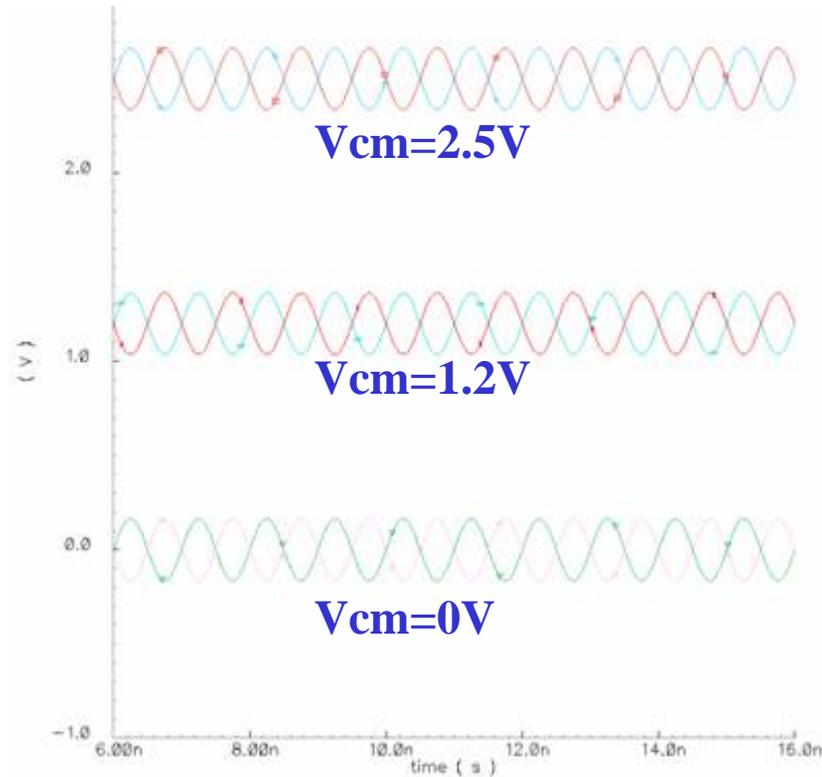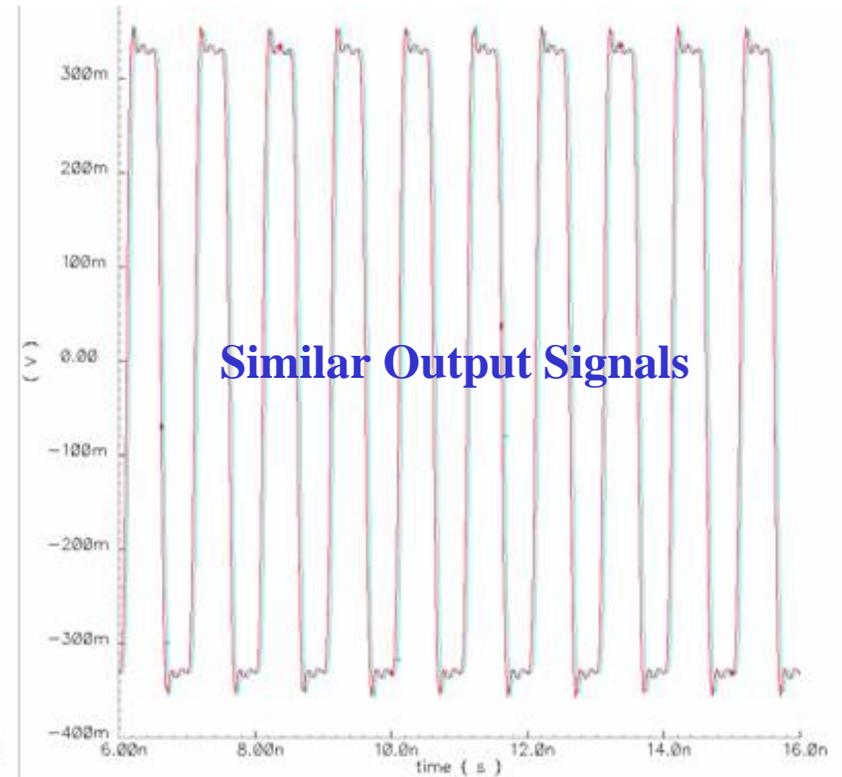
Input Signaling at 1GHz: (a) Single Ended Signals at Vcm = 0.0V, 1.2V, and 2.5V and (b) Resulting Differential Output Signals.

Radiation Tolerant Layout


Source

Annular Gate

Drain

Annular Transistor Layout (NFET)

• Layout follows methodology presented in [4] and additional guidelines provided by Micro-RDC in order to harden the circuitry against TID up to 2.0$Mrad$.

• Proprietary layout techniques were used to achieve minimized device mismatch, small area, and low values of parasitic components within a short design cycle.

• The test chip was designed and fabricated in a standard 90nm CMOS technology.

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Test Results: Waveforms

Evaluation Board
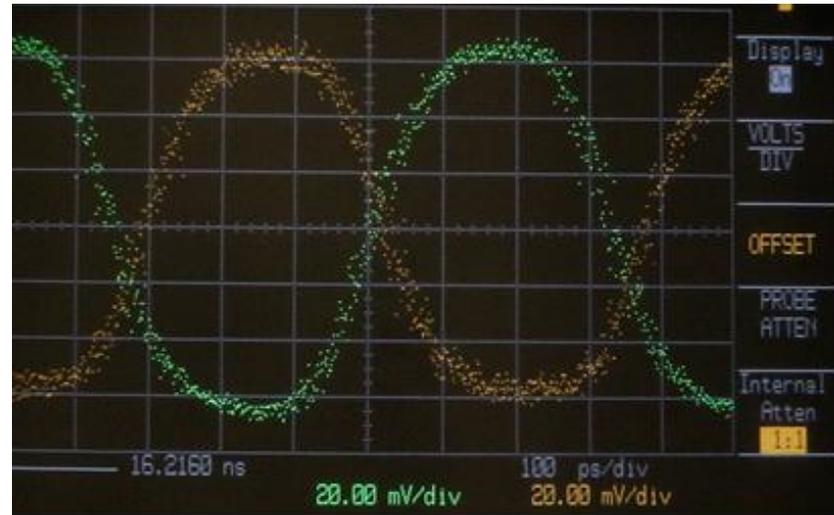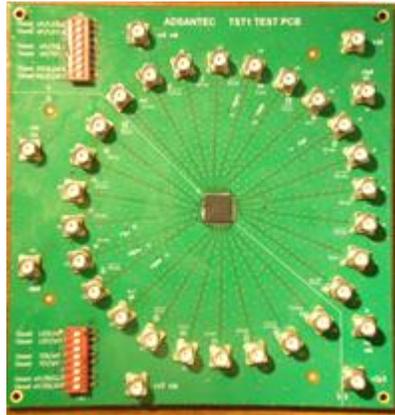
Output Signals Identical!

Output Stage Signal at 1.4GHz (1:3 attn.).

(a) Input Vcm = 0V   (b) Input Vcm = 0.5V   (c) Input Vcm = 2.5V

Input Signaling at 1.4GHz (1:12 attn.).

Test Results: TID Testing

TID (*krad*)	0	100	300	500	1000	2000	Annealed
Total Chip Power Supply Current (*mA*)	59.5	61.0	59.8	60.0	60.7	61.0	60.2
Maximum I/O Frequency of Operation (*GHz*)	1.68	1.70	1.68	1.74	1.64	1.66	1.69

Annealed: 168 hours at 100°C.

- TID testing of the LVDS I/Os was conducted at Kirtland Air Force Base, Albuquerque, NM with support from Jim Smith and his Micro-RDC testing team.
- The results prove the soundness of the layout hardening techniques.
- ADSANTEC wishes to thank Dr. David Alexander of AFRL for his help.

Simulated vs. Measured

IO Type	Parameter name	Simulated Values		Measured Values		Units	Comments
		min	max	min	max		
OB	*Operational frequency*	-	1.4	-	1.7	*GHz*	
	Output swing	265	380	320	350	*mV*	Single ended
	DC common mode voltage	1132	1267	1175	1220	*mV*	
	Output impedance	40	140	60	65	*Ohm*	Each pin
	Power supply	+2.375	+2.625	+2.3	+2.7	*V*	±8%
	Anti-TID & Latch-up	Yes		Yes			Passed Test
IB	*Operational frequency*	-	1.45	-	1.7	*GHz*	
	Input sensitivity	100		~105		*mV*	Single ended
	Common voltage range	0	2.4	-0.2	2.6	*V*	DC Tested Only
	Input impedance	90	110	98	98	*Ohm*	Differential
	Power supply	+2.375	+2.625	+2.3	+2.7	*V*	±8%
	Anti-TID & Latch-up	Yes		Yes			Passed Test

Conclusions

- Multi-gigahertz FET based I/Os that satisfy the LVDS IEEE standard 1596.3-1996 have been presented.

- The output buffer utilizes a proven optimal architecture and careful schematic optimization to generate high-quality output signals while consuming less than $5mA$ of current.

- The input buffer exceeds the LVDS specifications by utilizing an adaptive approach to correctly process input signals with CM levels equal to or between Vcc and GND.

- I/O resistance to TID up to $2Mrad$ is achieved by hardening-by-design methods that have been verified through testing results.

References

1. "IEEE Standard of Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)", IEEE Std. 1596.3-1996, Approved 21 March 1996, ISBN 1-55937-746-1.

2. Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits", ANSI/TIA/EIA-644-1995, Telecommunications Industry Association, March 1996.

3. V. Bratov, J. Binkley, V. Katzman, and J. Choma, "Architecture and Implementation of a Low-Power LVDS Output Buffer for High-Speed Applications", IEEE Trans. on Circuits and Systems I, v. 53, No. 10, Oct. 2006, pp. 2101-2108.

4. David R. Alexander, David G. Mavis, Chatles P. Brothers, and Joseph R. Chavez, "Design Issues for Radiation Tolerant Microcircuits in Space", 1996 IEEE Nuclear and Space Radiation Effects Conference Short Course, 1996.