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Fault Tolerant, Reconfigurable FPGAs in High-Speed Encryption Application



Abstract

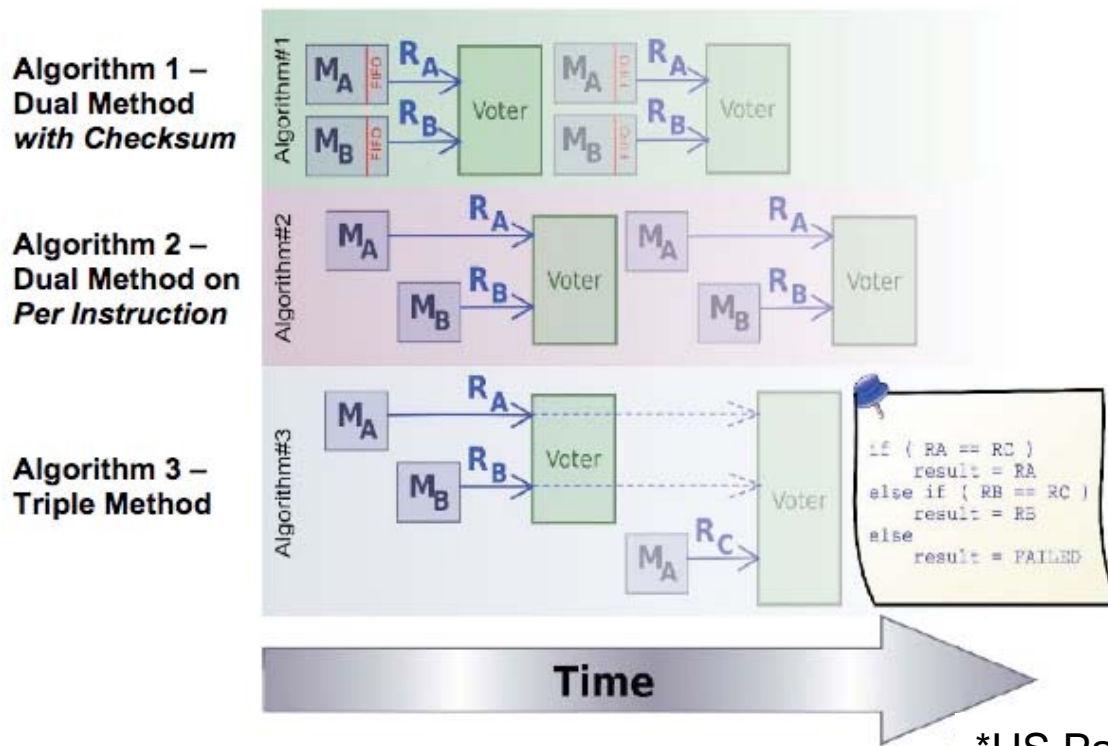
Research was completed on the Proton300k™, a radiation hardened and SEE fault tolerant, reconfigurable FPGA computing platform.

The research included development of a unique SEU mitigation technique, TTMR™ (Time-Triple Modular Redundancy), which enables detection and correction of SEUs in reconfigurable FPGA logic blocks.

Additional research was completed on a hardware and software method , Hardened Core-2™, for detection and correction of SEFI and reconfiguration errors.

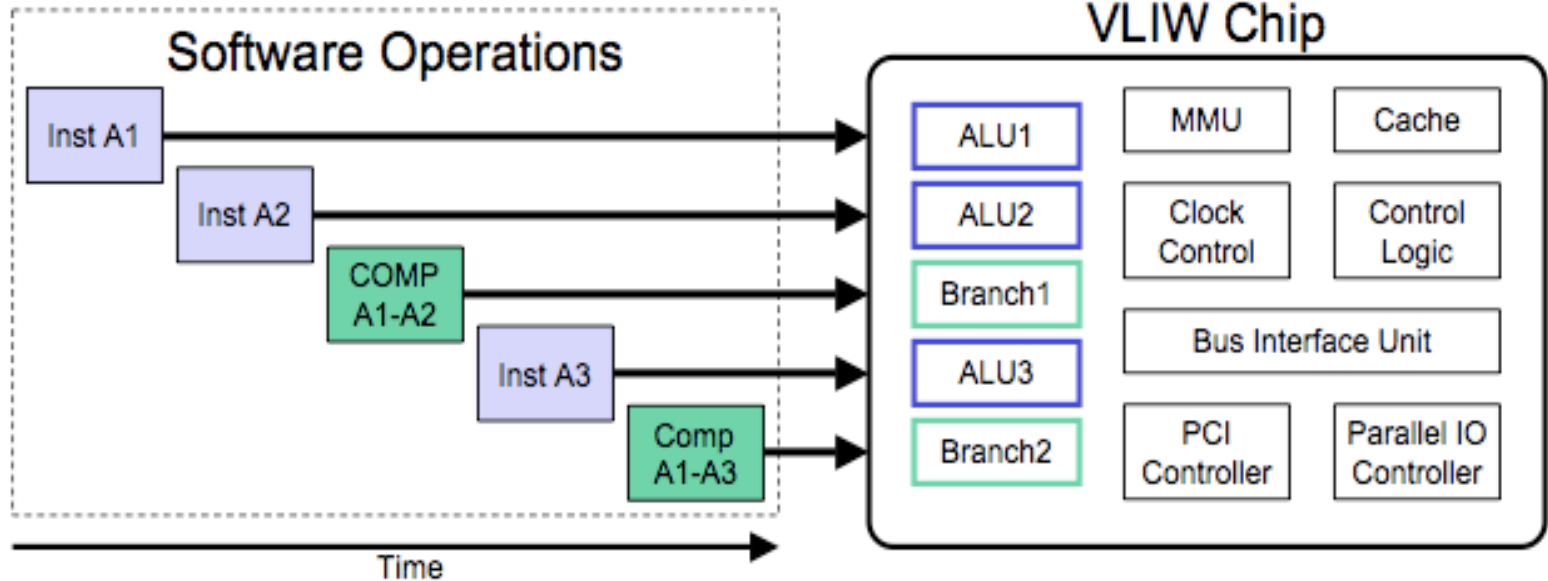
TTMR™* For FPGA

Research was completed on a radiation hardened and SEE fault tolerant reconfigurable FPGA computing platform, termed the Proton300k™. The research included development of a unique SEU mitigation technique, called Time-Triple Modular Redundancy™, which enables detection and correction of SEUs in reconfigurable FPGA logic blocks.



*US Patent 7,260,742

TTMR™* for Processors

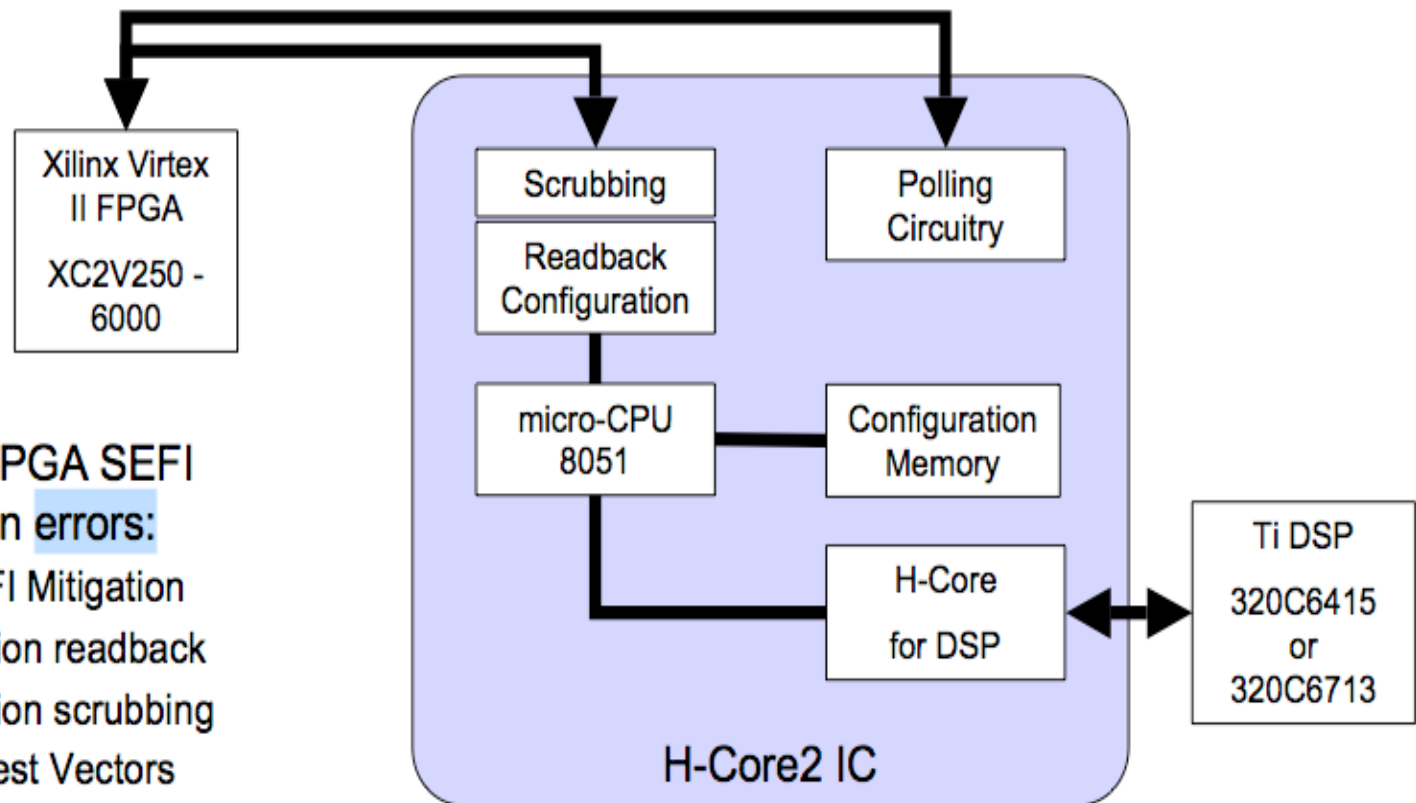


- TTMR™ Combines Time & Spatial redundancy
- Takes advantage of VLIW parallel opportunities
- SEU error rate equal to TMR rates
- SEFI is NOT fixed with TTMR
- Proton radiation tested at 51 MeV
- Detects & corrects SEUs

*US Patent 7,260,742

H-CORE2™* for FPGA

Use Industry Standard Techniques to Fix SEFI & Reconfiguration



- H-Core2 for FPGA SEFI & configuration errors:
 - FPGA SEFI Mitigation
 - Configuration readback
 - Configuration scrubbing
 - Periodic Test Vectors
 - Signature Analysis

H-CORE™* for Processors

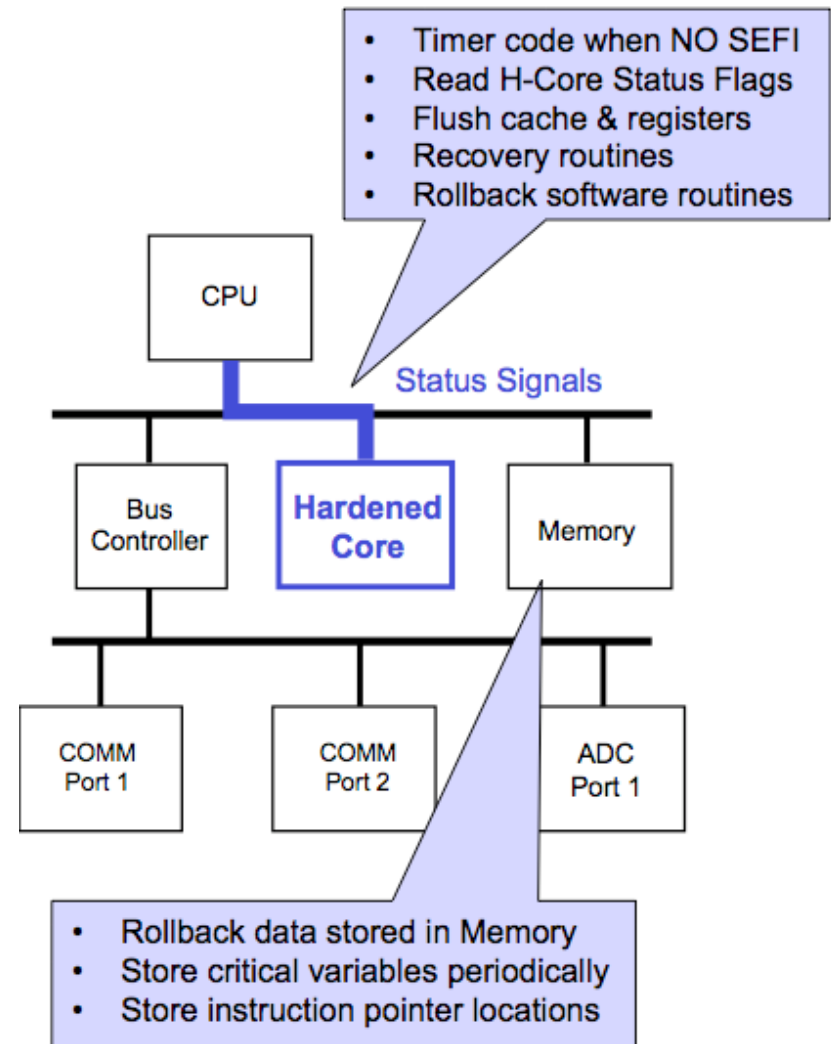
Hardware:

✧ Rad-Hard External watchdog, sends functional interrupts and resets as required

Software:

✧ Generate health /status signals, and runs interrupt routines
✧ H-Core IC, Monitor signals, initiate post-SEFI recovery using interrupts, and full reset as required

*U.S. Patents 7,237,148
7,260,742



UC Davis SEE Tests of Proton300k™ Dec 10, 2007

The Virtex-4 FPGA will be hit with protons at 63MeV. The goal of the test is to observe SEU and SEFIs being detected and "corrected" in accordance to the TTMR algorithms. All SEUs should be handled by the voter, while SEFIs should be handled by a reconfiguration, and if needed, a power-cycle of one or more boards.

Once the radiation experiment is started, the Virtex-2 FPGA configures the Virtex-4 through the SMAP interface. Once configured, the DSP begins to send test vectors to the Virtex-4. Every 10 test vectors, a checksum is received. Each EDAC unit sends a checksum, and these checksums are compared. Using these checksums, the software evaluates if an SEU or SEFI has occurred. When a SEFI occurred, both boards were powered cycled.

Test Results:

Beam Type: Proton
 Beam E (MeV): 63
 Target: Si
 dE/dx (MeV*cm²/g): 8.43
 Date: 12/4/2007

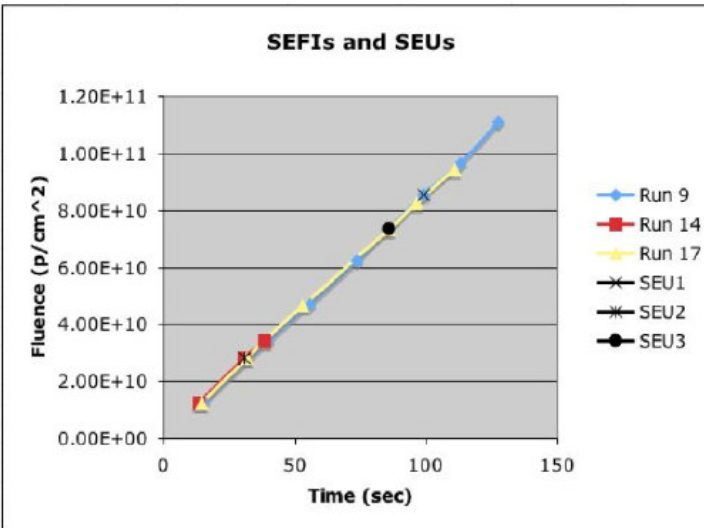
FC/SEM Ratio: 1.47E+000 ± 2.2406E-03 File Name:
 FC Lkg (A): 5.61E-014 ± 2.624E-14
 SEM Lkg (A): 1.57E-014 ± 8.417E-15



Figure 4: Virtex-4 Board in beam path.



Figure 5: DSP/Virtex-2 board set away from beam.



SEFI and SEU occurrence with respect to Time.

RUN#	RunTime (s)	Mean Current (A)	Std Dev <I> (A)	Incr Dose (rad)	Acc Dose (rad)	Incr Fluence (p/cm ²)	Acc Fluence (p/cm ²)	Avg Dose Rate (rad/s)	Beam Prof
Run #1	12:54:17 PM 18.23	6.47E-011	1.16E-011	2.72E+001	2.72E+001	2.01E+008	2.01E+008	1.49E+000	0 - 0.5 cm
Run #2	12:58:58 PM 6.59	5.55E-011	1.64E-011	8.43E+000	3.55E+001	6.24E+007	2.63E+008	1.28E+000	0 - 0.5 cm
Run #3	01:02:01 PM 112.5	6.30E-011	5.70E-012	1.63E+002	1.99E+002	1.21E+009	1.47E+009	1.45E+000	0 - 0.5 cm
	01:04:17 PM	FC Lkg (A): -4.51E-013 ± 6.248E-14							
		SEMLkg (A): 1.05E-012 ± 9.544E-14							
Run #4	01:07:50 PM 16.05	7.82E-010	2.70E-010	2.89E+002	4.88E+002	2.14E+009	3.61E+009	1.80E+001	0 - 0.5 cm
Run #5	01:11:11 PM 92.52	1.00E-009	1.26E-010	2.13E+003	2.62E+003	1.58E+010	1.94E+010	2.30E+001	0 - 0.5 cm
Run #6	01:14:49 PM 105.09	9.64E-010	1.16E-010	2.33E+003	4.95E+003	1.73E+010	3.66E+010	2.22E+001	0 - 0.5 cm
Run #7	01:26:43 PM 35.11	9.69E-010	3.37E-011	7.83E+002	5.73E+003	5.80E+009	4.24E+010	2.23E+001	0 - 0.5 cm
	01:56:20 PM	FC Lkg (A): -4.25E-013 ± 1.650E-13							
		SEMLkg (A): 9.65E-013 ± 7.457E-13							
	03:47:01 PM	FC/SEM Ratio: 1.50E+000 ± 1.2548E-03							
Run #8	03:49:36 PM	FC/SEM Ratio: 1.50E+000 ± 1.2548E-03							
Run #9	03:52:07 PM 129.42	5.02E-009	2.11E-010	1.50E+004	7.11E+003	1.02E+010	5.26E+010	1.08E+002	0 - 0.5 cm
Run #10	04:05:37 PM 6.52	5.16E-009	7.46E-011	7.75E+002	2.21E+004	1.11E+011	1.63E+011	1.16E+002	0 - 0.5 cm
Run #11	04:07:29 PM 35.42	4.81E-009	4.11E-010	3.92E+003	2.28E+004	5.73E+009	1.69E+011	1.19E+002	0 - 0.5 cm
Run #12	04:11:11 PM 21.23	4.89E-009	1.02E-009	2.39E+003	2.68E+004	2.90E+010	1.98E+011	1.11E+002	0 - 0.5 cm
Run #13	04:14:19 PM 10.11	4.82E-009	1.45E-009	1.12E+003	2.92E+004	1.77E+010	2.16E+011	1.13E+002	0 - 0.5 cm
Run #14	04:16:03 PM 38.56	5.19E-009	3.09E-010	4.61E+003	3.03E+004	8.30E+009	2.24E+011	1.11E+002	0 - 0.5 cm
Run #15	04:22:05 PM 113.27	5.01E-009	5.02E-010	1.31E+004	3.49E+004	3.41E+010	2.58E+011	1.19E+002	0 - 0.5 cm

Proton300k™ Encryptor

TTMR™ & HCore-2™ combined with Xilinx Virtex FPGA provides Radiation Hardened, reconfigurable computing platform.

RH Reconfigurable Encryptor Application Of Proton300k™ :

Capabilities:

- ✧ >4Gbps encryption speed
- ✧ >1,000 tunnels, NSA Type 1 encryption
- ✧ TID >100 krad(Si)
- ✧ SEU <1E-3 unrecoverable errors/day
- ✧ SEFI Fully recoverable

Summary of Results:

A very high-speed, HAIPE compatible Encryptor, in-orbit reprogrammable

