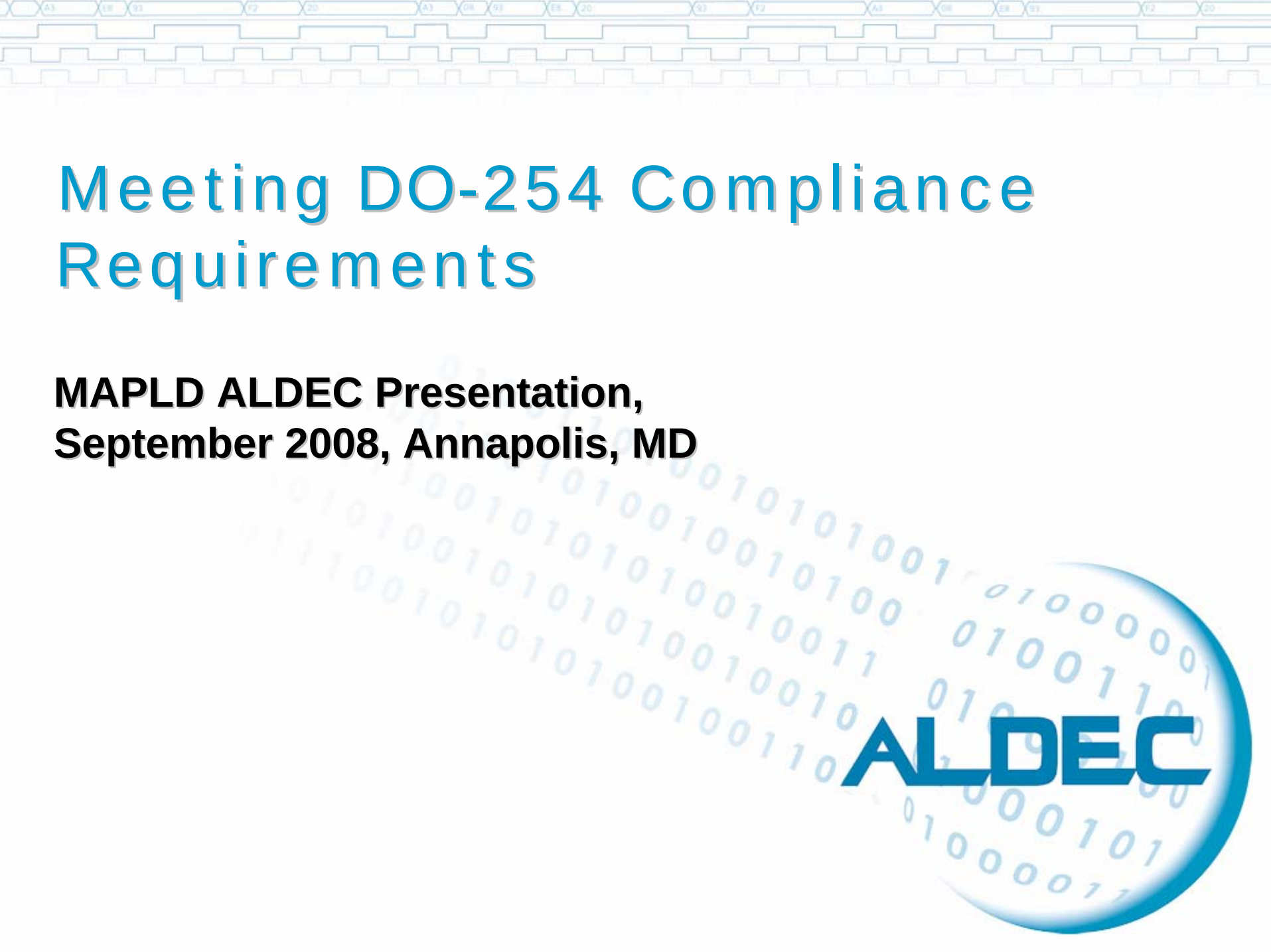
Meeting DO-254 Compliance Requirements

MAPLD ALDEC Presentation,
September 2008, Annapolis, MD



Outline

- Aldec background and position in DO-254 Compliant Design Process
- Verification in Hardware with Requirements Traceability
- Independent Tool Qualification
- Summary

Aldec DO-254 Position

1. **Verification in Hardware with Requirements Traceability**

   Objective: Fast and reliable design verification process accepted by the certification authorities

   Solution: Aldec/DO-254 CTS

   Supports: Chapter 6.2 (Verification Process) of DO-254 document

2. **Tool Qualification Process**

   Objective: Independent Tool Qualification

   Solution: Aldec/DO-254 CTS (Compliance Tool Set)

   Supports: Chapter 11.4 (Tool Assessment and Qualification) of DO-254 document

Aldec Verification Technology and Experience

- Aldec is a verification expert, focused on multi-domain verification tools
- Aldec has several key patents in verification technology
- Aldec/DO-254 CTS built from proven components; 20+years in business, 30,000+ licenses issued worldwide
- Development Centers in the European Union
- Direct Technical Support in Europe, USA and Japan
- Broad customer base in Aerospace and Defense Industry
- Relationships with DER and DO-254 service organizations and FPGA vendors (Actel, Altera, Geensys, HighRely, others)

Design Verification for DO-254

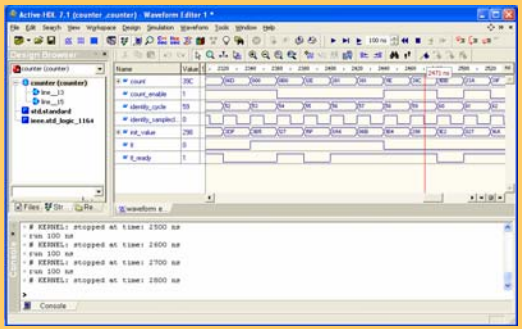
"Since the results depend on the models and scenarios employed, **simulation results alone cannot be used for the purpose of certification credit without supporting evidence of their validity.**"

Chapter 6.3.2
DO-254 Specification, Apr 19, 2000.

"Verification methods, such as tests, **simulation , prototyping**, analyses and reviews, should be selected and performed."

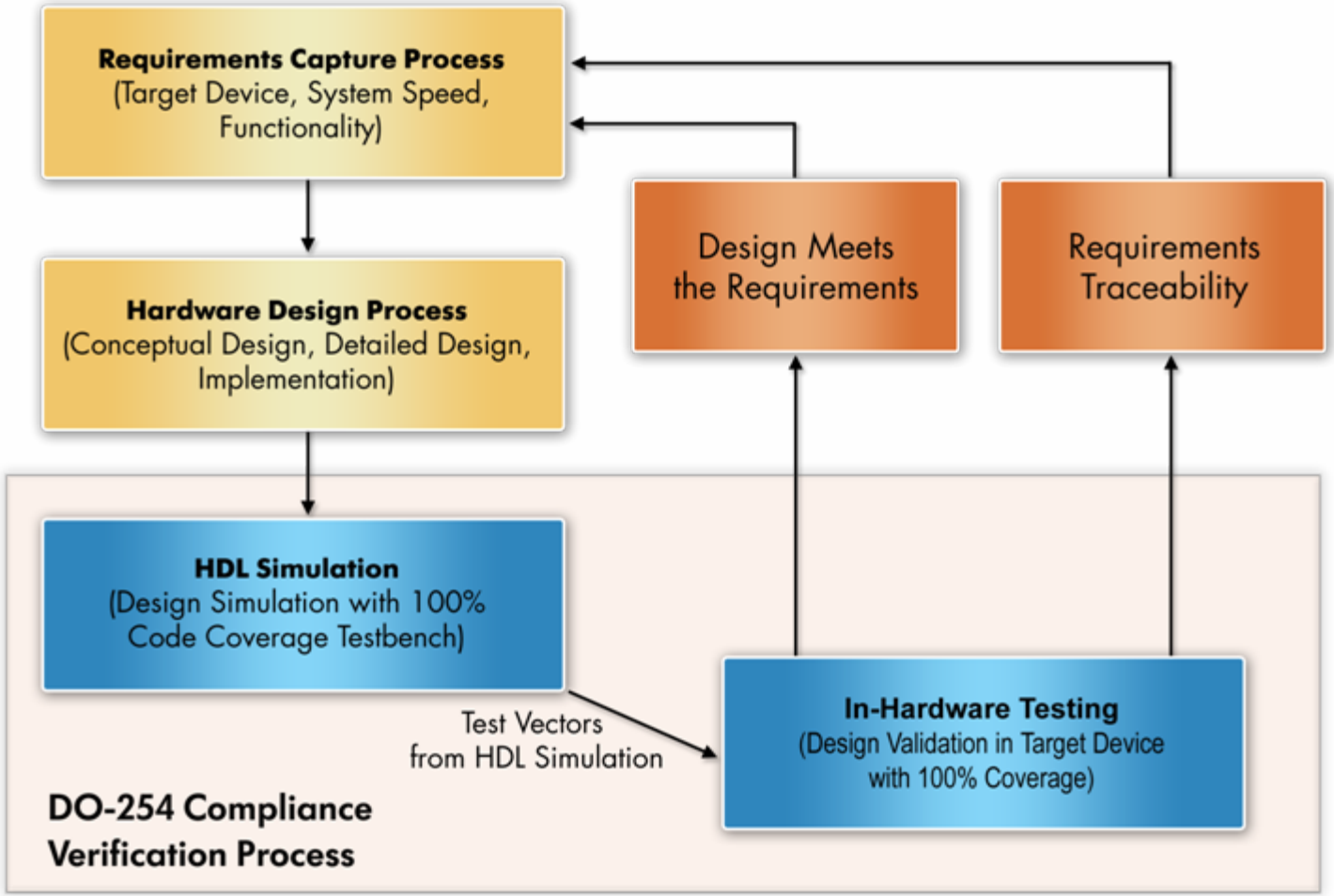
Chapter 6.2.2
DO-254 Specification, Apr 19, 2000.

Verification in Simulator



Verification in Hardware

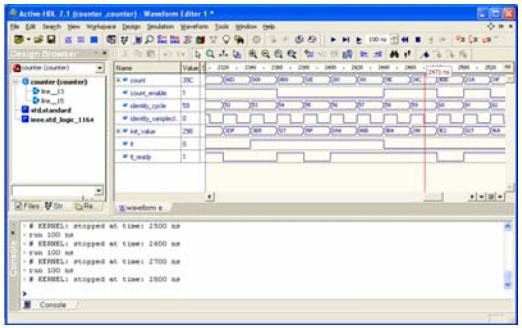
Design Verification for DO-254



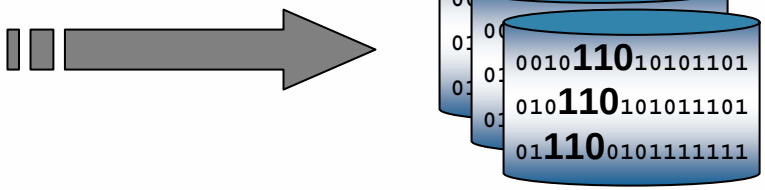
RTL, Netlist and Timing Simulation

- Simulation is driven by the set of testbenches
- Results are stored in the signal database files (waveforms, etc)
- Simulation levels tested
  - Functional simulation
  - Gate-Level netlist simulation
  - Timing simulation
- All tested levels reuse the same testbenches

HDL Simulator



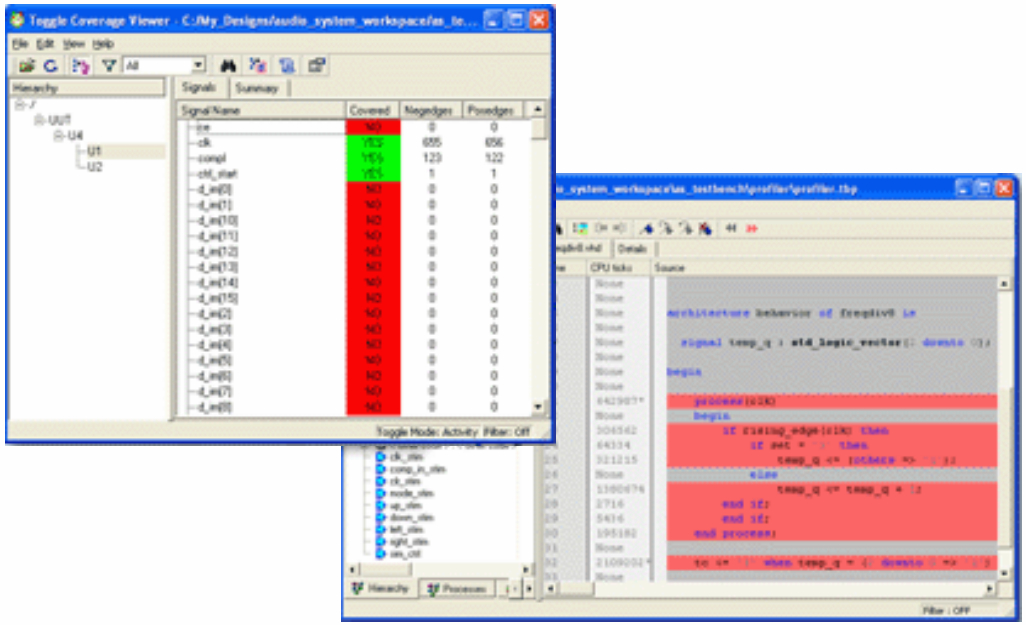
Results of RTL Simulation – Signal DB files



Analysis Tools with HDL Simulation

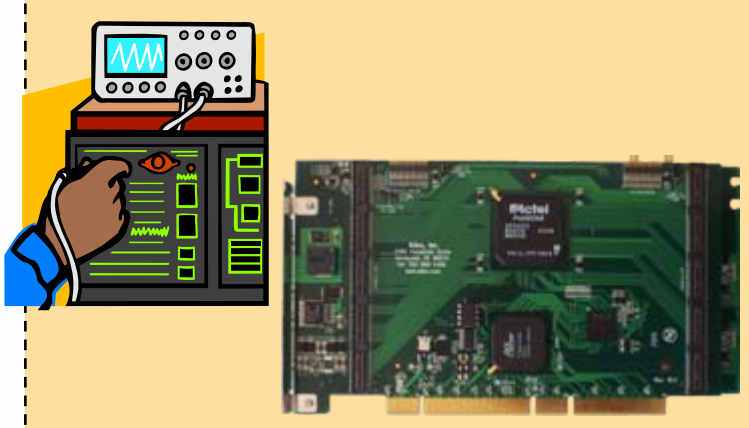
- **Code Coverage**
  - Statement coverage
  - Branch coverage
  - Toggle coverage
  - Expression coverage
- **Code Linting**
  - Coding Styles rules
  - Design for Test rules
  - Design Style rules
  - Simulation rules
  - Synthesis rules

Active-HDL & Riviera Analysis Tools



Traditional Testing in Hardware

- Real-time stimuli are streaming through the design inputs
- Design outputs (FPGA) are connected to other discrete components on the board



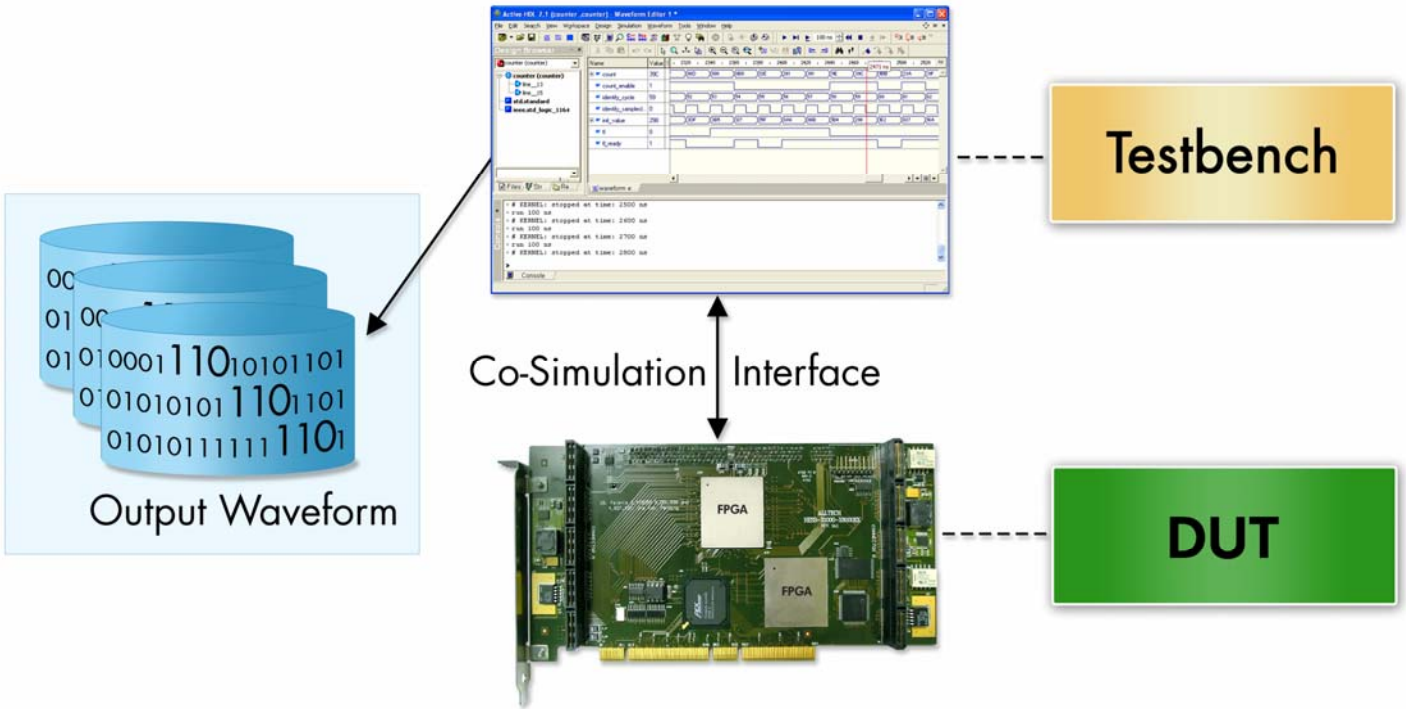
Challenges

- Limited Controllability of Design Inputs
- Limited Traceability of Design Outputs

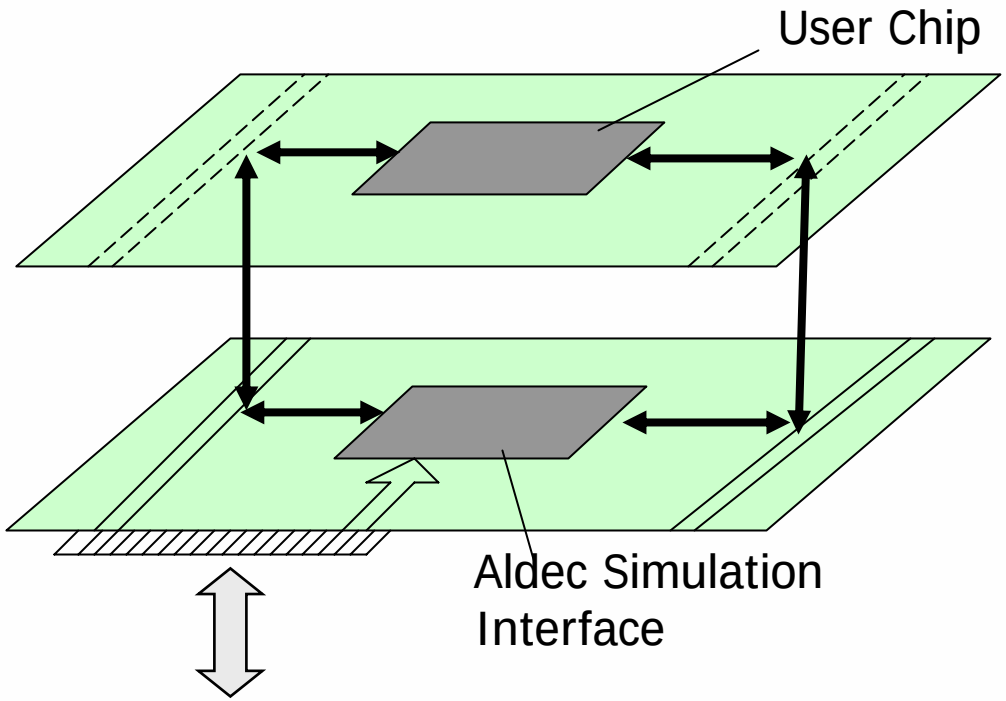
- Special analysis is used to prove the coverage of all testing requirements

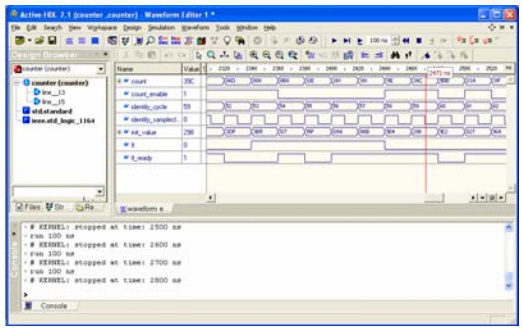
Functional In-Hardware Simulation

- The FPGA design is implemented to target FPGA on Custom Daughter Board
- The simulation is driven by the same testbench used for RTL simulation
- HDL simulator drives input and reads output of the design circuit inside FPGA
- The results of the In-Hardware Simulation are stored in the waveform file



Aldec Hardware Architecture



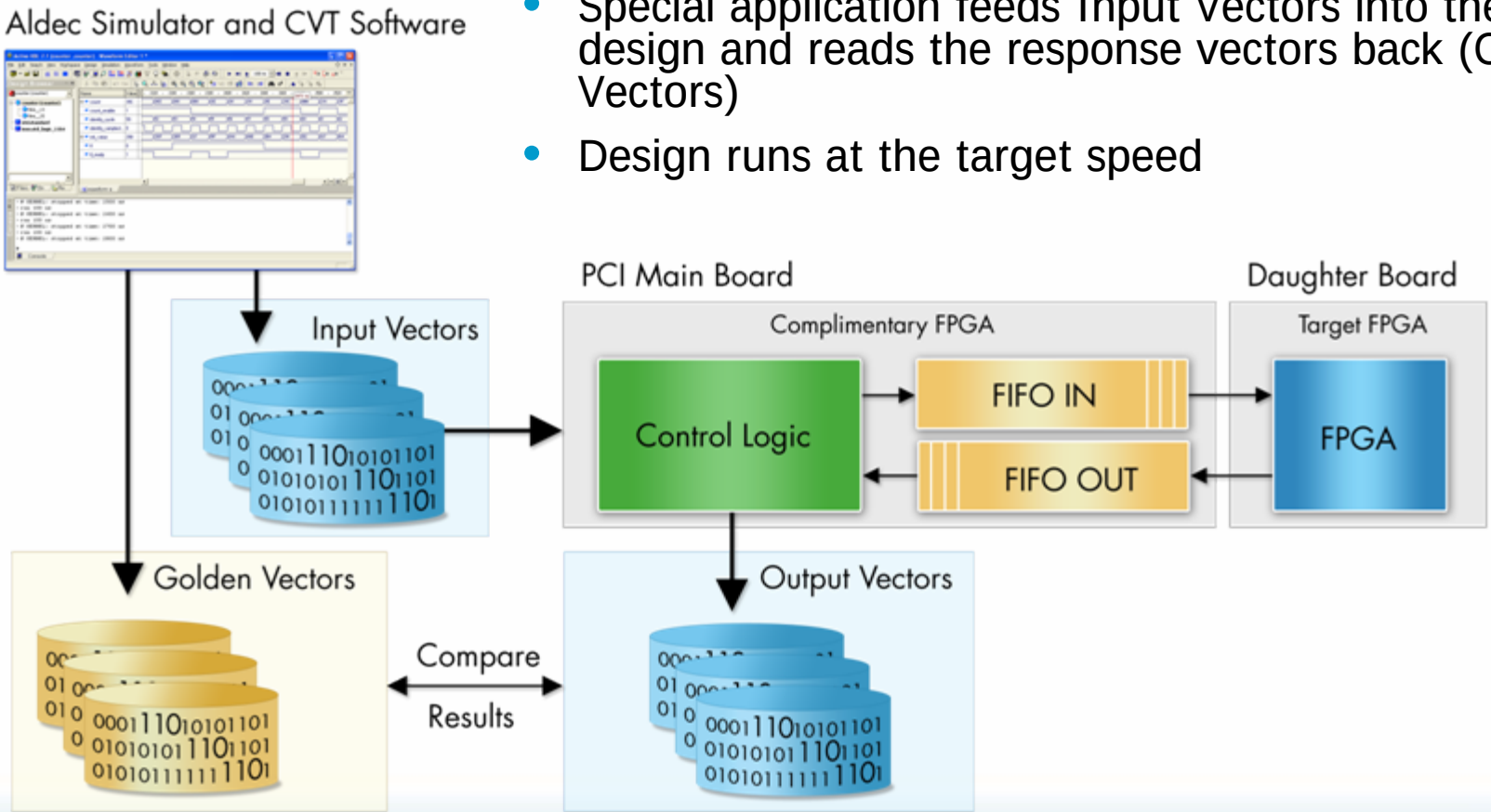


Simulation Flow:

1. Run synthesis and P&R for user design
2. Program user chip with the design
3. Start and run simulation in Aldec simulator (Active-HDL)
4. If the design was modified go back to step 1.

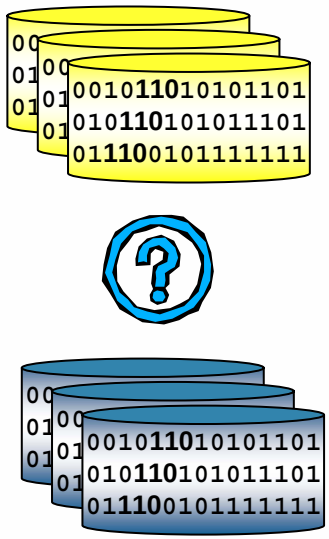
In-Hardware Simulation at Speed

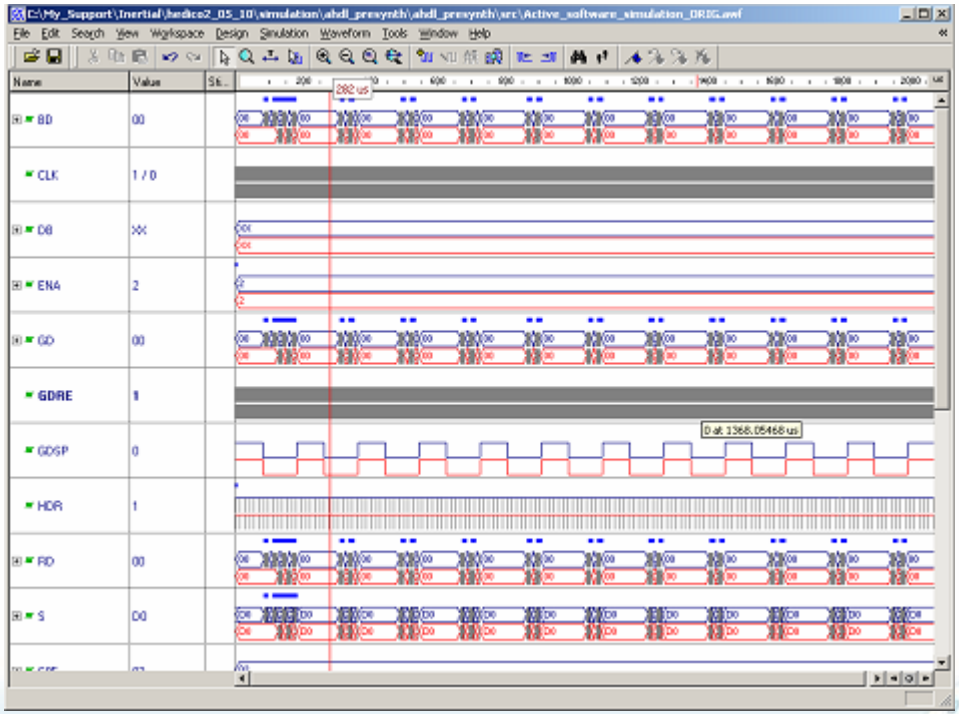
- Input Vectors can be custom created to check any test requirement
- Special application feeds Input Vectors into the design and reads the response vectors back (Output Vectors)
- Design runs at the target speed



Hardware Output Validation

- Visual analysis of generated waveforms
- Golden vectors are generated during RTL simulation
- Output vectors captured from Hardware are compared
  - graphically as waveform files
  - as two binary files





In-Hardware Simulation in DO-254 Spec

In-Hardware Simulation is a Test method of verification.

"Test is a method that confirms that the hardware item correctly responds to a stimulus or series of stimuli. Examples of tests include functional test on the hardware item, (...)"

Chapter 6.3.1
DO-254 Specification, Apr 19, 2000.

DO-254 Specification Test Guidance Recommendations

"The testing stimulus, sequence and test conditions, (...), should be defined for each test."

> In-Hardware Simulation tests use stimuli and sequences captured from HDL simulation. Thus identification of stimuli is automated and well suited to the certification process.

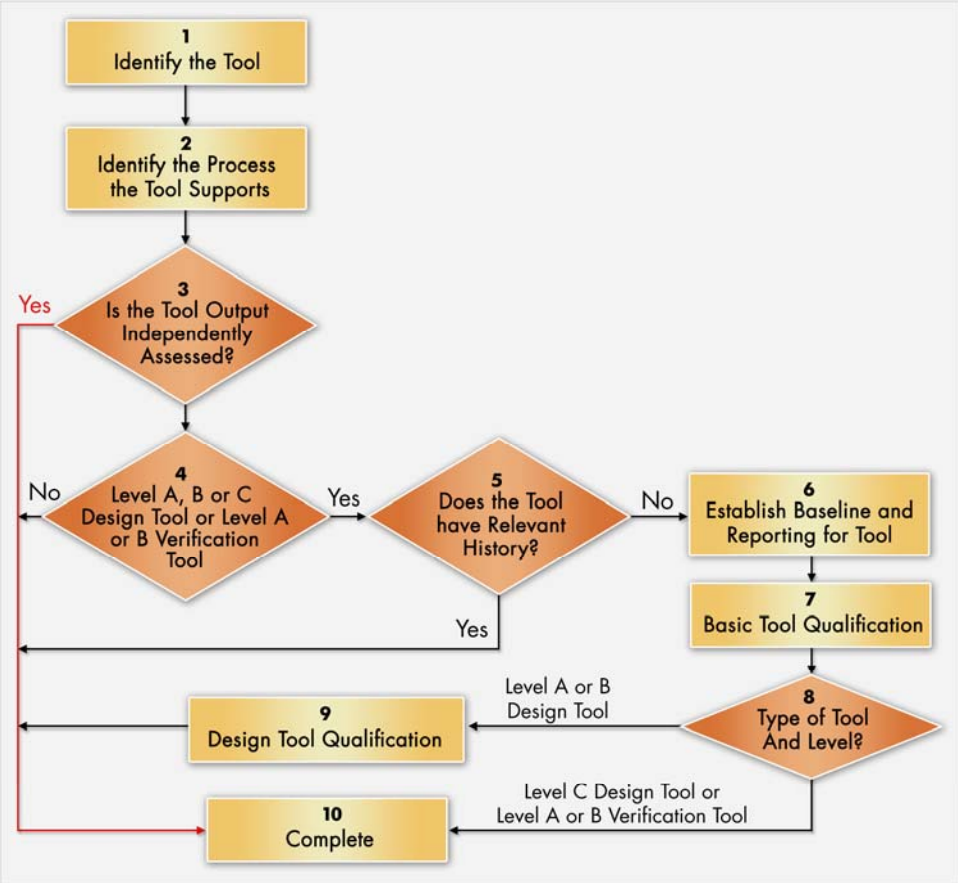
"Pass/fail criteria and a method for recording the results should be defined prior to test execution."

> In-Hardware Simulation provides method for capturing and recording results from hardware. The ASDB or VCD waveforms can be recorded.
>
> Recorded waveforms can be compared to HDL simulation results (by waveform comparison tool). Pass/fail criteria is based on automatic comparison of waveforms.

"Test results should be recorded and retained."

> Recorded waveforms can be retained as reference.

Tool Assessment and Qualification Process



Design and Verification Tool Assessment and Qualification flow chart (ch.11.4)

Tool Assessment and Qualification Process

Main purpose of the process: *to ensure the tool is capable of performing the particular design and verification activity to an acceptable level of confidence* (...).

Tool Assessment and Qualification Process:

- Identify the Tool (name, source, version, environment etc).
- Identify the Process the Tool Supports (design or verification process).
- Is the tool independently assessed?

An independent assessment verifies the correctness of the tool output using an independent means. If the tool output is independently assessed, then no further assessment is necessary.

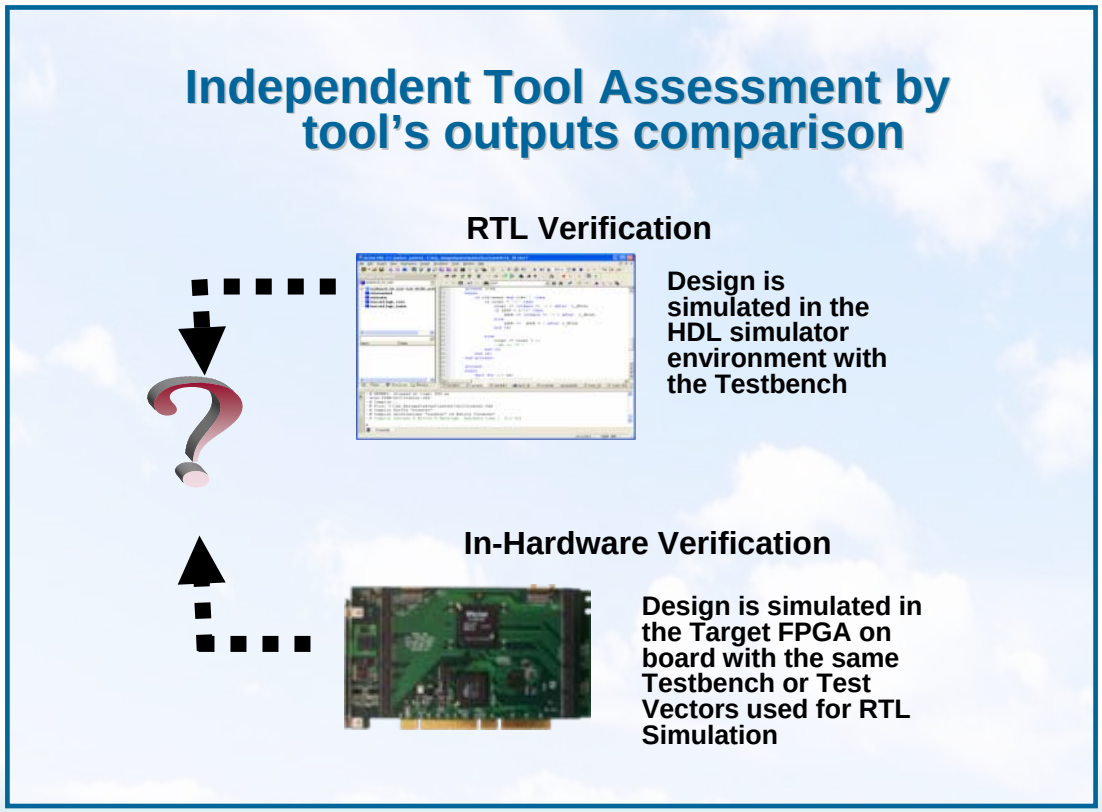
A tool assessment should be performed prior to the use of a tool.

Source: chapter 11.4 of DO-254/ED80 Specification

Independent Tool Assessment with Aldec/DO-254 CTS

"Independent assessment of a design tool's output may include a manual review of the tool outputs or may include a comparison against the outputs of a separate tool capable of performing the same verification activity as the tool being assessed.

Chapter 11.4.1.3, DO-254 Specification, Apr 19, 2000.

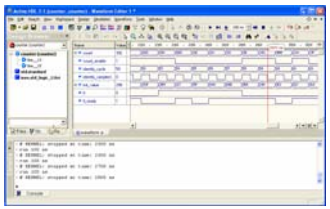


Independent Verification Environment

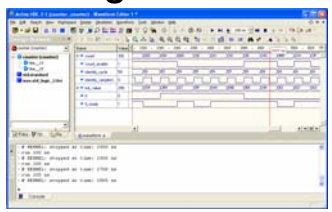
Testbench | Design Files | Simulation Scripts

ALDEC DO-254 CTS

HDL Simulator
(Verification Tool used
in DO-254 Verification Process)

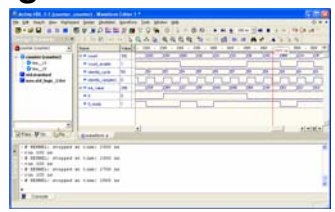


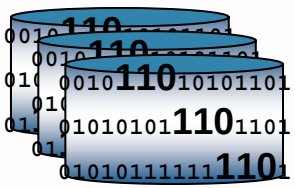
Tool Qualification Using Simulator

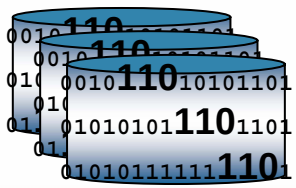


or

Tool Qualification Using Hardware Simulator







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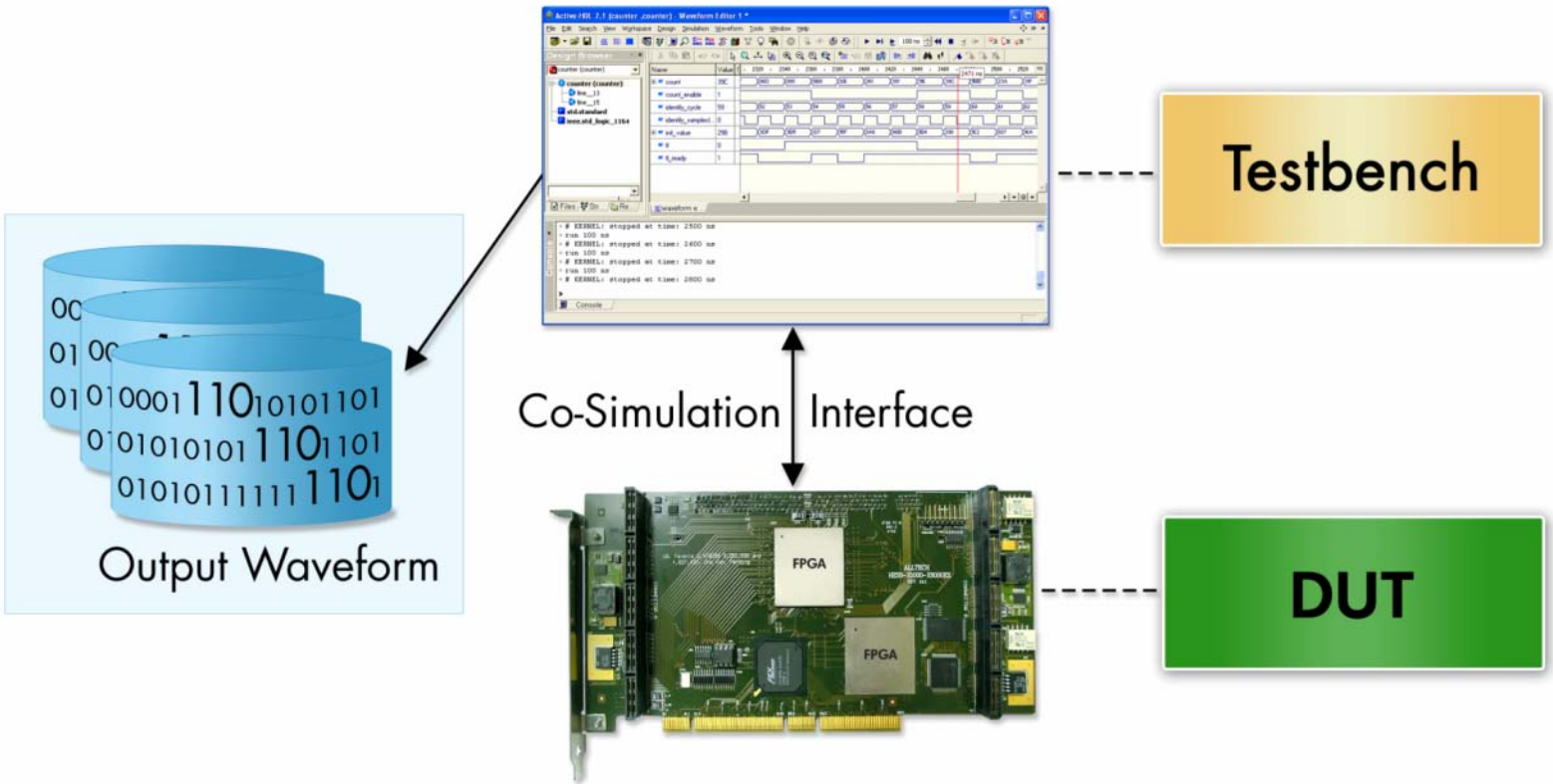
Qualification Process – Chapter 11.4

Tool Qualification with Hardware Simulation

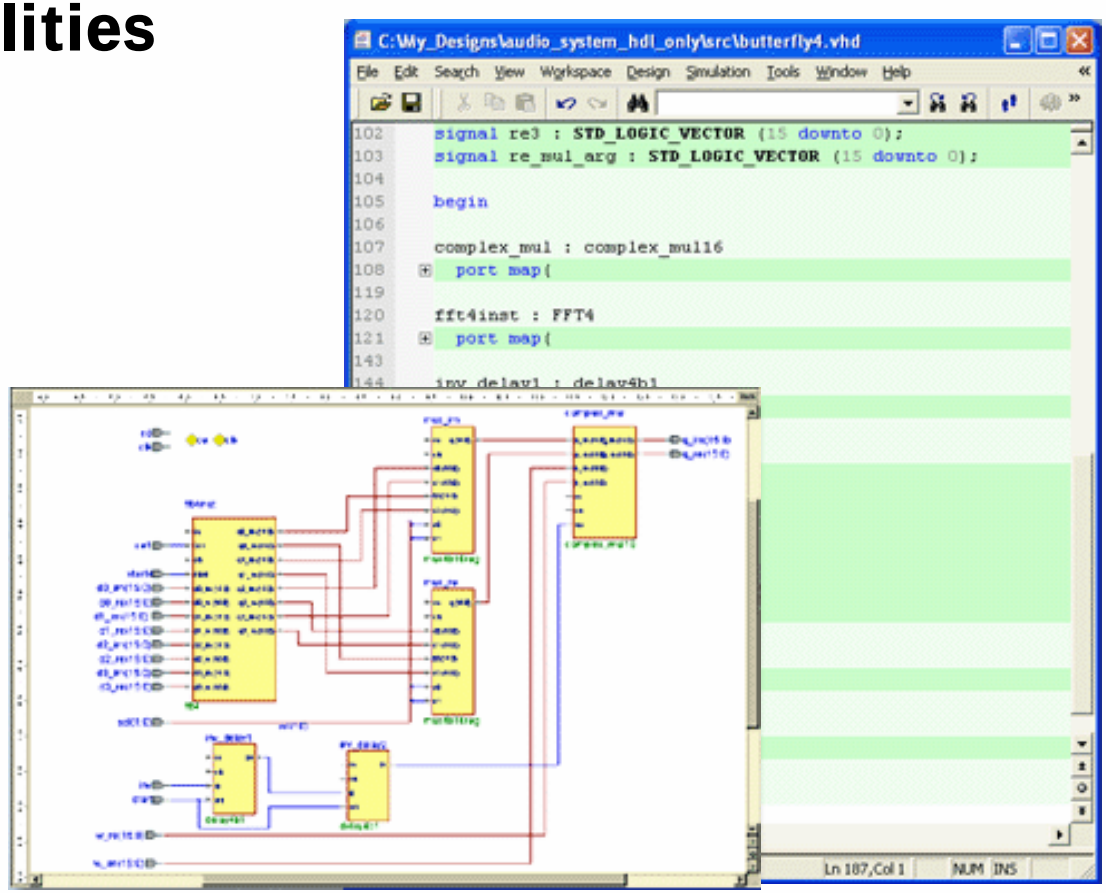
- The results of In-Hardware Simulation are stored in the waveform file and compared against the software simulator output



Documenting User's Design

Documentation capabilities

- **Code2Graphics**
  - Converts HDL code into graphical representation
    - Block Diagrams
    - Bubble Diagrams (FSM)
- **Export to HTML**
- **Export to PDF**



Summary: Aldec/DO-254 CTS

- Functional and at-speed verification of the design implementation in target hardware
- Target Device without any extra circuits or functions is used in the solution
- Target Device uses RTL simulation test vectors for inputs (high controllability of design inputs)
- In-Hardware Simulation results stored in the waveform format for easy analysis and maintaining
- Independent Tool Assessment (easy tool Qualification)
- Automated results comparison methodology
- Complete traceability of all design outputs
- Code Coverage, and Code Linting analysis