A BREADBOARD FOR REAL-TIME IMAGE PROCESSING ON BOARD GAIA

**THE PRINCIPLES OF BREADBOARDING**

In this first version, the processor is realized on a daughter-board, the memories are mounted on an intermediate board and the two boards are interconnected through a standard interface.

**FIRST VERSION OF THE DEMONSTRATOR**

In this poster, we chose to address the task 1. The sequence of processes needed is explained to the right.

**THE TECHNICAL CONSTRAINTS**

Due to the need for a real-time processor to retrieve data from the output SRAM, we have chosen to test this experimental version in an extensive way to identify problems and secure the development of a second version.

**A CASE STUDY**

To remedy these problems, two directions were investigated.

**TOWARDS A VERSION 2.0**

The second version will feature:

**CONCLUSION**

We conclude that the hardware architecture is well suited for the purpose of the real-time image processing onboard Gaia.