Using Fusion Mixed-signal FPGAs to Implement System Management in µTCA Applications

Mike Brogley
Product Marketing Manager, System Applications
and
Ken O'Neill
Director, High Reliability Product Marketing
Actel Corporation

Agenda

- TCA Hardware Platform Management Challenges
- Traditional Design using Discrete Devices
- Mixed-signal FPGA Advantages
- Design Examples
- Lessons Learned
- Conclusions
- Contact Information

TCA Hardware Platform Management Challenges

- Startup and Power Sequencing
- Power, Current, and Temperature Monitoring
- IPMI Communications
- Interoperability
- Thermal and Power Management
- Redundancy and Reliability
- Manufacturability

Traditional Solutions using Discrete Devices

- Startup and Power Sequencing
  - **Limited configurability**
  - **“All sizes fit one”**
- Power, Current and Temperature Monitoring
  - **Limited customization**
  - **“All sizes fit one”**
- IPMI
  - **Multiple I2C devices**
  - **Must be managed by external processor**

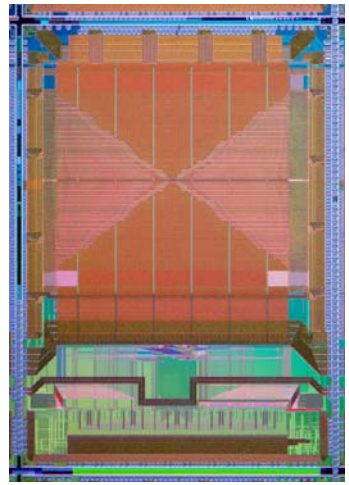
Traditional Solutions using Discrete Devices, continued

- Interoperability
  - **Designs required to “Play Well With Others”**
  - **Firmware-centric solutions challenged in spec-driven critical timing requirements**
- Thermal and Power Impact
  - **High BOM counts**
  - **Power budgets**
  - **Chassis thermal loading**

Traditional Solutions using Discrete Devices, continued

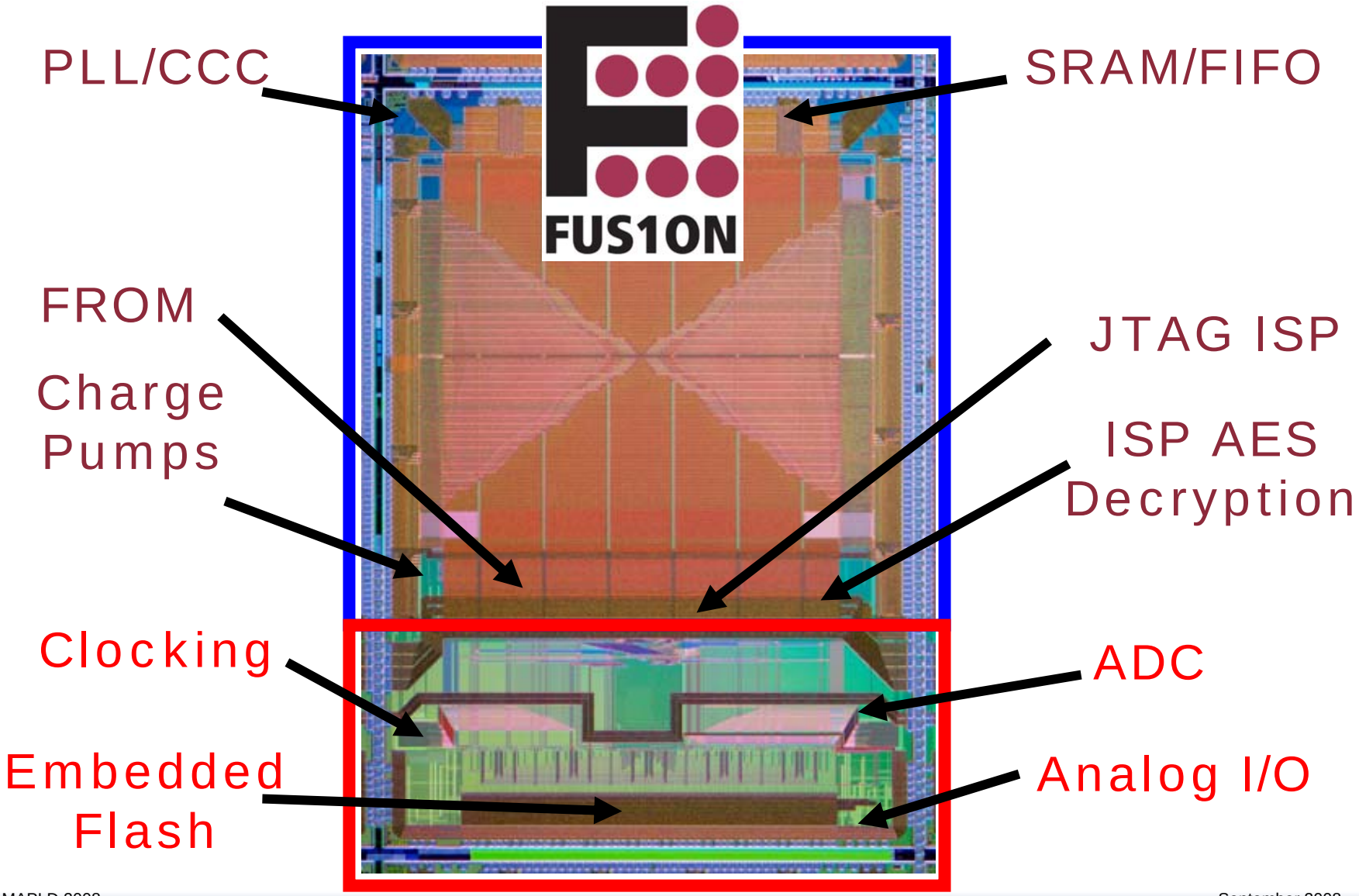
- Redundancy and Reliability
  - **Every discrete part is a new single point of failure**
- Manufacturability
  - **High BOM count:**
    - **Increases board layout time**
    - **Increases required board layers**
    - **Increases routing complexity (thru-holes, vias)**
    - **Increases assembly expense**
    - **Increases BOM kitting challenges**

Mixed-Signal FPGA Advantages

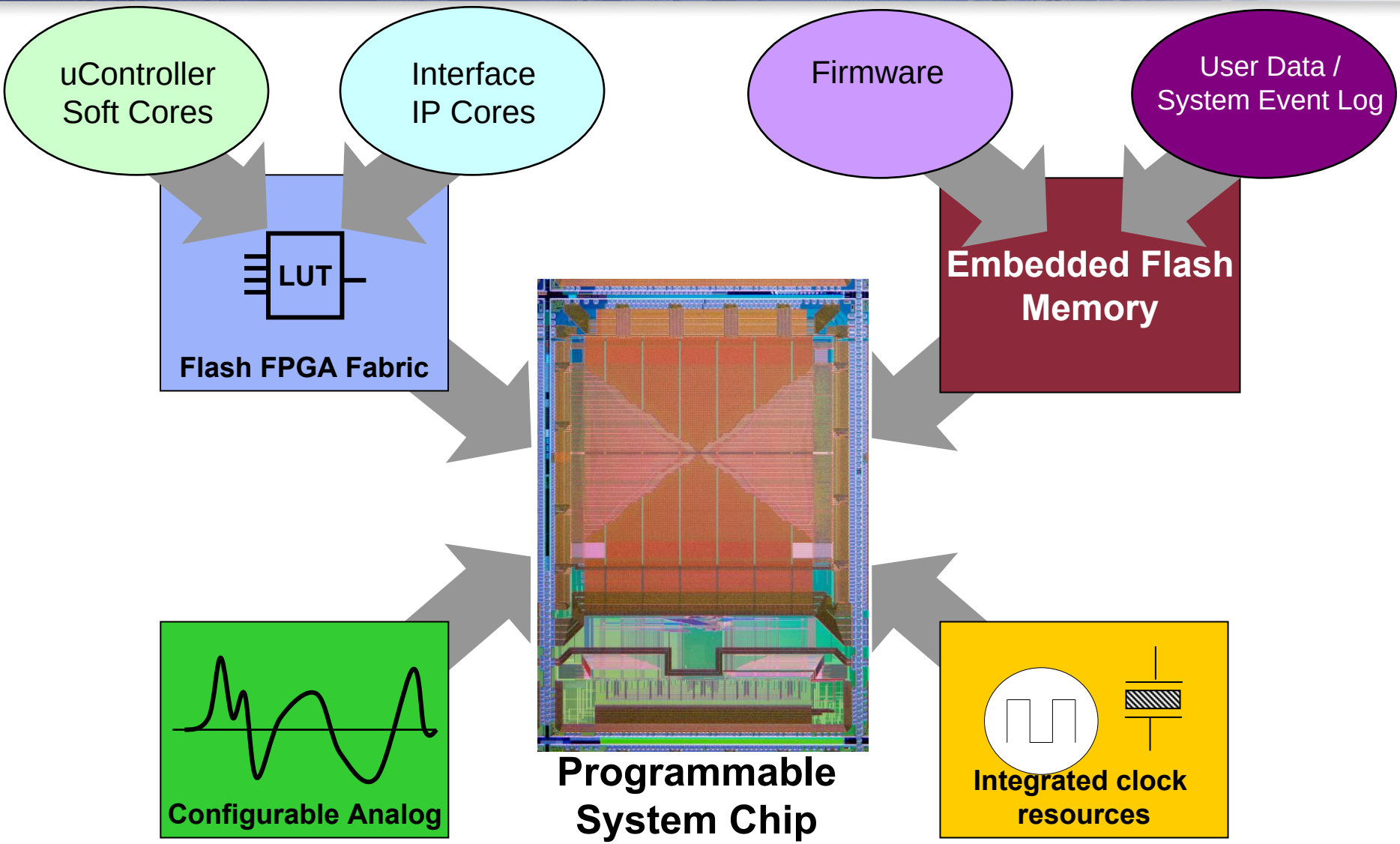


- Intrinsically Low Power
- Extensive Security Features
- Live at Power Up
- Reprogrammable
- Intrinsically Great Noise Immunity
- Voltage, Current and Temperature Monitoring
- FET Driver Outputs
- On-chip NVM
- Configurable Clocking Resources
  - **Internal RC oscillator, Crystal Oscillator, CCC/PLL and Real Time Counter**
- Embedded CPUs
  - **CoreABC, 8051 and ARM Cortex-M1 processor**
  - **8051**
  - **Cortex-M1**

Fusion: Actel's Mixed Signal FPGA



Actel FPGA


uController
Soft Cores
Interface
IP Cores
Firmware
User Data /
System Event Log
LUT
Flash FPGA Fabric
Embedded Flash
Memory
Programmable
System Chip
Configurable Analog
Integrated clock
resources

Integration Advantages of Mixed-Signal FPGAs

- BOM Integration
- Board Design Simplification
- Reduced Thermal Loading
- Reduced Points of Failure
- Increased Design Flexibility
- Reprogrammability
- Customizability

Mixed-Signal FPGA Design Approach

- Leverage Existing Pre-built IP and Minimize Full-custom Development
- Maximize Design Flexibility,
  - **Taking advantage of FPGA reprogrammability**
- Maximize Design Reuse,
  - **Particularly for common elements in standards-driven designs**
- Partner with Industry Leaders
- Design to Accommodate Real Customer Needs

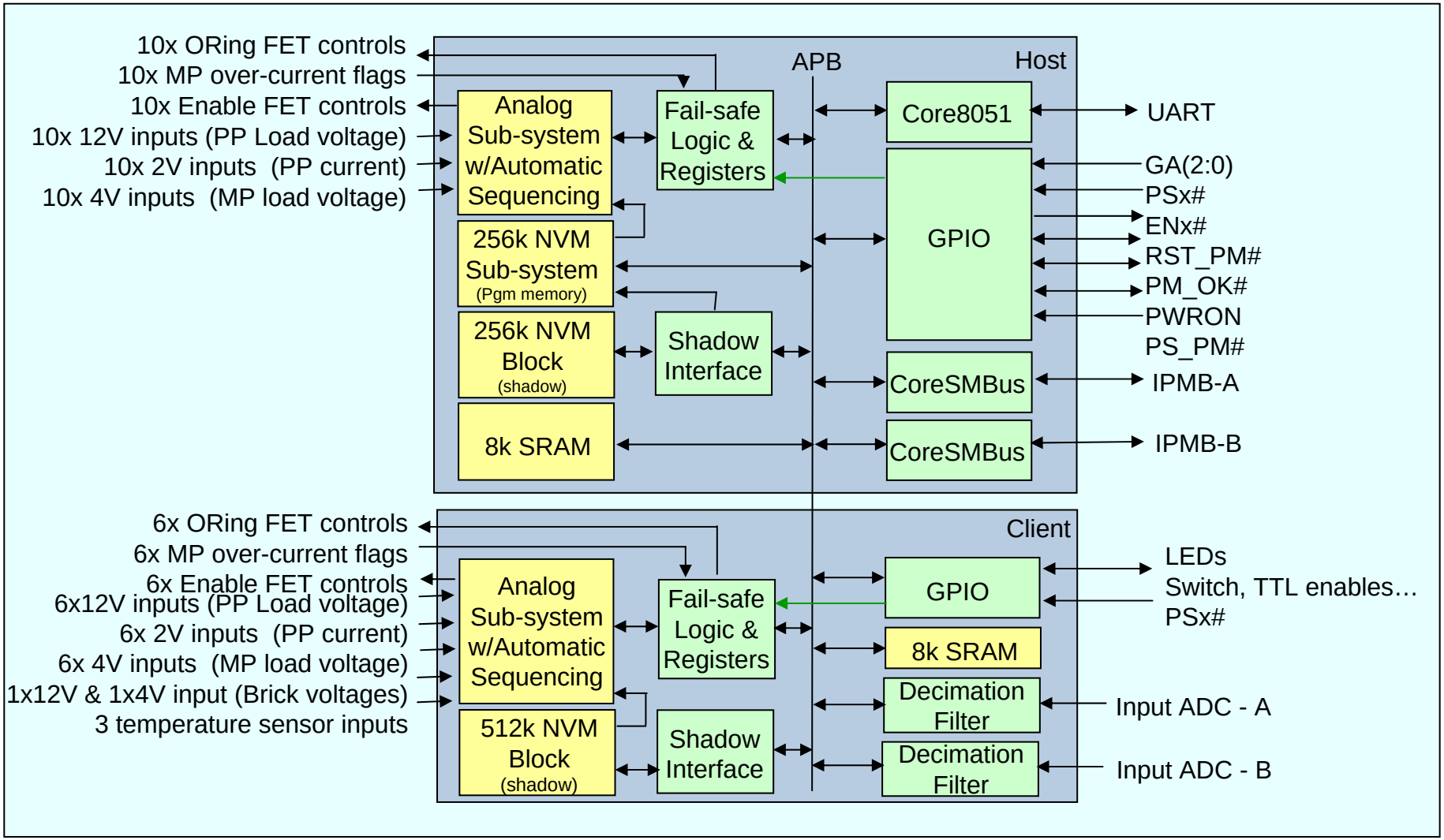
Mixed-Signal FPGA Results

- BOM Total Parts Count Reduction
  - **µTCA PM: 53% (from ~800 parts to ~370)**
  - **ATCA IPMC core: 39%**
  - **ATCA AMC Carrier w/8 AMC sites: 37%**
- BOM Cost Reduction
  - **µTCA PM: 23%**
  - **ATCA IPMC core: 11%**
  - **ATCA AMC Carrier: 27%**
- Board Area Reduction
  - **µTCA: 27%**
  - **ATCA IPMC core: 38%**
  - **ATCA AMC Carrier: 38%**

Design Example: MicroTCA Power Module

- Integrated Power Management for MicroTCA Chassis
- Fusion FPGA plus 8051 processor Enhanced Module Management Controller (EMMC)
  - **Continuous monitoring of >60 different analog signals**
  - **Monitor voltage, current and primary shut-off every 100ms on 32 channels**
  - **Programmable current limit 40ma increments to 10 amps**
  - **During payload power failure with standby management power**
  - **All inputs and outputs continue to be monitored**
  - **All management functions are fully operational**
  - **Redundant I2C IP platform**
  - **Independent channels can be primary or backup with redundant PMs**
  - **Gate logic implemented failure mode response**

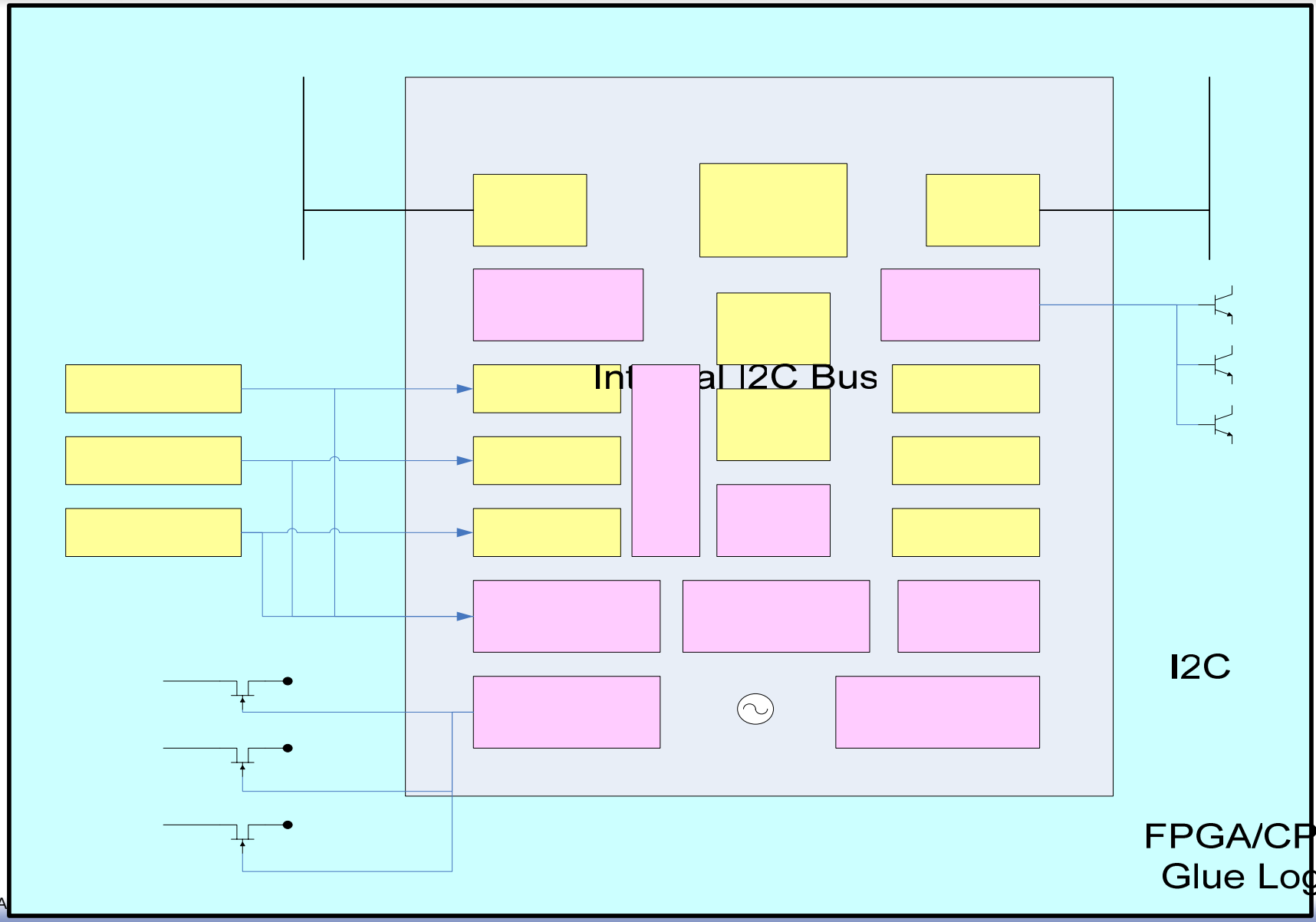
MicroTCA Power Module (EMMC)



Design Example: Advanced Mezzanine Card (MMC)

- Integrated board monitoring, power management and communications MMC
- On-board analog and digital processing
  - **Core8051s processor**
  - **Dual CoreI2C for IPMI**
  - **Fusion analog processing block**
  - **CoreUARTapb and CoreGPIO blocks**
  - **CorePWM controls variable load payload**
- Load Board Payload
  - **Reference design provides variable load and system monitoring**

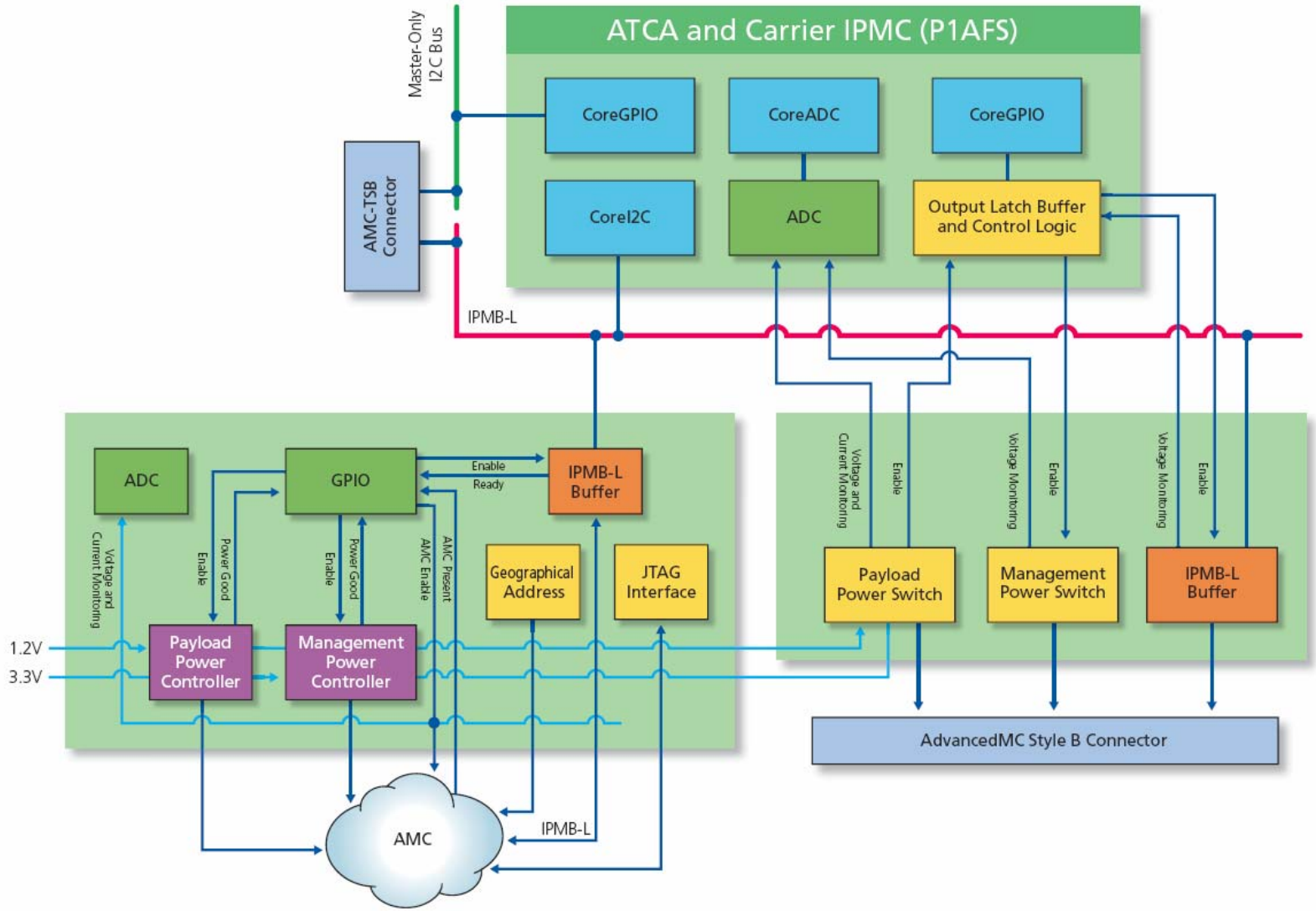
Advanced Mezzanine Card (MMC)



Design Example: AMC Carrier (Carrier IPMC)

- Management controllers for ATCA AMC Carrier blades
- Fusion FPGA with ARM Cortex-M1 soft processor core
- Digital Logic in Standard IP
  - **CoreI2C, CoreUartApb, CoreABC, CoreMBX and CoreAI alongside bus fabric cores**
- Analog Offload with Standard IP
  - **CoreAI used as the analog engine**
    - **Raw ADC sampling**
  - **CoreABC used as the closed loop control of the analog engine**
    - **Autonomous threshold detection**
  - **CoreMBX used as the communication medium between the Cortex-M1 and CoreABC processors**
    - **CoreABC interrupts Cortex-M1 based on certain events via CoreMBX**

AMC Carrier Architecture



BOM Comparison: IPMC Core Only

H8S PPS IPMC BOM (IPMC Core)

QTY	PART#	Desc	unit price	ext price
1	HD64F2166	H8S	$ 23.400	$ 23.40
1	ECS-2100AX-073.7	oscillator 7.3728MHz	$ 1.063	$ 1.06
1	TPS3103K33	reset generator	$ 1.103	$ 1.10
2	LTC4300A-1	LTC4300A-1	$ 2.000	$ 4.00
1	LTC1754	LTC1754	$ 1.550	$ 1.55
1	SN74LVC2G06	SN74LVC2G06	$ 0.104	$ 0.10
1	DS1815R	latch buffer and its control	$ 0.468	$ 0.47
1	SN74LVC2G132	SN74LVC2G132	$ 0.160	$ 0.16
1	SN74LVTH16373	SN74LVTH16373	$ 0.440	$ 0.44
1	AD1582A	external reference	$ 0.813	$ 0.81
1	DS75	thermal sensor digital	$ 0.912	$ 0.91
1	AT24C32/64	serial EEPROM	$ 0.640	$ 0.64
0	SN74LVTH16373	latch buffer	$ 0.440	$ -
13		Parts Subtotal		$ 34.65
		Assembly Cost	$ 0.050	$ 0.65
		TOTAL		**$ 35.30**

Fusion PPS IPMC BOM (IPMC Core)

QTY	PART#	Desc	unit price	ext price
1	P1AFS600-FGG256	PPS + Cortex-M1 enabled Fusion FPGA	$ 25.000	$ 25.00
1	CTS636, 25MHz	oscillator	$ 1.020	$ 1.02
1	DS1815R	reset generator	$ 0.468	$ 0.47
1	2SD2391	1.5V regulator transistor	$ 0.021	$ 0.02
2	LTC4300A-1	LTC4300A-1	$ 2.000	$ 4.00
1	MMBT3904	thermal sensor analog	$ 0.017	$ 0.02
1	AT24C32/64	serial EEPROM	$ 0.640	$ 0.64
8		Parts Subtotal		$ 31.17
		Assembly Cost	$ 0.050	$ 0.40
		TOTAL		**$ 31.57**

-39% Improvement in BOM total parts count
-10% Savings, BOM only cost
-11% Savings, total cost incl. assembly
-38% reduction in core board area (1,140mm2 vs. 708mm2): $4 savings per board

BOM Comparison: AMC Carrier (8 AMC sites)

H8S PPS Carier IPMC BOM with 8 AMC sites

QTY	PART#	Desc	unit price	ext price
1	HD64F2166	H8S	$ 23.400	$ 23.40
1	ECS-2100AX-073.7	oscillator 7.3728MHz	$ 1.063	$ 1.06
1	TPS3103K33	reset generator	$ 1.103	$ 1.10
2	LTC4300A-1	LTC4300A-1	$ 2.000	$ 4.00
1	LTC1754	LTC1754	$ 1.550	$ 1.55
1	SN74LVC2G06	SN74LVC2G06	$ 0.104	$ 0.10
1	DS1815R	latch buffer and its control	$ 0.468	$ 0.47
1	SN74LVC2G132	latch buffer and its control	$ 0.160	$ 0.16
1	SN74LVTH16373	latch buffer and its control	$ 0.440	$ 0.44
1	AD1582A	external reference	$ 0.813	$ 0.81
1	DS75	thermal sensor digital	$ 0.912	$ 0.91
1	AT24C32/64	serial EEPROM	$ 0.640	$ 0.64
8	SN74LVTH16373	latch buffer	$ 0.440	$ 3.52
16	LTC4210	LTC4210	$ 3.100	$ 49.60
8	IRMLS2002	IRMLS2002	$ 0.040	$ 0.32
8	STD95N4F3	STD95N4F3	$ 0.838	$ 6.70
16	MIC841	MIC841	$ 0.468	$ 7.49
8	LTC4300A-1	LTC4300A-1	$ 2.000	$ 16.00
8	SN74LVC02A	SN74LVC02A	$ 0.120	$ 0.96
8	SN74LVC1G08	SN74LVC1G08	$ 0.166	$ 1.33
8	SN74LVC1G38	SN74LVC1G38	$ 0.096	$ 0.77
101		Parts Subtotal		$ 121.34
		Assembly Cost	$ 0.050	$ 5.05
		TOTAL		**$ 126.39**

Fusion PPS Carrier IPMC BOM with 8 AMC sites + SoL(PT or SPT modes)

QTY	PART#	Desc	unit price	ext price
1	P1AFS600-FGG256	PPS + Cortex-M1 enabled Fusion FPGA	$ 25.000	$ 25.00
1	CTS636, 25MHz	oscillator	$ 1.020	$ 1.02
1	DS1815R	reset generator	$ 0.468	$ 0.47
1	2SD2391	1.5V regulator transistor	$ 0.021	$ 0.02
2	LTC4300A-1	LTC4300A-1	$ 2.000	$ 4.00
1	MMBT3904	thermal sensor analog	$ 0.017	$ 0.02
1	AT24C256	serial EEPROM	$ 0.740	$ 0.74
8	AAT4610	AAT4610	$ 0.040	$ 0.32
8	LTC4210	LTC4210	$ 3.555	$ 28.44
8	STD95N4F3	STD95N4F3	$ 0.838	$ 6.70
8	ADM4073	ADM4073	$ 0.634	$ 5.07
8	LTC4300A-1	LTC4300A-1	$ 2.000	$ 16.00
8	BC847	BC847	$ 0.023	$ 0.18
8	BC857	BC857	$ 0.078	$ 0.63
64		Parts Subtotal		$ 88.61
		Assembly Cost	$ 0.050	$ 3.20
		TOTAL		**$ 91.81**

Notes:

- PPS Actel Fusion design as analyzed supports Serial-over-LAN (SoL) Pass Through (PT) or Super Pass Through (SPT) modes – SoL Is Not Supported by PPS H8S design.
- PPS Actel Fusion design requires no customer royalty to PPS. Customer Designs using PPS H8S design require a per board royalty to PPS.

37% improvement in BOM total parts count
27% savings, BOM only cost
27% savings, total cost including assembly
38% reduction in board area (4,094mm^2 vs. 2,540mm^2): ~$35 savings per board

Lessons Learned

- BOM consolidation results are real
- Flash FPGAs with security features enable production flexibility
- IP cores reduce development risk
- IPMI firmware development is non-trivial
- Customers will push environmental envelopes

More Lessons Learned

- Some problems can only be solved in circuit design
- Some problems can only be solved in firmware
- Care must be taken to have the correct developers address problems as a team
- Flash FPGA FPGAs allow more flexibility in solving problems that fall in the gray area

Conclusions

- Standards-based Hardware Platform Management requirements drive up design complexity
- Design solutions using discrete parts add to designer challenges
- Mixed Signal Flash FPGA use reduces design complexity, minimizes BOM parts count, reduces board area and congestion, reduces power consumption and thermal loading, and increases noise and SEU immunity
- Use of design examples proven in hardware reduces risk
- Using with existing IP blocks reduces risk
- Mixed Signal Flash FPGA solutions delivers measurable advantages directly to the bottom line

Actel Corporation

- Established fabless FPGA company
  - First product shipped in 1988
  - $196M sales in 2007
  - NASDAQ: ACTL
  - Strong balance sheet: $183M cash and investments, no debt
  - More than 580 employees worldwide
  - #1 nonvolatile FPGA supplier
- Contacts:

Mike Brogley
Product Marketing Manager, System Applications
mike.brogley@actel.com
650-318-4982

Ken O'Neill
Director, High Reliability Product Marketing
keno@actel.com
650-318-4291