Using Fusion Mixed-signal FPGAs to Implement System Management in µTCA Applications

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Agenda

- TCA Hardware Platform Management Challenges
- Traditional Design using Discrete Devices
- Mixed-signal FPGA Advantages
- Design Examples
- Lessons Learned
- Conclusions
- Contact Information
TCA Hardware Platform Management Challenges

- Startup and Power Sequencing
- Power, Current, and Temperature Monitoring
- IPMI Communications
- Interoperability
- Thermal and Power Management
- Redundancy and Reliability
- Manufacturability
Traditional Solutions using Discrete Devices

- **Startup and Power Sequencing**
  - Limited configurability
  - "All sizes fit one"

- **Power, Current and Temperature Monitoring**
  - Limited customization
  - "All sizes fit one"

- **IPMI**
  - Multiple I2C devices
  - Must be managed by external processor
Traditional Solutions using Discrete Devices, continued

- **Interoperability**
  - Designs required to “Play Well With Others”
  - Firmware-centric solutions challenged in spec-driven critical timing requirements

- **Thermal and Power Impact**
  - High BOM counts
  - Power budgets
  - Chassis thermal loading
Traditional Solutions using Discrete Devices, continued

- **Redundancy and Reliability**
  - Every discrete part is a new single point of failure

- **Manufacturability**
  - High BOM count:
    - Increases board layout time
    - Increases required board layers
    - Increases routing complexity (thru-holes, vias)
    - Increases assembly expense
    - Increases BOM kitting challenges
Mixed-Signal FPGA Advantages

- Intrinsically Low Power
- Extensive Security Features
- Live at Power Up
- Reprogrammable
- Intrinsically Great Noise Immunity
- Voltage, Current and Temperature Monitoring
- FET Driver Outputs
- On-chip NVM
- Configurable Clocking Resources
  - Internal RC oscillator, Crystal Oscillator, CCC/PLL and Real Time Counter
- Embedded CPUs
  - CoreABC, 8051 and ARM Cortex-M1 processor
  - 8051
  - Cortex-M1
Fusion: Actel’s Mixed Signal FPGA

- PLL/CCC
- FROM
- Charge Pumps
- Clocking
- Embedded Flash
- SRAM/FIFO
- JTAG ISP
- ISP AES Decryption
- ADC
- Analog I/O
Integration Advantages of Mixed-Signal FPGAs

- BOM Integration
- Board Design Simplification
- Reduced Thermal Loading
- Reduced Points of Failure
- Increased Design Flexibility
- Reprogrammability
- Customizability
Mixed-Signal FPGA Design Approach

- Leverage Existing Pre-built IP and Minimize Full-custom Development
- Maximize Design Flexibility,
  - Taking advantage of FPGA reprogrammability
- Maximize Design Reuse,
  - Particularly for common elements in standards-driven designs
- Partner with Industry Leaders
- Design to Accommodate Real Customer Needs
Mixed-Signal FPGA Results

- **BOM Total Parts Count Reduction**
  - μTCA PM: 53% (from ~800 parts to ~370)
  - ATCA IPMC core: 39%
  - ATCA AMC Carrier w/8 AMC sites: 37%

- **BOM Cost Reduction**
  - μTCA PM: 23%
  - ATCA IPMC core: 11%
  - ATCA AMC Carrier: 27%

- **Board Area Reduction**
  - μTCA: 27%
  - ATCA IPMC core: 38%
  - ATCA AMC Carrier: 38%
Design Example: MicroTCA Power Module

- Integrated Power Management for MicroTCA Chassis
- Fusion FPGA plus 8051 processor
- Enhanced Module Management Controller (EMMC)
  - Continuous monitoring of >60 different analog signals
  - Monitor voltage, current and primary shut-off every 100ms on 32 channels
  - Programmable current limit 40mA increments to 10 amps
  - During payload power failure with standby management power
  - All inputs and outputs continue to be monitored
  - All management functions are fully operational
  - Redundant I2C IP platform
  - Independent channels can be primary or backup with redundant PMs
  - Gate logic implemented failure mode response
Design Example: Advanced Mezzanine Card (MMC)

- **Integrated board monitoring, power management and communications MMC**
- **On-board analog and digital processing**
  - Core8051s processor
  - Dual CoreI2C for IPMI
  - Fusion analog processing block
  - CoreUARTapb and CoreGPIO blocks
  - CorePWM controls variable load payload
- **Load Board Payload**
  - Reference design provides variable load and system monitoring
Design Example: AMC Carrier (Carrier IPMC)

- Management controllers for ATCA AMC Carrier blades
- Fusion FPGA with ARM Cortex-M1 soft processor core
- Digital Logic in Standard IP
  - CoreI2C, CoreUartApb, CoreABC, CoreMBX and CoreAI alongside bus fabric cores
- Analog Offload with Standard IP
  - CoreAI used as the analog engine
    - Raw ADC sampling
  - CoreABC used as the closed loop control of the analog engine
    - Autonomous threshold detection
  - CoreMBX used as the communication medium between the Cortex-M1 and CoreABC processors
    - CoreABC interrupts Cortex-M1 based on certain events via CoreMBX
AMC Carrier Architecture
BOM Comparison: IPMC Core Only

-39% Improvement in BOM total parts count
-10% Savings, BOM only cost
-11% Savings, total cost incl. assembly
-38% reduction in core board area (1,140mm² vs. 708mm²): $4 savings per board
37% improvement in BOM total parts count
27% savings, BOM only cost
27% savings, total cost including assembly
38% reduction in board area (4,094mm² vs. 2,540mm²): ~$35 savings per board
Lessons Learned

- BOM consolidation results are real
- Flash FPGAs with security features enable production flexibility
- IP cores reduce development risk
- IPMI firmware development is non-trivial
- Customers will push environmental envelopes
More Lessons Learned

- Some problems can only be solved in circuit design
- Some problems can only be solved in firmware
- Care must be taken to have the correct developers address problems as a team
- Flash FPGA FPGAs allow more flexibility in solving problems that fall in the gray area
Conclusions

- Standards-based Hardware Platform Management requirements drive up design complexity
- Design solutions using discrete parts add to designer challenges
- Mixed Signal Flash FPGA use reduces design complexity, minimizes BOM parts count, reduces board area and congestion, reduces power consumption and thermal loading, and increases noise and SEU immunity
- Use of design examples proven in hardware reduces risk
- Using with existing IP blocks reduces risk
- Mixed Signal Flash FPGA solutions delivers measurable advantages directly to the bottom line
Actel Corporation

- **Established fabless FPGA company**
  - First product shipped in 1988
  - $196M sales in 2007
  - NASDAQ: ACTL
  - Strong balance sheet: $183M cash and investments, no debt
  - More than 580 employees worldwide
  - #1 nonvolatile FPGA supplier

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