Reconfigurable Computing Task

RHESE Reconfigurable Computing (RC) Task Lead:
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Goals and Objectives

Reconfigurable Computing Task

Central Goal of RHESE RC:

"Development and Delivery of Reconfigurable Computing Resources for Space Infrastructure"

Resulting in:

- **Hardware and functional interchangeability among CxP elements**
- **Increased cross-use and reuse of computing resources for multiple purposes**
- **Reduced flight spares and increased payload capacity**
- **Ability to change function and performance of a particular computing resource in part or entirely: manually or automatically**
- **Increased efficiency: lower long-term development cost, faster implementation, decreased power consumption**
- **Faster servicing, better mission assurance, and increased safety**

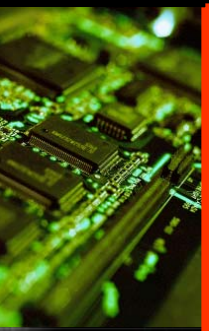
Development Approach

Reconfigurable Computing Task

- **Development Focuses on Three Interrelated Areas:**
  - **Internal Modularity**
  - **External Modularity**
  - **Fault Management**

Internal Modularity

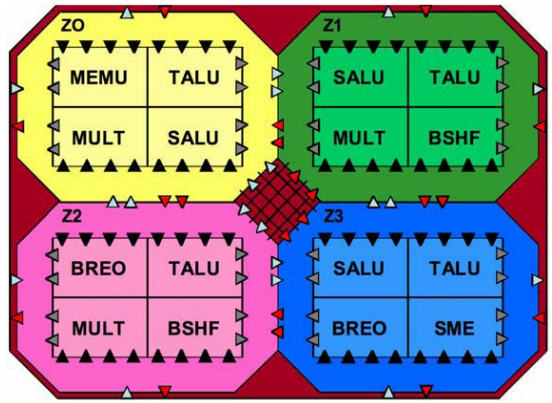
Reconfigurable Computing Task



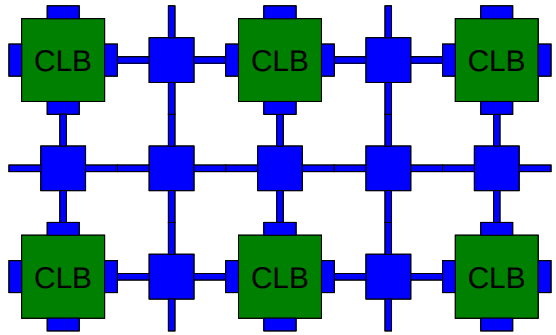
Internal Modularity

Reconfigurable Computing Task

- **ElementCXI ECA-64 “Field-Programmable Node Array” (FPNA)**
- **Field-Programmable Gate Arrays (FPGA)**
  - SIRF: Rad-Hard Virtex-5 FPGA
- **Other viable RC-capable options**
  - Not restricted to one technology or even one chip
  - Digital, Hybrid, or Analog (FPAA: “Analog Arrays”)
  - CPU technology may be utilized
  - New technologies as available
- **Coarse vs. Fine Granularity**
  - Gate-level RC allows complete versatility, but costs in development complexity
  - Medium to Coarse level adds abstraction, but costs in lowered flexibility
  - Compromise, at least for now, should allow earlier development payoffs. E.g.: reconfiguration speed, HOS, fault handling



ECA Structure

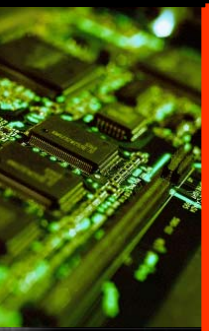


Credits: Clive Maxfield, “The Design Warrior's Guide to FPGAs”

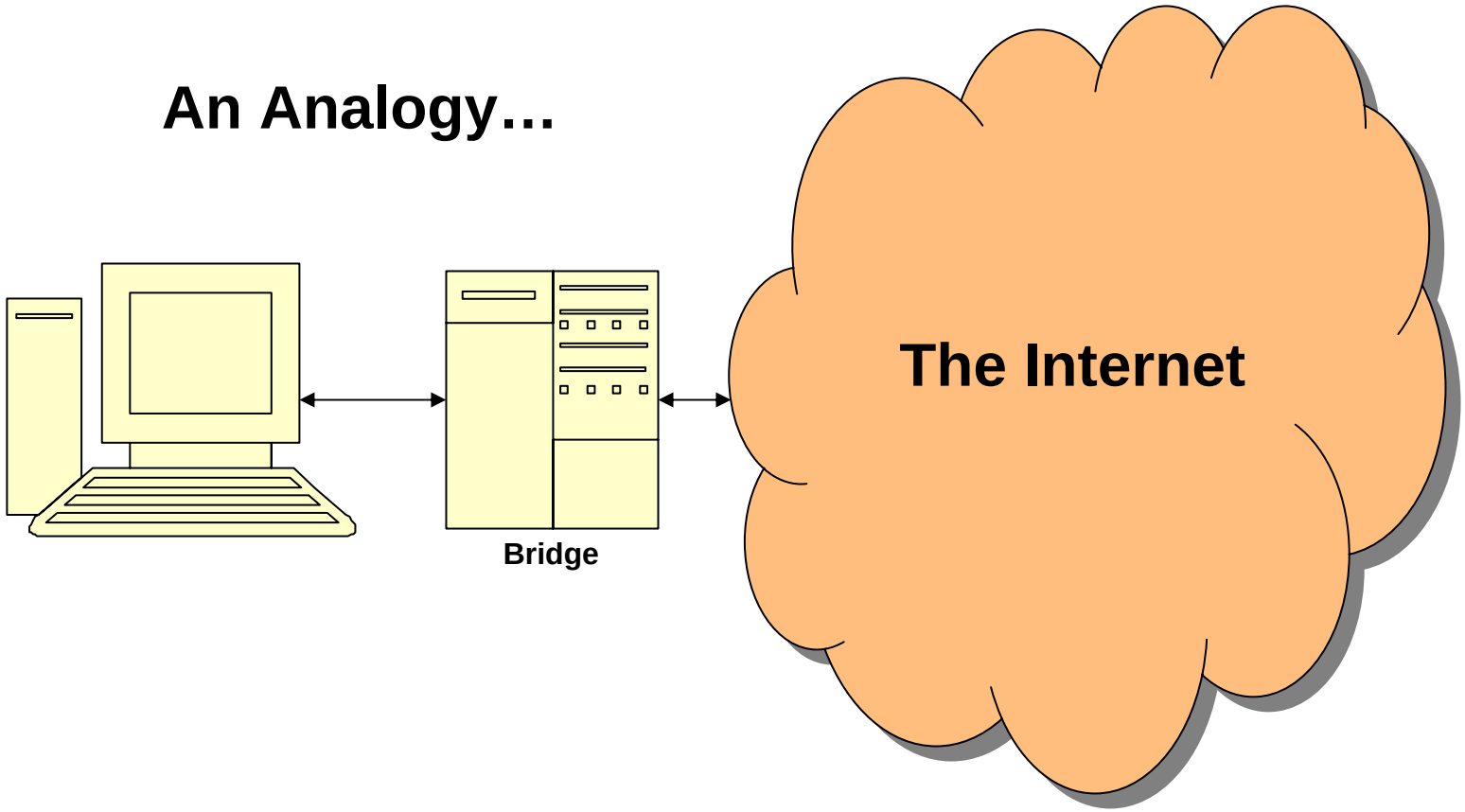
FPGA Structure

External Modularity

Reconfigurable Computing Task

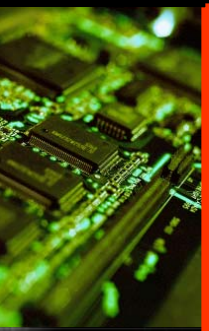


An Analogy…

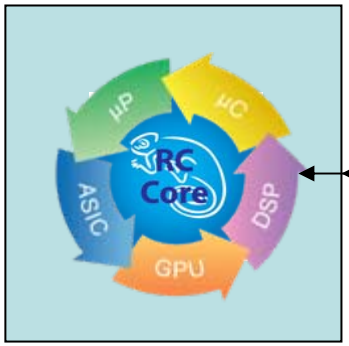


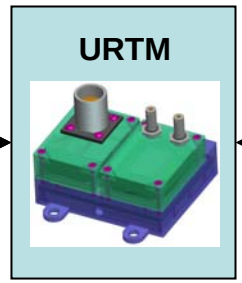
External Modularity

Reconfigurable Computing Task




…Becomes…





Universal Reconfigurable Translator Module

Sensors, Peripherals, Other RC,

The “Outside World”

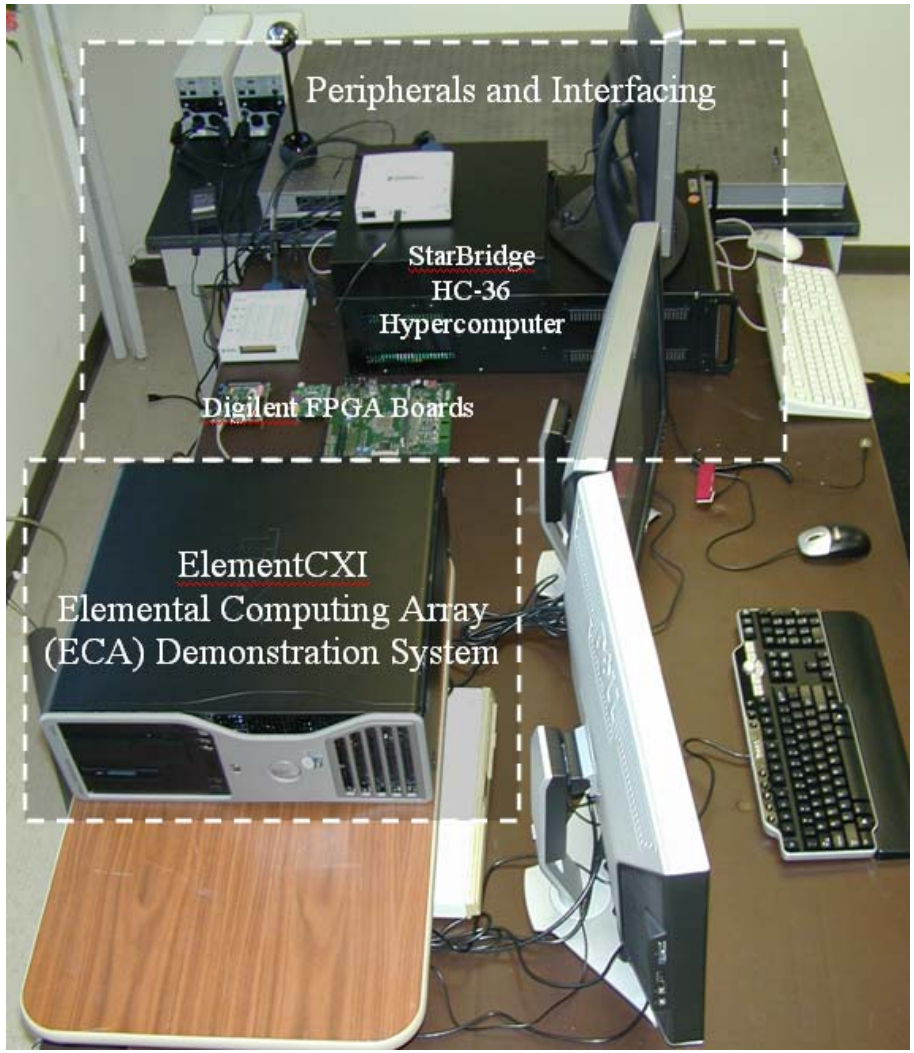
External Modularity

Reconfigurable Computing Task

- **Multi-Channel, Reconfigurable Interface Control**
  - **Plug and Play**
  - **Enables Interchangeability and Scalability**
  - **Dynamic Channel and Bandwidth Management**
  - **Fault Detection and Healing**
- **URTM**
  - **LaRC and Sigma Space**
  - **Currently, reconfigurable in bus standard implementations only**
  - **Three, or possibly four, bus standards:**
    - **SpaceWire**
    - **1553**
    - **1194b (“Firewire”)**
    - **Gigabit Ethernet – option studied**

Demonstration #1

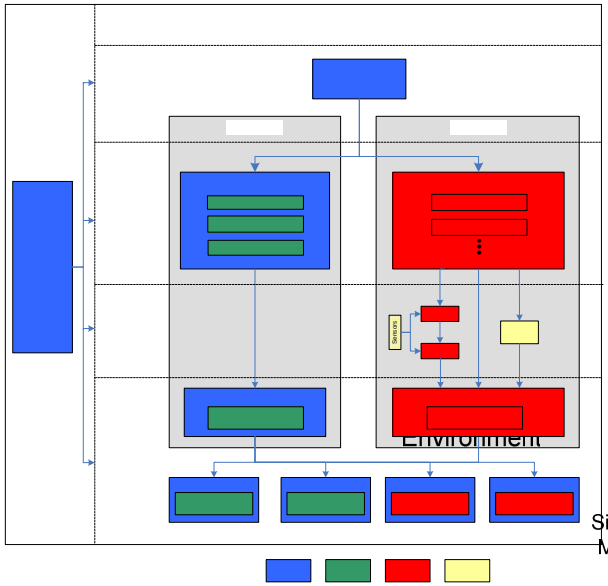
Reconfigurable Computing Task

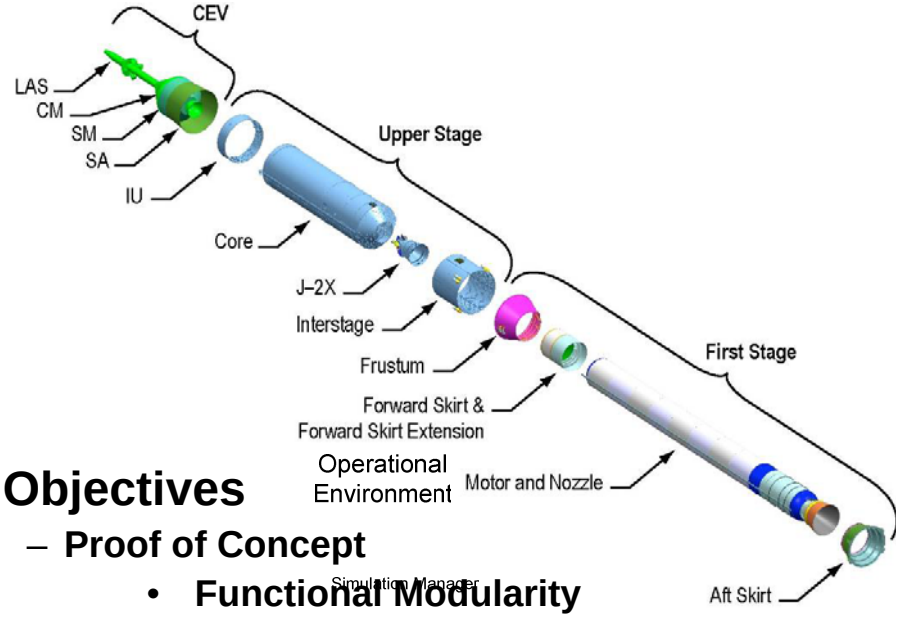


- **Objectives**
  - **Proof of Concept: Basic Reconfigurability**
  - **Demonstrate multiple discreet configurations separately**
- **Configurations**
  - **µP: Turing Machine**
  - **DSP: Video FFT**
  - **µC: Motor Control and Feedback**
- **MSFC, September 16, 2008**

Demonstration #2

Reconfigurable Computing Task





- **Objectives**
  - **Proof of Concept**
    - **Functional Modularity**
    - **Physical Modularity**
    - **Automated Reconfiguration**
  - **Demonstrate cooperative integrated application of tasks**
- **Proposed Configurations**
  - **Video input**
  - **Command processing**
  - **Remote robot control and feedback**
  - **Integration with FDDR Ares I Lander Simulator**
- **MSFC, Mid-Year 2009**

Fault Handling

Reconfigurable Computing Task




Triple-Mode Redundancy (TMR) and Time-Domain Redundancy

- **Detection**
- **Mitigation**
- **Healing**
  - **Circuit Paging**
  - **RC-as-Hard-Disk**
  - **Circuit Isolation**

- **Fault Handling is already being explored as time allows, but not scheduled to be addressed until later**

Motivation: Addressing Customer Needs

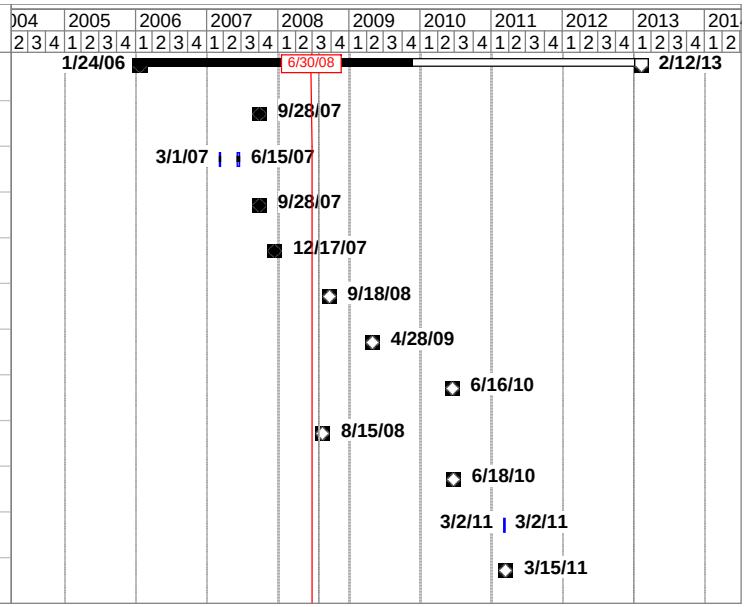
Reconfigurable Computing Task

- **Flight-Qualified, Multi-String Redundant Hardware is Expensive**
  - **Development, Integration, IV&V, and Flight Qualification**
  - **Space and Weight**
  - **Power Consumption**
  - **Dissimilar Spares**
- **Design of Computing Resources "From Scratch" for Every New Flight System is Unnecessary and Wasteful**
- **Current Options for Harsh/Flight Environment Systems are Limited**
  - **Custom Hardware, Firmware, and Software**
  - **Dedicated and Inflexible**
  - **Often Proprietary**
- **Increased Requirements for Flexibility**
  - **Reconfigurable and Modular Capabilities will address these**
  - **Capacity to use one system to back up any number of others**
  - **General Reusability of hardware = more payload capacity**
  - **Interchangeability = reduction of development time and expense**

Schedule and Milestones

Reconfigurable Computing Task

ID	WBS	Task Name	NASA Site	% Compl
256	**1.2.5**	**Reconfigurable Computing**	**MSFC**	**54%**
263	1.2.5.7	Complete Procurement of Testbed HW & SW - Phase 1	MSFC	100%
269	1.2.5.13.1	Develop Initial Testbed Interface	MSFC	100%
271	1.2.5.13.3	Complete Testbed Interface Refinement	MSFC	100%
276	1.2.5.16.2	Elemental Computing Array (ECA) Delivery	MSFC	100%
285	1.2.5.16.11	Demonstration #1 of Basic Reconfigurability	MSFC	0%
291	1.2.5.18	Demonstration # 2 of Reconfigurable Spares	MSFC	0%
296	1.2.5.23	Demonstrate RC Automated/ Autonomous Fault Response & Recovery	MSFC	0%
304	1.2.5.25.6	IP Cores Delivery & Demo	MSFC	0%
308	1.2.5.27	Demonstrate Platform/ Vehicle Sys Modularity	MSFC	0%
312	1.2.5.31	RC Infusion Plan Completed	MSFC	0%
314	1.2.5.32a	Demo Platform-Indep Automated / Autonomous Adaptive Env-Hard Avionics Suite Complete	MSFC	0%



Key Performance Parameters

Reconfigurable Computing Task

Objective	Constellation Milestone Supported	Key Performance Parameters	Units	State of the Art (SOA)	Performance Target (Full Sucess)	Performance Target (Min Sucess)	Validation Method
Improve Reconfiguration Speed	LPRP, CEV Block 2	Speed of Dynamic Reconfiguration	sec	5	1.00E-03	1	Test
Develop Reconfigurable Robust Electronics	LPRP, CEV Block 3	Redundancy and Reconfigurability	Levels of Reconfigurability	None	4	3	Test

Accomplishments

Reconfigurable Computing Task




RC Accomplishments include:

- Substantial groundwork and planning has been completed
- Main body of test bed acquisition and installation is complete
- Elemental Computing Array ECA-64 demo system has been acquired and assembled. Integration and development are ongoing.
- Implementation of large portion of first demo will be a Turing Machine.
- Initial work on Fast Fourier Transform (FFT) implementation
- Peripheral interfacing with ECA-64 progressing
- Student interns utilized as available for exploratory development of advanced demo materials: robotics, vision systems, etc.
- Universal Reconfigurable Translator Module (URTM), being developed by Sigma Space under contract to LaRC, is close to delivery. Acceptance review is planned for August 28, 2008.

FY09 Planned Activities

Reconfigurable Computing Task

FY09 Planned Activities include:

- **Report on first test bed demonstration**
- **Second demonstration and report(s)**
- **Begin efforts in basic fault detection, mitigation and healing**
- **Initial development of advanced external modularity**
- **Initial advanced test bed procurement and installation**
- **Forward planning for next phases**
- **Further advanced concepts development ahead of schedule where possible**

Deliverables

Reconfigurable Computing Task




FY09 Deliverables

- Demo #1 Report
- Demo #2 and Report
- Forward Planning and Engineering
- Initial Results of Advanced Development

FY10+ Deliverables

- Flight-Qualified, Radiation-Hardened Universal Modular RC
- TRL-6 Infusion at end of FY10 (aggressive)