A Multi-Mode Reconfigurable OFDM Communication System on FPGA

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System Objectives

— Switching between different communication modes
— Modular design to accommodate different implementation techniques, such as mode switching or dynamic reconfiguration, error rate measurement, etc.
— Adapt to measured environmental conditions, such as link quality, and efficient use of bandwidth during protocol operation

System Overview

— Server and client nodes
— Normal and mode switching states
— Manual or automatic trigger, or both
— Modular designs for channel measurement trigger, transmission error rate measurement, mode switching and recovery, etc

Hardware Platform and Experimental Setup

Hardware Platform
— Xilinx Virtex II VP70
— WARP toolkit, including FPGA, radio and clock boards

Experimental Setup
— Two PCs connecting with the boards through Ethernet ports
— FPGA nodes acting as a wireless bridge transparent to both PCs
— Application software running on PCs to conduct measurement

System Design

Packet Format and Types

Field Value | Packet Type
-------------|-----------
0 | Data
1 | Ack
2 | Start
3 | Ack_Start
4 | Measurement
5 | End
6 | Result_End
7 | Synch
8 | Ack_Synch
9 | Rollback
10 | Ack_Rollback

Handshake Protocol

Phase I
— Triggered by an expired timer
— Server sends “start” packets
— Client acknowledges the server

Phase II
— Either software method or hardware-assisted BER measurement
— Software method sending a certain number of short measurement frames
— Selection of method agreed upon beforehand between the server and its client

Phase III
— “Quiescence” scheme to prevent miscommunication
— Server changes mode and then keeps silent
— Client detects the silence by a timer
— Mode switching technique
  — changing parameters into a modular design
  — utilizing Dynamic Partial Reconfiguration (DPR) available on the state of the art Xilinx FPGAs

Implementation and Results

Implementation
— C programming on PowerPC for all the MAC layer protocol
— Mode switching between SISO-OFDM with different modulation schemes, such as QPSK and QAM16
— Hardware implementation based on the WARP framework
— Double timer setup to enhance data transfer reliability during the time of poor link quality
— Xilinx EDK tool chain

Results
— 1 PowerPC
— 70% of FPGA slices and 80% of BRAM
— Measured bandwidth at about 2 to 7 Mbps
— Time for the whole mode switching process varying between 0.5~0.6 seconds
— Transmission error rate measurement used 2000 short packets

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