SET Characterization and Mitigation in RTAX-S Antifuse FPGAs

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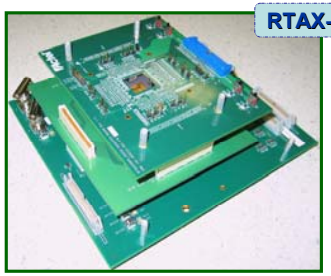
Objectives

- RTAX-S SET Characterization of Global Signals
- RTAX-S SET Characterization & Mitigation (C-Cells)
- RTAX-S SEU Characterization & Mitigation (R-Cells)

Heavy Ion Radiation Tests

- Devices Under Test: 0.15µm RTAX250S-CQ352 and RTAX2000S-CQ352
- Facility: Lawrence Berkeley National Laboratories (LBNL) - Heavy Ions
- Fluences > 10^7 cm^{-2} per run
- Test Frequencies: 6, 30, 60, 80 and 120 MHz
- Test Dates: May, June & August 2008

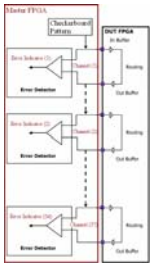
RTAX-S EXPERIMENTAL TEST SETUP



Devices Under Test

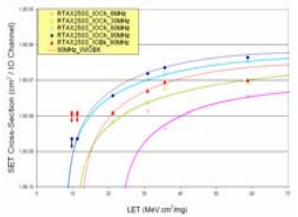
PART	RTAX250S	RTAX2000S
C-Cells	2816	21,504
R-Cells	1408	10,752
RAM (Kbits)	54	288
Global Signals	8 (4HCLK, 4RCLK)	8 (4HCLK, 4RCLK)
IO Banks	8	8
User IOs	198	684

Input/Output Structures

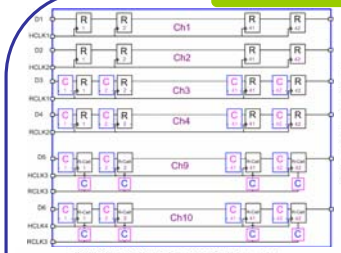


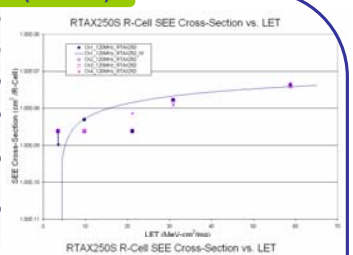
Test Design

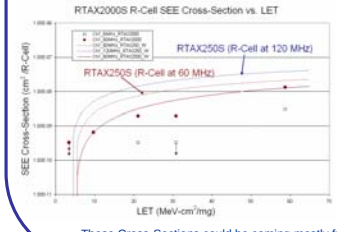
- DUT: RTAXS250-CQ352
- 44 LVDS IO Channels

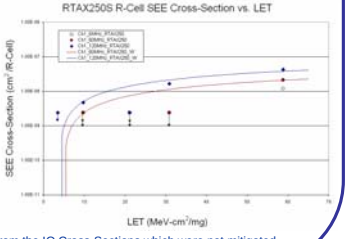


FPGA Core (R-Cells)

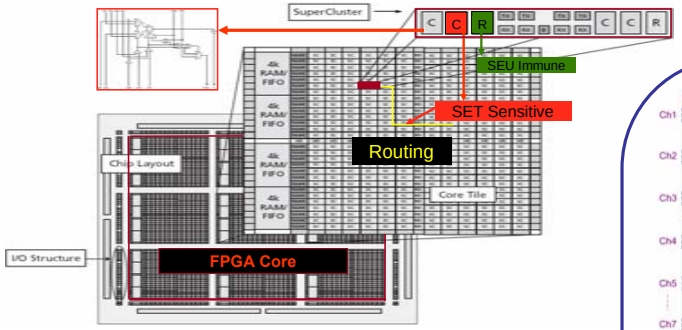




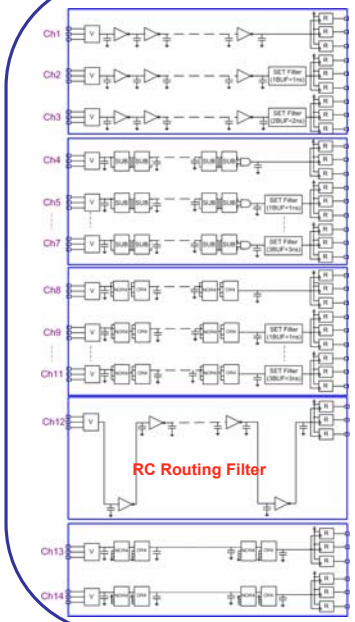


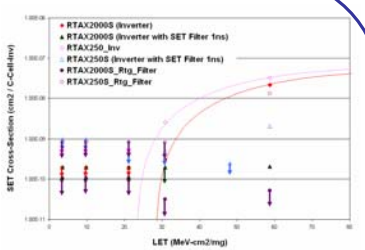


These Cross-Sections could be coming mostly from the IO Cross-Sections which were not mitigated, since the R-Cells are mitigated to SEU

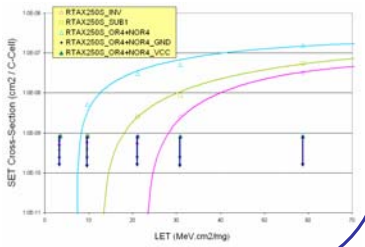


FPGA Core (C-Cells)

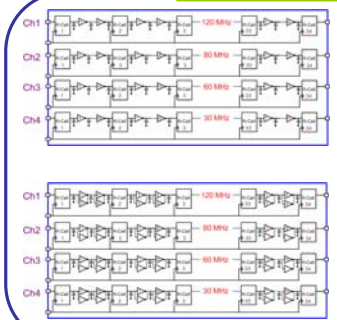


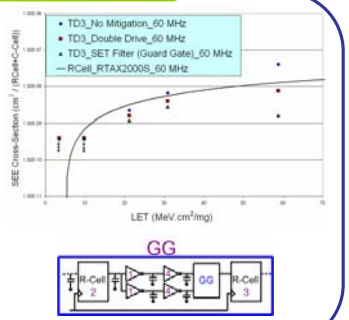


FPGA	# Inverters / Channel
RTAX250S	120
RTAX2000S	950

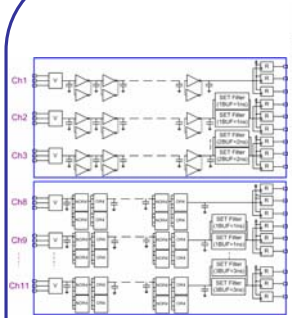


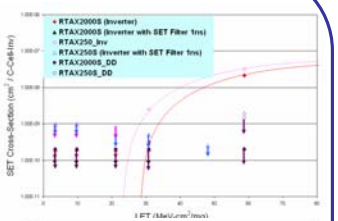
Test Design (R-Cells + C-Cells)

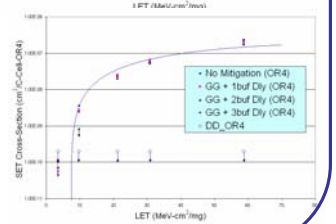




SET Mitigation







Summary

This poster targets primarily a comprehensive SET characterization and mitigation of the RTAX-S FPGA family (RTAX250S-CQ352 and RTAX2000S-CQ352), mainly the FPGA core and the IO blocks when configured with two IO standards (LVDS 2.5 and LVCMOS 2.5). Furthermore, by using test techniques previously employed for the SET characterization of the ACTEL Flash-FPGA family [1], C-Cell SET cross-sections and the maximum resulting SET pulse widths in the FPGA are measured. Also, designs from novel SET mitigation techniques, based on SET filtering mechanism at the input of a TMR'd sequential cell are validated in heavy-ion beams at Lawrence Berkeley National Laboratories (LBNL). These are derived from some of the previously presented techniques in [1], in particular the techniques using the guard-gate cells (with temporal delay or duplication of the logic C-Cells) and for the first time on new re-routing mitigation solutions (to filter the SET), with no additional hardware overhead but a simple time penalty (less than the maximum SET pulse width).

SET mitigation in the Combinatorial-Cells (C-Cells) of the RTAX-S family might not be needed (depending on the criticality of the application). Indeed, SET have very little effects on C-Cells and only starting from an LET > 20 MeV-cm²/mg. This is due to the small geometry (0.15-µm) and its unique architecture (non-volatile and a naturally filtering architecture, reducing the SET pulse widths at each C-Cell).

REFERENCES

[1] S. Rezgui, J.J. Wang, E. Chan Tung, J. McCollum and B. Cronquist, "New Methodologies for SET Characterization and Mitigation in Flash-Based FPGAs", *IEEE TNS, Vol. 54, NO. 6*, Dec. 2007, pp 2512-2524.
[2] M. Berg, J. J. Wang, R. Ladbury, S. Buchner, H. Kim, J. Howard, K. Label, A. Phan, T. Irwin, and M. Friendlich, "An Analysis of Single Event Upset Dependencies on High Frequency and Architectural Implementations within Actel RTAX-S Family Field Programmable Gate Arrays", *IEEE TNS, Vol. 53, NO. 6*, Dec. 2006, pp 3569-3574.
[3] RTAX-S Antifuse Family FPGAs Datasheet: Available: http://www.actel.com/documents/RTAXSDetailedSpecs_DS.pdf
[4] J.J. Wang, "RTAX EDAC-RAM Single Event Upset Test Report", Available: http://www.actel.com/documents/RTAX-S%20SEE%20EDAC%20RAM.pdf