“Functional and Performance validation of the 80S32 μC for Space Applications”

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Abstract

This project is performed in the frame of an ESA contract undertaken by ISD and involves the validation of an 8bit µC (80S32) for use in Space Applications.

The µC is an 8032 variant enhanced with extended timers, 4 USART interfaces, a CRC unit compliant with CCSDS TM/TC, additional external interrupt inputs, de-multiplexed address/data bus and an extended addressing range supporting up to 8MB Code and 16MB Data.

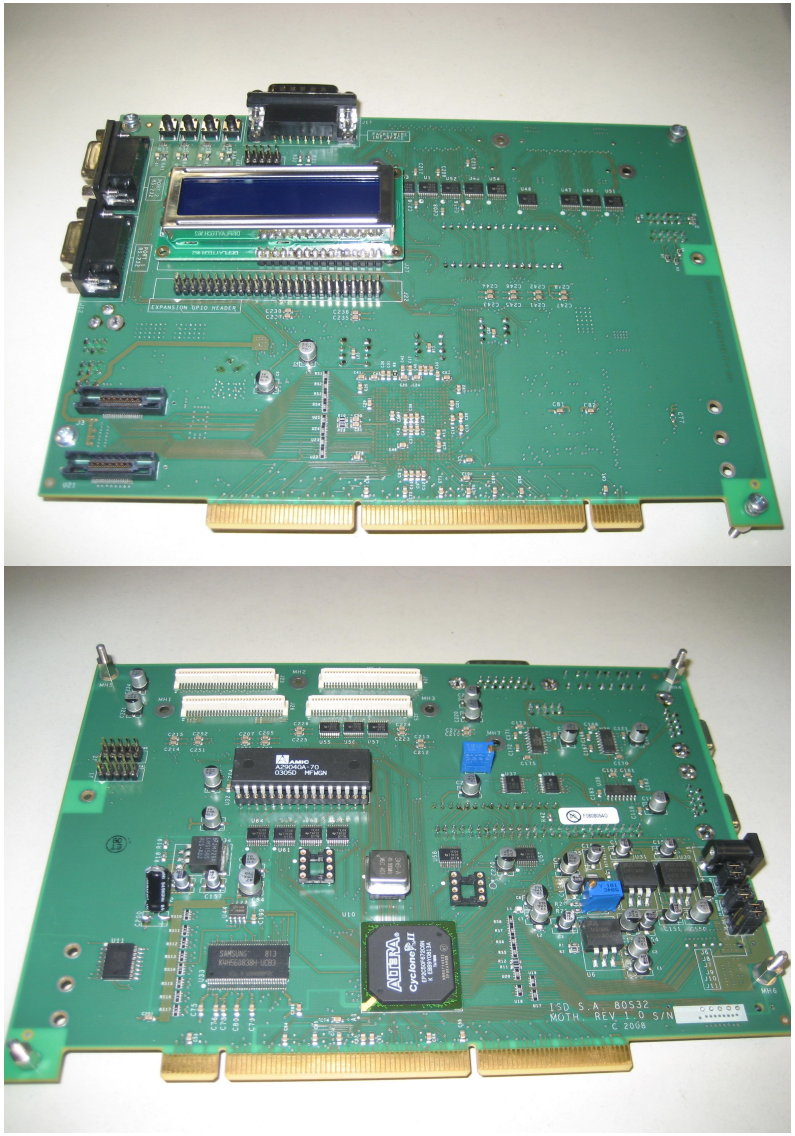
The 80S32 [1], [2] is fabricated in Atmel 0.5 um radiation tolerant gate array technology MG2RT [3]. Single Event Upset (SEU) protection is ensured by using hardened flip-flops for critical registers and an Error Detection And Correction (EDAC) scheme for on-chip and external memory.

A test system has been developed, interfacing the 80S32 to an FPGA emulating components commonly interacting with the µC in space applications. The test system is composed of a motherboard providing FPGA, memory, power, clock and I/O devices, as well as a DUT board hosting the 80S32 and possibly other extension boards with additional interfaces.

Validation testing includes SEU testing at ESA's CASE (Californium-232) system [4]. After successful validation, a commercialisation of the 80S32 and its test and evaluation board is planned.

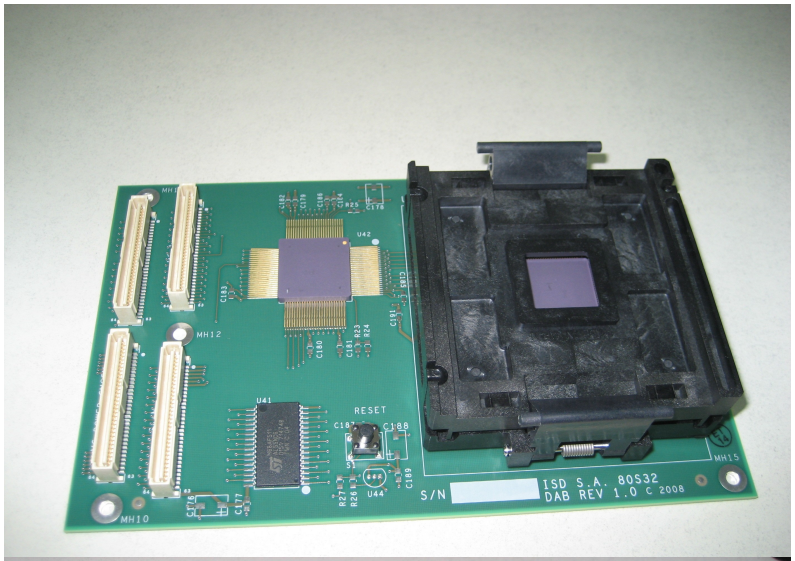
Motherboard

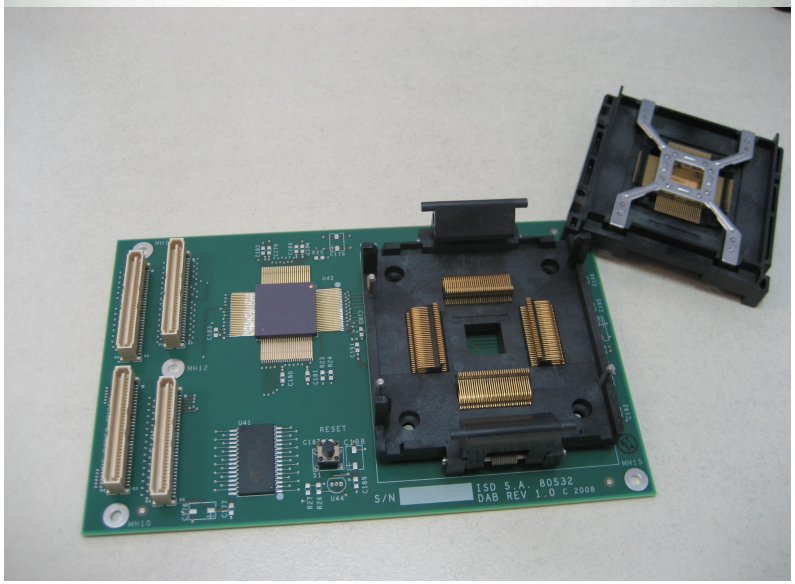
- Altera EP2C50 FPGA
  - Used as DUT functionality monitor
- 32 MB DDR Memory
- Flash Memory
- External interfaces
  - 5 x RS-232 ports
  - 4 x Packet wire ports
  - 2 x 16 LCD Display
  - PCI-X connector
  - JTAG/Debug headers
  - General Purpose extension connector
- Clock generator
- Power regulators



DUT board

- The DUT board is populated with
  - 80S32 µC
  - SRAM
  - Connectors linking it with the Motherboard
- The DUT board allows irradiation of the 80S32 and/or the SRAM chip for validation of the SEU protection



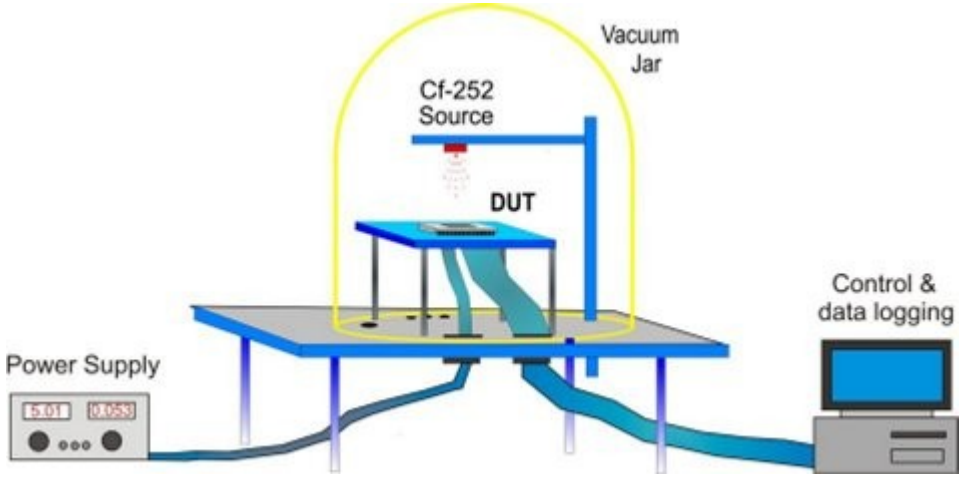


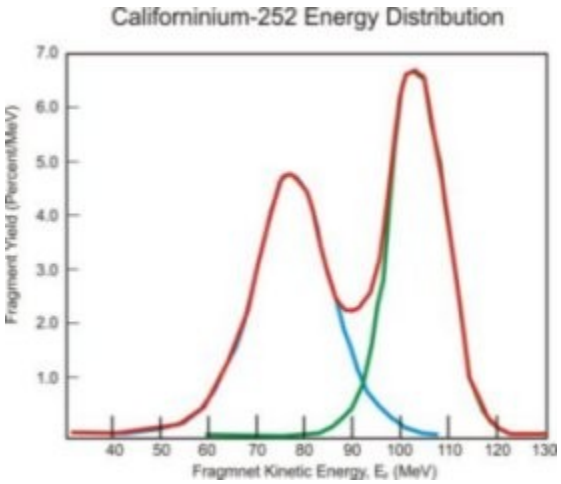
Analog Card

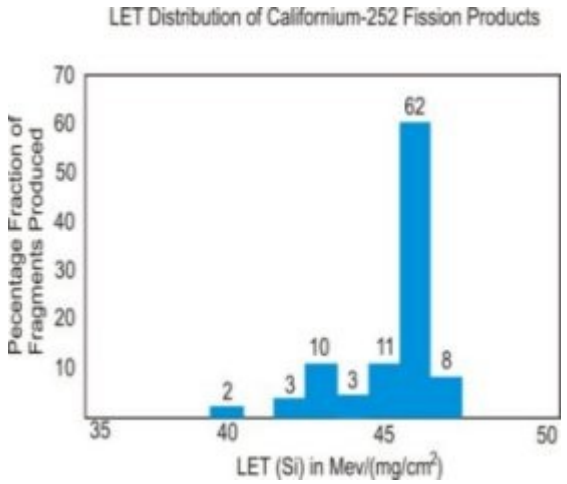
- An analog board is being developed that interfaces external analog signals with the rest of the digital System. This board is to be joined with the Motherboard using an extension connector. It is populated with:
  - 1 x 4 Channel 8bit Analog to Digital Converter with a maximum sampling rate of 2 MSMPS and sampling clock of up to 10 MHz
  - 1 x 8bit Digital to Analog Converter

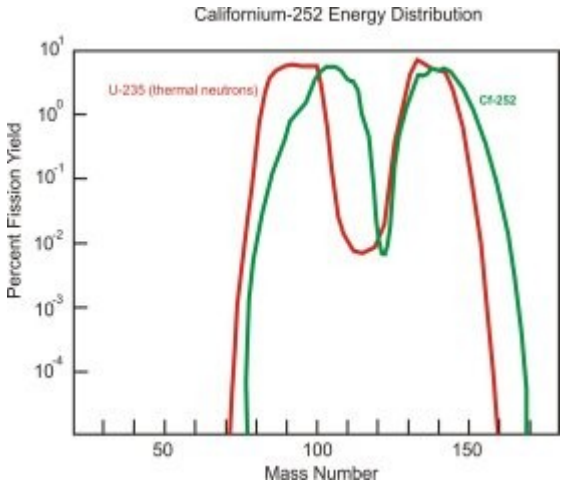
Radiation Testing

ESA's CASE System (**C**alifornium-232 **A**ssessment of **S**ingle event **E**ffects) [4]

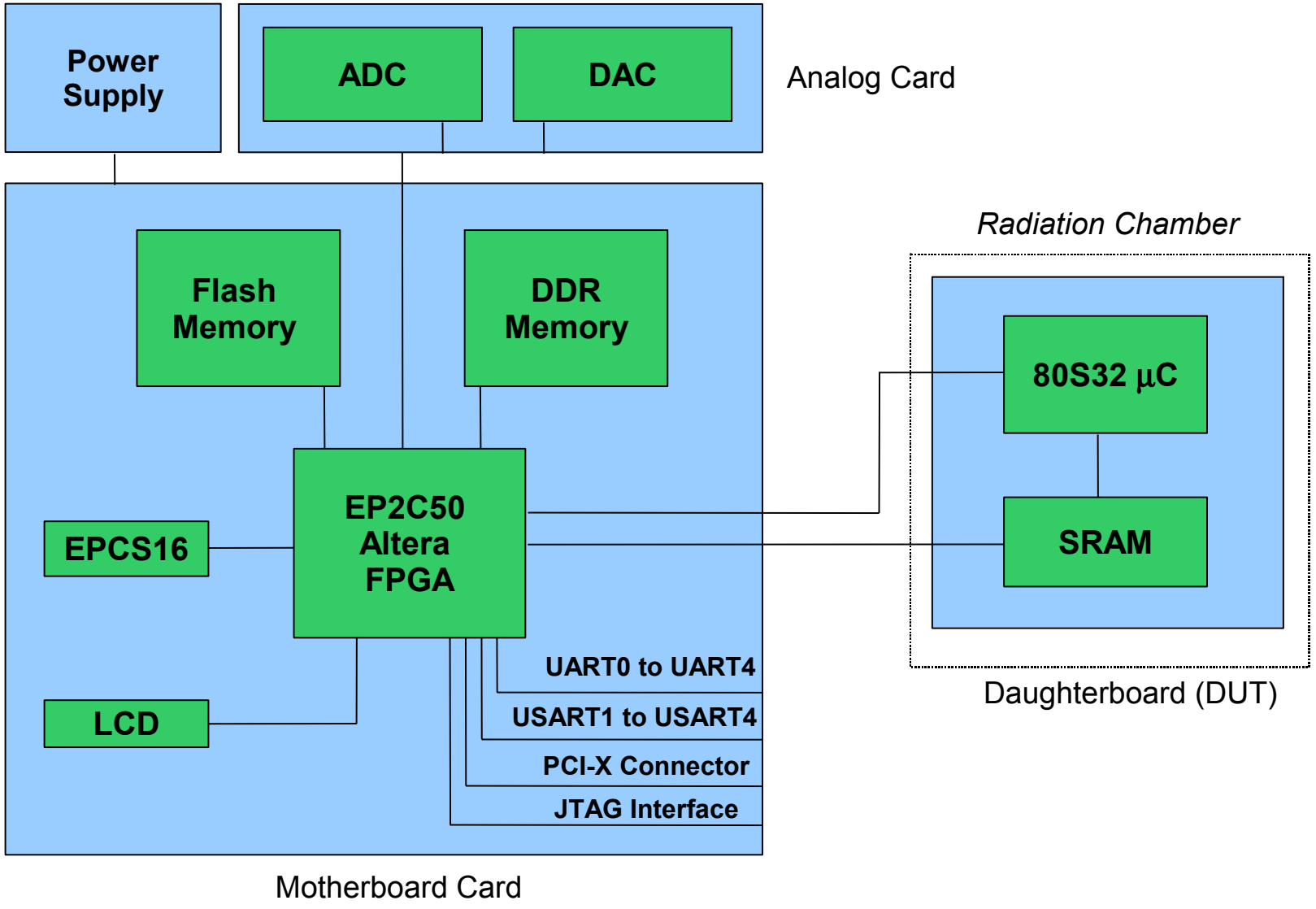








Test Setup


Power Supply
ADC
DAC
Analog Card
Flash Memory
DDR Memory
EP2C50 Altera FPGA
EPCS16
LCD
UART0 to UART4
USART1 to USART4
PCI-X Connector
JTAG Interface
Motherboard Card
Radiation Chamber
80S32 µC
SRAM
Daughterboard (DUT)

Functional Evaluation

- Validating Memory of the 80S32
  - Test to be performed to memory include: lower 128 bytes, upper 128 bytes, SFR region and XRAM without EDAC. Internal memory with EDAC. External memory with/without EDAC enabled.
- Validating Timer functionality of the 80S32
  - Test Modes for the internal timers are: 13bit, 16bit, 8bit and 2x8bit. Timer being configured as counter with IFD, Auto -Reload clock triggering, external triggering, and in Capture Mode.
- Validating UART Ports of the 80S32
  - UART Tests include: Shift Register Mode, 8bit Variable Bd, 9bit Fixed Bd, 9bit Variable Bd Mode, RS232 mode with FIFO support, RS232 mode without FIFO support, PacketWire (PW) mode, TTC-B-01 mode transmit master and transmit slave Modes.
- Validating Interrupt Service of the 80S32
- Validating CRC Generation Block of the 80S32
- Validating the command set of the 80S32

Performance Tests

- The performance tests will cover the following items
  - 8-bit and 16-bit arithmetic
  - Matrix Multiplication
  - LU decomposition
  - Matrix determinant
  - Block Data Manipulation
  - Sorting searching algorithms
  - Conditional Branching
  - Context Switching
  - Table Lookup & Interpolation
  - Digital Signal Processing such as Finite Impulse Response (FIR) Filter, Fast Fourier Transform (FFT), Inverse Fast Fourier Transform (iFFT)
  - Benchmarking such as the Dhrystone benchmark
  - ESA IP PTME (Packet Telemetry Encoder)
- SEU specific test sets within the chamber will also be run on the 80S32

References

- A Microcontroller with Built-In Support for CCSDS Telecommand and Telemetry, Marc Pollina, Peter Sinander, Sandi Habinc
  ftp://ftp.estec.esa.nl/pub/vhdl/doc/Micro8052.pdf
- The 80S32 Data Sheet
  ftp://ftp.estec.esa.nl/pub/vhdl/doc/ADV80S32_DataSheet_2.5.pdf
- http://www.atmel.com/dyn/products/product_card.asp?part_id=2315
- The CASE System at ESA
  (Californium Assessment for Single event Effects)
  https://escies.org/ReadArticle?docId=252