A New Radiation Tolerant Field Programmable Gate Array Based on Non-Volatile Flash Configuration Switches

Eric Chan Tung, J.J. Wang, Sana Rezgui, Yiming Sun, Brian Cronquist, and John McCollum
Actel Corporation, Mountain View, CA 94043, USA

ABSTRACT

A New Radiation-Tolerant ProASIC3 is announced for aerospace applications. This device retains all the features from the A3P FPGA family including enhanced I/Os and lower power consumption. This paper presents Radiation Test Results for Single Event Effects (SEE) and Total Ionizing Dose (TID) tests performed on the A3P FPGA family.

INTRODUCTION

- Flash-based FPGA is both reprogrammable and non-volatile
- Flash technology provides a low-power and single chip solution
- SEE testing was performed at Lawrence Berkeley National Laboratories (LBNL) and Texas A&M University (TAMU). TID testing was performed at the Defense of Microelectronic Activity (DMEA) facility in Sacramento, CA
- Objectives: To characterize and harden the existing ProASIC3 product against radiation for aerospace applications
- Purposes: Announcement of a New Radiation-Tolerant Non-Volatile Reprogrammable FPGA

Radiation Test Results

- ProASIC3 goes RT! ProASIC3 is now RADIATION- TOLERANT, while featuring enhanced I/Os, greater density, and very low power consumption

REFERENCES


CONCLUSIONS

- Except for the embedded FROM, which is very radiation hard, all the other programmable architectures are sensitive to SEE
- SEE and SET hardening are achieved by the implementation of soft macros. There are no Single Event Functional Interrupts (SEFI) or Latch-ups (SEL)
- For a complete SEE immunity at high frequencies (50 MHz and above), triplication of I/Os is mandatory in addition to their separation on 3 different IO banks.
- FPGA Core TID tolerance is harden to 100krad(Si) by a refresh scheme and the margining/programming circuit can withstand up to 40krad(SiO)
- As expected for a non-volatile FPGA, no observed error-event required a reconfiguration of the Flash-based FPGA nor were there any destructive SEE events.

FEATURES

- Low Power Use Single-Chip Nonvolatile Secure On-Chip NVM Firm Error Immune
- Reprogrammable No NRE 1IP Easy Prototyping Fast Time to Market