A New Radiation Tolerant Field Programmable Gate Array Based on Non-Volatile Flash Configuration Switches

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ABSTRACT

A New Radiation-Tolerant ProASIC3 is announced for aerospace applications. This device retains all the features from the A3P FPGA family including enhanced I/Os and lower power consumption. This poster presents Radiation Test Results for Single Event Effects (SEE) and Total Ionizing Dose (TID) tests performed on the A3P FPGA family.

INTRODUCTION

- Flash-based FPGA is both reprogrammable and non-volatile
- Flash technology provides a low-power and single chip solution
- SEE testing was performed at Lawrence Berkeley National Laboratories (LBNL) and Texas A&M University (TAMU). TID testing was performed at the Defense of Microelectronic Activity (DMEA) facility in Sacramento, CA
- Objectives: To characterize and harden the existing ProASIC3 product against radiation for aerospace applications
- Purpose: announcement of a New Radiation-Tolerant Non-Volatile Reprogrammable FPGA

RT ProASIC3

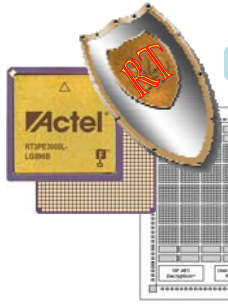


Fig. 1: ProASIC3 Flash FPGA Block Diagram Architecture

FPGA SWITCHES

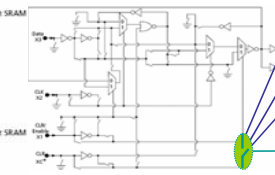
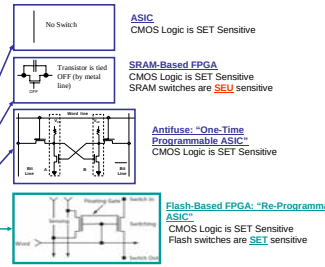


Fig. 2: ProASIC3L Logic Tile Internal Architecture



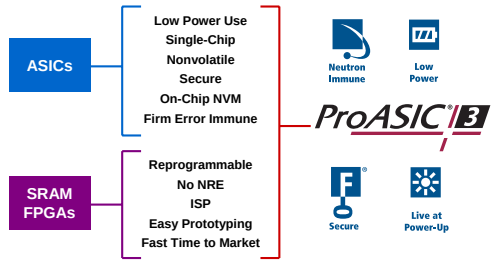
ASIC
CMOS Logic is SET Sensitive

SRAM-Based FPGA
CMOS Logic is SET Sensitive
SRAM switches are SEU sensitive

Antifuse: "One-Time Programmable ASIC"
CMOS Logic is SET Sensitive

Flash-Based FPGA: "Re-Programmable ASIC"
CMOS Logic is SET Sensitive
Flash switches are SET sensitive

FEATURES



ProASIC3 goes **RT**! *ProASIC3* is now **RADIATION-TOLERANT**, while featuring enhanced I/Os, greater density, and very low power consumption

RADIATION TEST RESULTS

FPGA Core (Flip-Flops)

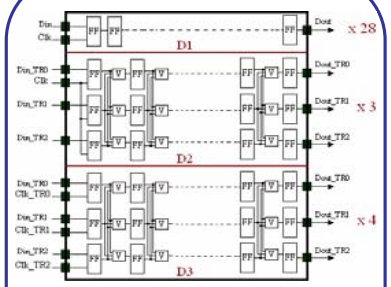


Fig. 3: Block Diagram of the DFF Test Design

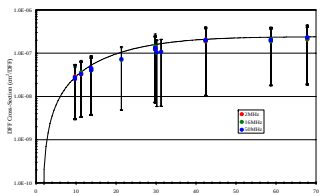


Fig. 4: DFF SEU Cross-Sections

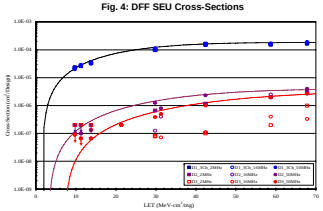


Fig. 5: D1, D2 and D3 SEE Cross-Sections

FPGA Core (Combinational)

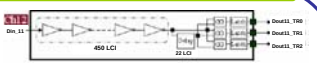


Fig. 6: Mitigated Test Design with Various LCI Delays

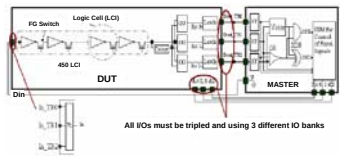


Fig. 7: Mitigated Test Designs and IO Bank SET Mitigation

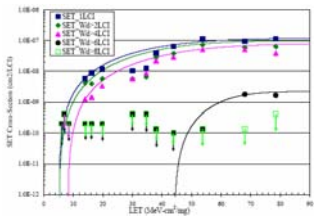


Fig. 8: SET Cross-Sections for Test Designs with different LCI Delays

Clock Network

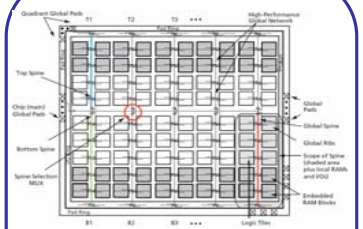


Fig. 9: A3P Clock Network

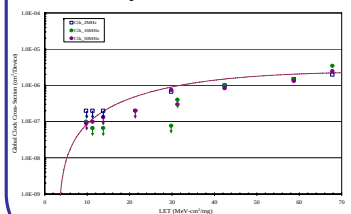


Fig. 10: Global Clock SET Cross-Section

PLL

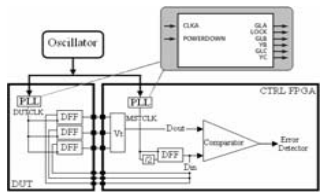


Fig. 11: Block Diagram of the PLL Test Design

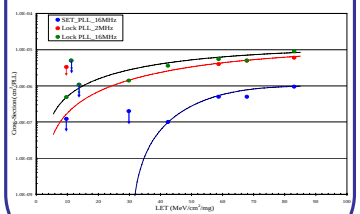


Fig. 12: PLL SET Cross-Sections

SRAM

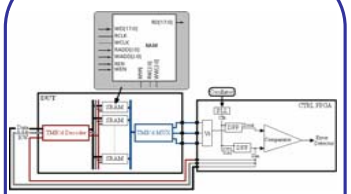


Fig. 13: Block Diagram of the SRAM Test Design

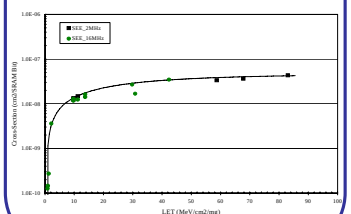


Fig. 14: SRAM SEU Cross-Sections

Flash-ROM (FROM)

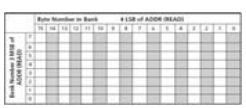


Fig. 15: FROM Block Diagram

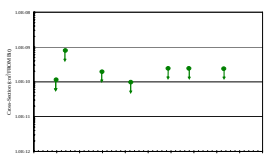


Fig. 16: FROM SEE Immunity

Total Ionizing Dose Effect

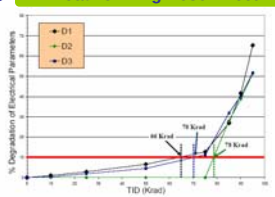


Fig. 17: D1, D2 and D3 Electrical Parameters Degradation vs. TID of X-ray Irradiation for three A3P250-PQ208 DUTs

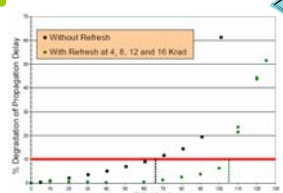
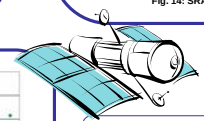
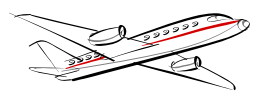


Fig. 18: Refresh Effects on the A3P250 DUTs



VERY LOW ERROR RATES
This device is ready for take-off !



CONCLUSIONS

- Except for the embedded FROM, which is very radiation hard, all the other programmable architectures are sensitive to SEE
- SEU and SET hardening are achieved by the implementation of soft macros. There are no Single Event Functional Interrupts (SEFI) or Latch-ups (SEL)
- For a complete SEE immunity at high frequencies (50 MHz and above), triplication of I/Os is mandatory in addition to their separation on 3 different IO banks.
- FPGA Core TID tolerance is hardened to 106krad(SiO_2) by a refresh scheme and the margining/programming circuit can withstand up to 40krad(SiO_2)
- As expected for a non-volatile FPGA, no observed error-event required a reconfiguration of the Flash-based FPGA nor were there any destructive SEE events.

REFERENCES

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