

# Actel's RTAX4000S Space Qualification Update

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### RTAX4000S Qualification Summary

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## Introduction



#### RTAX4000S is Actel's most recent and largest antifuse FPGA

- Wafers fabricated on 0.15 µm process at United Microelectronics Corp (UMC), Taiwan
- 4 million user gates
- System Solution 30 times the size of an RTSX32SU
- First Antifuse FPGA that offers up to 4 Million system gates with enhanced features:
  - Embedded RAM blocks
  - Extensive I/O standard support
  - Hardened charge pump, clock trees, Power On Reset circuit
  - TMR Flip Flops

	RTAX4000S
Equiv. System Gates	4,000,000
ASIC Equivalent Gates	500,000
Dedicated Registers	20,160
Max Registers	42,840
I/O Registers	2,520
Total Modules	60,4 <mark>8</mark> 0
RAM Blocks	120
Total RAM Bits	540K
Max User I/Os	840
Packages	352-CQFP 1272-CCGA/LGA

## **Qualification Vehicles**



#### RTAX4000S-CG1272 was used for the qualification

- Utilizing the largest package to ensure maximum number of I/O's were exercised
- Master design specially generated for the RTAX4000S
  - Design includes all types of reliability test designs used for RTAX-S
    - QBI: Maximizes resource utilization
    - EAQ: Uses highly perceptive and stressful designs for antifuse evaluation
    - HSB: Maximizes the utilization of single S-Antifuse and single B-Antifuse
    - TID, SEE blocks are also added in the Master design

#### Design Utilization

Inf	0					Utilization				
		Pins	Clocks				Logic Cells		Summary	
									seq +	Total
Device	Package	I/O	RCLK	HCLK	RAM/FIFO	Carry Chain	R-Cell	C-Cell	combo	Modules
RTAX4000S	CG1272	840	4	4	120	387	20,155	40,298	99.96%	60,453

- Different I/O standards are utilized in the design
  - Single ended, differential, and voltage referenced I/O's are configured

## **RTAX-S QBI block**



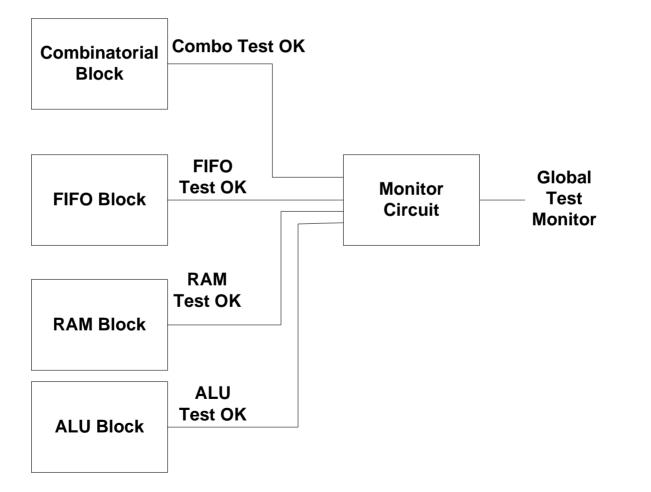
### Design Overview

- QBI (Qualification Burn In) design
- Goal of this design:
  - Maximum utilization of logic cells
  - Test all IO standards
  - Testing of all macros offered (like Carry chain, buffys etc)
  - Test RAM feature
- QBI block also used as Quality Control Monitor (QCMON) design in smaller devices

## **QBI DESIGN FEATURES**



Top level design includes different blocks to ensure testing of all device features with maximum utilization



### **EAQ Design Overview**

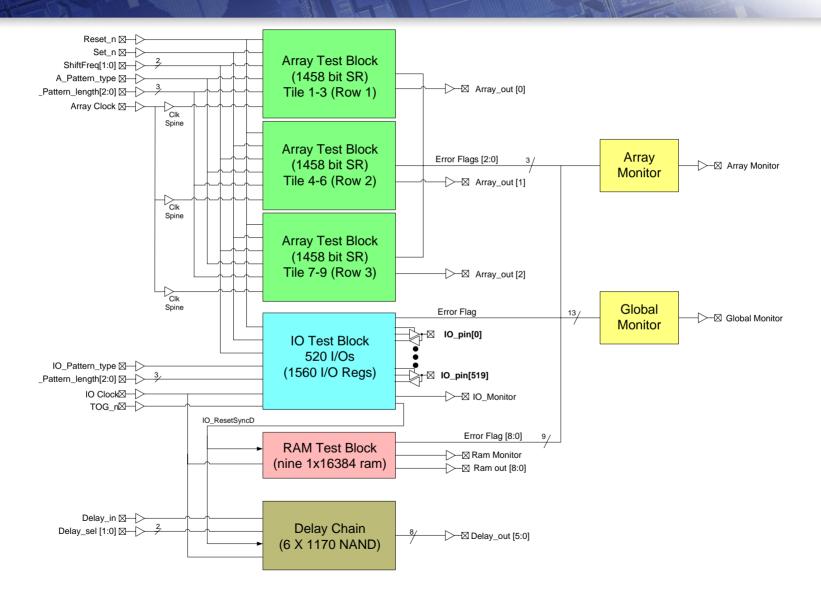


## Goal of Enhanced Antifuse Qualification (EAQ) design

- Design used for study of antifuse reliability experiment
- Design fully utilized smaller devices
  - ♦ RTAX2000S, RTAX1000S, RTAX250S
- Design has high perceptibility of delay measurement deltas
  - Multiple delay lines of combinatorial modules
  - ♦ I/O test block
  - RAM test blocks

## Top level diagram (EAQ Block)



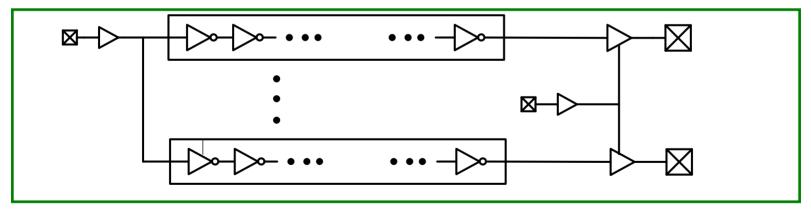


### **HSB Design Overview**



#### Goal of High Single-S and Single-B antifuse design

- Increase the utilization of Single-S and Single-B antifuse
- Short delay lines of combinatorial and sequential logic
- Multiple delay lines per device compared against each other at every burn-in pull point
  - Combinatorial delay lines shown below



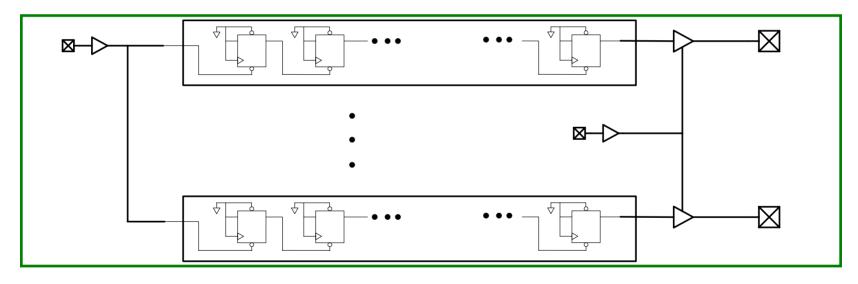
Combinatorial delay lines

## **HSB Design Overview**



#### Sequential delay lines

 Both sequential and combinatorial delay lines exercised during burn-in with the same 2 MHz clock frequency



Sequential delay lines

gnd



10

PRE

Q

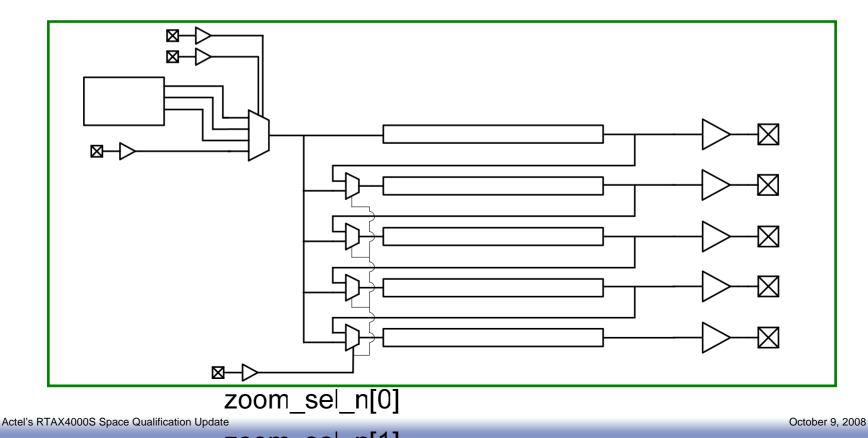
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### **SEU Combinatorial Delay Block**



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- SEU delay lines have longer delays compared to EAQ and HSB delay lines
  - The delay line could be exercised through an input pin or a clock divider block
  - Each delay line can be cascaded to make up one long delay line



# **Master Design - Antifuse Utilization**



Antifuse Type	Number of Antifuses	Description
F	69,251	Between module output segment & short vertical segment
н	21,370	Antifuse between two horizontal tracks
I	127,644	Between short horizontal segments & module input segment
S	42,710	Semi-direct antifuse
V	10,179	Antifuse between two vertical tracks
X	72,244	Antifuse Between short horizontal & vertical segments
К	14,379	Between routed clock horizontal segments & module input segment
CSR	10,144	Antifuse for I/O configuration options
SSR1	8	Silicon Signature antifuse in silicon signature words
LDH	600	Horizontal inter-tile antifuse
LDV	2,925	Vertical inter-tile antifuse
В	4,160	Between local segment (DB inverter output) & input segment
LL	10,219	Between RX/TX input/output module segment & long horizontal/vertical segment
Total Antifuses	1,265,487	

### **Qualification Experiments**



### Qualification was done with MIL-PRF-38535, Class EV Level Compliance

- Master Design used to program qualification life test devices
  - Tri-temp (-55°C,125°C, 25°C) functional testing performed
  - Qualification devices processed through class EV assembly and screening before programming
- Group C test
  - (High Temp Operating Life) HTOL stress at 125°C for 1,000 hours
  - ♦ 77 RTAX4000S-CG1272 devices were programmed for this test
  - Burn-In performed at maximum supply conditions of V<sub>CCA</sub>=1.6V & V<sub>CCI</sub>=3.6V
- Group A, B, D, ESD, Latch-Up, IO Capacitance were also performed
- Characterization completed with 2 lots of RTAX4000S
  - Characterization report available with the qualification report

### **Qualification Experiments Cont'd**



#### Qualification Experiments Cont'd

- LTOL (Low Temp Operating Life) test
  - ♦ 24 RTAX4000S devices were stressed for 1,000 hours of LTOL at -55°C
- Class B qualification of the RTAX4000S completed at the end of 2007
- Thermal runaway characterization completed
  - Thermal runaway characterization was completed up to junction temperature of 150C
  - No thermal runaway issues were found

#### Class V Qualification

- The 1,000 hours HTOL extended to 6000 hours to qualify the RTAX-S family as class EV device
  - Qualification devices completed 5000 hours HTOL with <u>NO</u> silicon failures
  - Class V qualification to be completed with the 6000hrs HTOL on schedule for Nov 2008
- Qualification devices have been processed through class EV flow
  - Class EV screening performed starting from assembly through blank device screening
- Same "Master" design will be used for production Enhanced Lot Acceptance (ELA) test

### **RTAX4000S Generic Burn-in**



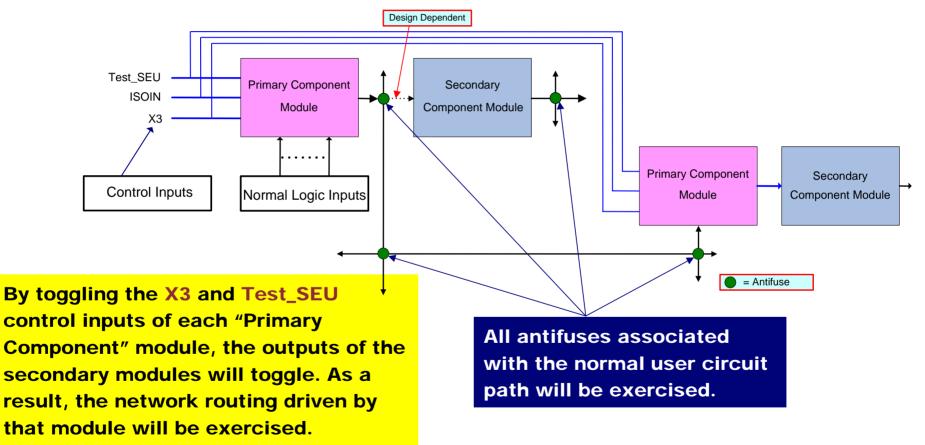
#### Generic Burn-in Features

- Actel customers will never need to generate specific test patterns for their programmed RTAX4000S design, <u>saving both time and costs</u>.
- ASIC burn-in test vectors often achieve less than 70% AC toggle coverage of the design whereas an Actel Generic Burn-in provides <u>complete network exercise</u>.
- <u>Specific Burn-in boards are not required</u> to accommodate custom user designs.
- RTAX4000S Programmed parts with <u>multiple designs can be burned-in</u> <u>simultaneously using</u> "Actel Generic Burn-In" boards.
- The generic burn-in test is implemented using <u>existing</u> global test circuit commands
- Simplified schematic of the combinatorial module test shown on next slide

## **Simplified Signal Path Schematic**



### Schematic of the combinatorial module path



### Generic Burn-in Verification and Qualification



- Verification of the Generic Burn-in concept was performed with software simulation and burn-in system
  - Bench level testing using dedicated Silicon Explorer probe pin outputs as well as TDO outputs verified cell toggling on all the available device features
  - Logging of pre and post burn-in data required
- Generic Burn-in qualification was completed with 1000 hours HTOL
  - Pre and post Burn-in data is logged and compared at each pullpoint
  - 24 RTAX4000S-CG1272 devices were used for the qualification
    - All devices passed successfully and no delay or faults were observed
    - These are the same devices which were used for the LTOL qualification

### Conclusion



- Actel has successfully completed the Mil-Std 883B qualification of the RTAX4000S
  - Reliability experiments with HTOL and LTOL were completed with <u>NO</u> silicon failures
- Generic burn-in feature verification and qualification was completed
- Class V qualification of the RTAX4000S will be completed with 6000 hour HTOL
  - 5000 hours already completed with no silicon failures and 6000 hours HTOL will be completed by November 2008
  - All qualification devices were processed through Class V process flow
  - This will establish Class V level compliance for RTAX-S products